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Addressing Thermal Challenges in High-Density Power Applications

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TECHNICAL NOTE

Demand for more features and higher performance from ever-smaller form factors presents significant challenges for engineers developing applications such as DC-DC conversion, computing, industrial motor drives, and telecommunications. In many cases, for example, enhancing capabilities and functionality can lead to the need for larger components and, consequently, demand for more cooling. Forced-air cooling can be cumbersome, unreliable and inefficient. Passive cooling using heatsinks adds bulk and cost to the design and, ultimately, the end product. Thermal issues can, effectively, stop innovation in its tracks.

Experienced power designers know that the best way to deal with heat is to not generate it in the first place, meaning that each design generation has to be more efficient than the previous. Correct selection of the topology and, more importantly, the power switching components, is critical to a successful design. However, all power circuits generate some heat, no matter how efficient they are. As designs get smaller, the opportunities for passive convection cooling are reduced and designers have to find intelligent and innovative ways to thermally connect semiconductor junctions to the ambient environment where the heat can dissipate.

Not only does the package affect thermal performance, the leads themselves can also have an impact. For instance, packages with longer leads introduce parasitic elements into the circuit that can affect both speed of operation and efficiency.

DUAL COOL® Advances PQFN Packaging

Pursuing a strategy of power density leadership, ON Semiconductor has developed a power-specific packaging technology to meet the escalating demand for improved thermal management in modern electronic designs. Based on industry-standard Power Quad Flat No-Lead (PQFN) packaging, ‘Dual Cool’ technology creates a direct heat path from the drain and source sides of the vertical MOSFET die structure through the addition of a heat slug to the top of the package. This structure allows for supplemental cooling on top of the package with a heatsink system while also providing a direct thermal conduction path into the printed circuit board (PCB).

Dual Cool package construction is an evolutionary extension of the popular PQFN form factor, incorporating new features to meet future performance expectations. By retaining the very popular Power33 and Power56 lead geometries and pinouts, the package allows designers to improve heatsink performance in existing PCB pad designs. Customers currently using a heatsink on the surface of a PowerQFN package will find this a very useful feature, allowing an easy transition.

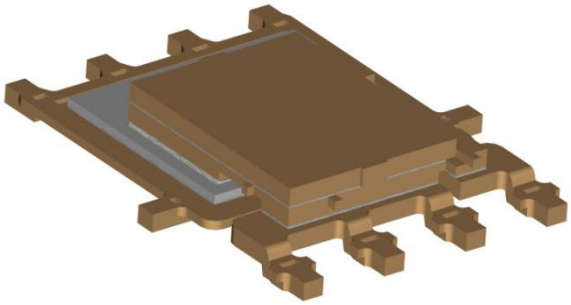

Figure 1. Solid Model Illustrating Dual Cool Package Construction

Copper clips, similar to leadframes, replace wire bonding inside the Dual Cool concept. Not only does this approach improve thermal conductivity but it also increases current handling capability within the compact PQFN form factor, thereby enabling higher power densities with excellent thermal properties. In fact, the standard PQFN package using the clip technology offers a 13.9% improvement over the wire bond-based PQFN package. Dual Cool technology further improves the performance differential to 57.5% in a 5×6 mm package.

Environment: Minimum Pad, Heat Sink, 200 LFM Forced Air

5 x 6 Package Interconnect	Q_{JA} (°C/W)	(%) Improvement from Wire Package
PQFN Wire	27.1	—
PQFN Clip	23.8	13.9
Dual Cool Package	17.2	57.5

Figure 2. The Cu Clip Offers Significant Improvement in Performance

Dual Cool uses 4 mils thin silicon as the core package design constraint. This represents half the thickness of the typical MOSFET that traditionally used 8 mils thick silicon dice. By reducing the die thickness to 4 mils, thermal and electrical performance are improved. This is thanks to the lower parasitic resistance created by the bulk resistance from the doped silicon area through which electrons flow to get from the trench structure at the top of the wafer to the drain lead frame connection at the bottom.

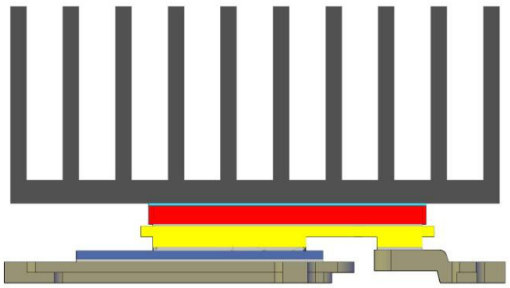

Figure 3. Cross Section of Dual Cool and Heatsink Assembly

The top and bottom surfaces of the die are plated with solderable metal to permit solder attachment of the drain lead frame on the bottom, and the source and gate clips on the top. To improve the heat transfer path from the die to the top of the package for use with a heatsink, a heat slug is soldered to the source clip. This is exposed on the top of the package to provide the heatsink interface.

Solder attachment of the silicon to the lead frames, with optimized copper clips additionally reduces electrical and thermal parasitics. The θ_{JC} (thermal resistance from the junction to the case) has two important values with this package type: the junction to case thermal resistance to the drain tab as well as the top heat slug. The datasheet offers these values for each specific product type. These numbers are a measure of the two efficient heat paths out of the component, giving the designer options for managing the heat loads created by high power density designs.

DUAL COOL Enhances POWERTRENCH® MOSFETs

ON Semiconductor's PowerTrench MOSFETs offer excellent electrical properties including very low levels of $R_{DS(on)}$. The fully RoHS-compliant products include an integrated monolithic SyncFET™ Schottky body diode making this technology a leading choice for power designers. PowerTrench SyncFETs became a natural choice to benefit from the new Dual Cool packaging concept. The combination of Dual Cool and PowerTrench occupies the same land pattern as 5 × 6 mm and 3.3 × 3.3 mm PQFN−JEDEC standard parts, yet allows for > 60% better thermal performance.

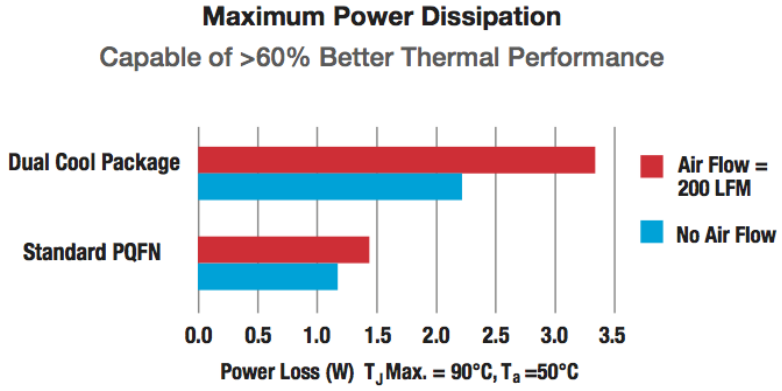

Figure 4. Dual Cool has > 60% Better Thermal Performance than PQFN

The Dual Cool PowerTrench MOSFETs with top-side cooling have a far better thermal coupling to the top of the device. In many cases, they can be used without an additional heatsink thereby reducing size, cost and weight. With enhanced dual-path thermal performance and improved parasitics over its wire-bonded predecessors, the use of a heatsink provides even more impressive results.

Laboratory testing proves that when a heatsink is used with Dual Cool package technology, synchronous buck converters deliver higher output current and increased power density. With ON Semiconductor's trench silicon technology, Dual Cool packaging proves to be a clear leader in both power density and thermal performance.

Figure 5. PQFN Based Dual Cool Packaging

The Dual Cool portfolio offers in excess of 20 products with BVD_{SS} covering the range 25 V to 150 V and a number of choices for $R_{DS(on)}$ and package size.

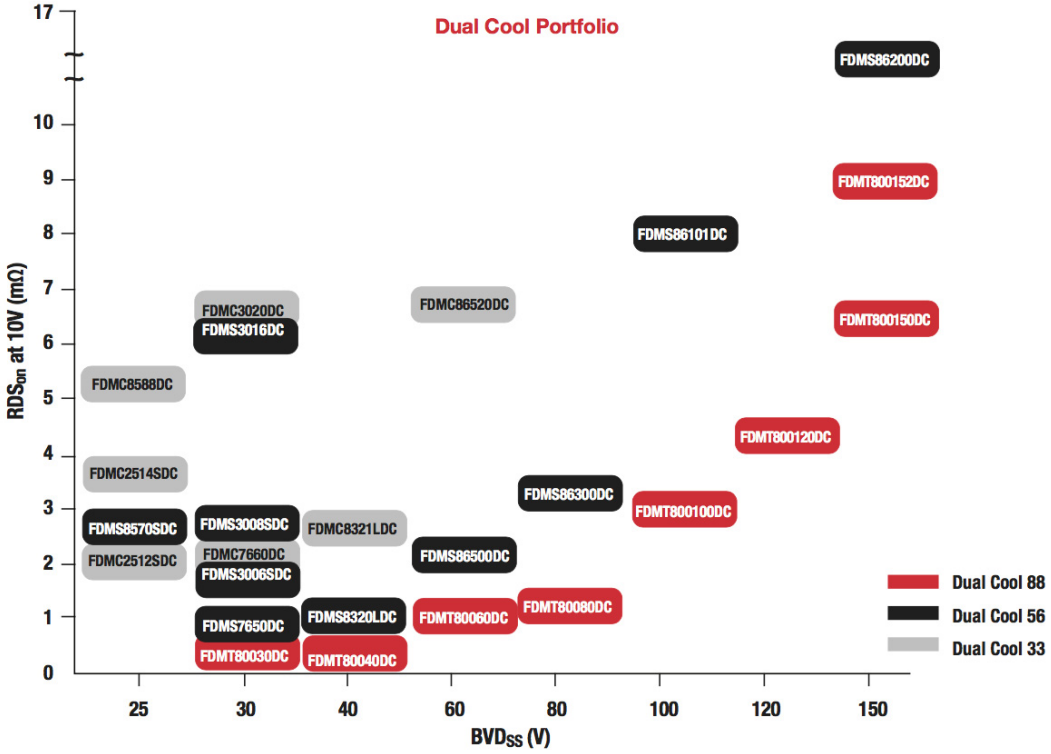

Figure 6. The Broad PowerTrench/Dual Cool Portfolio Offers Designers Choices

Dual Cool solutions are lead-free, RoHS-compliant, and available in 3.3 × 3.3 mm, 5 × 6 mm, and8 × 8 mm PQFN packages.

Use with Heatsinks

Depending on the size of any heatsink used on the top-side of the package and any air flow that may be present, the thermal resistance from the semiconductor to ambient can be further improved.

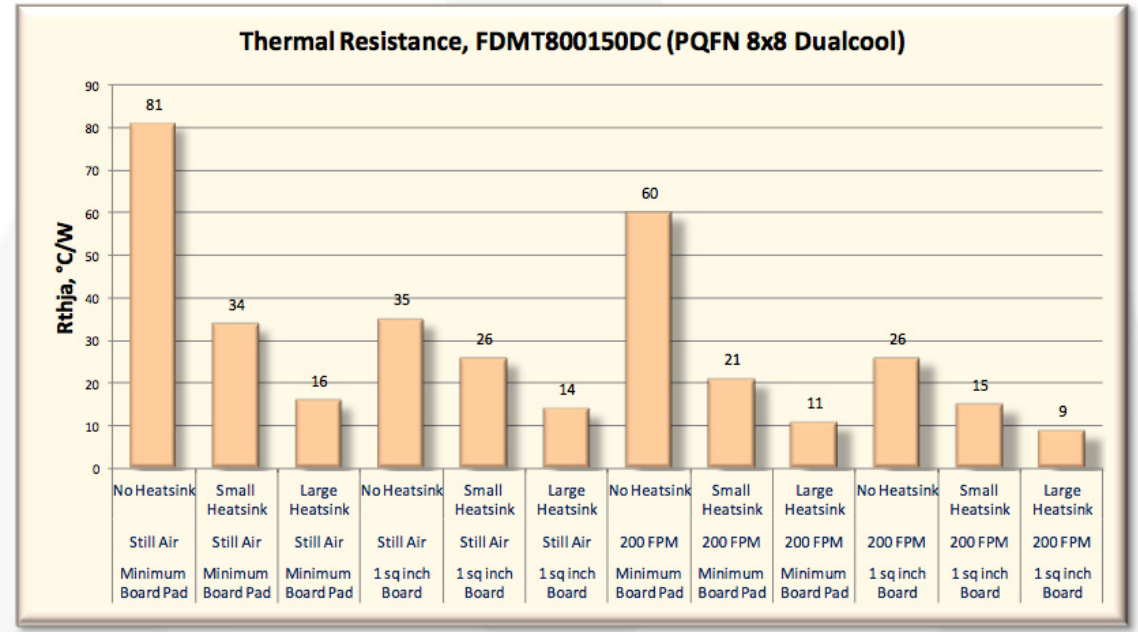

Figure 7. Comparison of Various Cooling Modes

In Figure 7 above, the large heatsink is aluminum measuring 45.2 × 41.4 × 12.7 mm, and the smaller one is 20.9 × 10.4 × 12.7 mm.

Various types of heatsinks are available and the design, form factor, and mechanism for thermal dissipation will depend on the application, available space and heat to be dissipated. Methods of attachment also vary and include solder anchoring, push pin, thermal tape, screwing, or glue/adhesive.

Thermal interface materials can be used to improve the contact between the Dual Cool package and the heatsink and eliminate the possibility of air gaps in the interface that will limit heat dissipation.

Thermal interface materials (TIM) are available in many forms and include the following:

- Thermal Grease
- Insulating Pad
- Phase-change Materials
- Thermal Tape
- Gap Filler Sheet or Gel
- Thermally Conductive Glue or Adhesives

Testing by ON Semiconductor has shown that thermal grease provides an across-the-board improvement over gap filler sheets. It was found for the wire bonded units that performance improved 10% over gap pad, for the clip bonded 12%, and for Dual Cool performance improved 21% over the Gap Pad.

This represents a theoretical improvement in allowable dissipated power from 5.8 W with the gap pad to 7.0 W with the grease. Grease is the best performance-wise, but is more difficult to dispense, rework and does not have the electrical isolation properties of the pad. The application will dictate if these trade-offs are worth making.

In applications where tightening a screw, a push pin, or a solder anchor is used to secure the heatsink, a compression load is placed on the component. The PQFN 8 × 8 Dual Cool package has been tested and simulated to withstand high compression loads. Results show that the package can withstand up to 1500 N of load without causing any electrical or mechanical failure.

PCB and Manufacturing Considerations

PQFN packages are widely used for low-voltage applications. Due to the small configuration and low profile, these packages provide a good space-saving alternative to the typical leaded options. The Dual Cool package offers a size advantage over the industrial standard D2PAK SMD package.

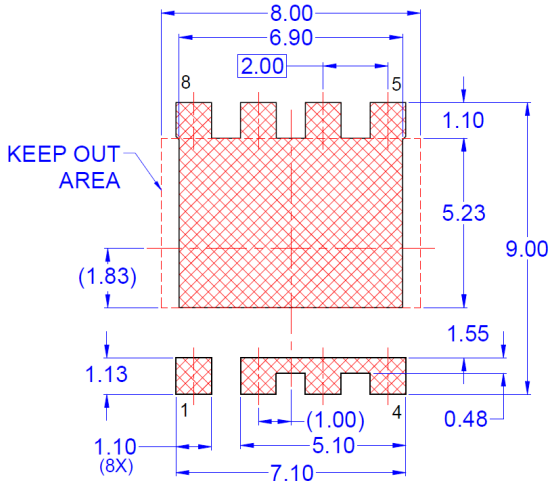

Figure 8. Recommended Land Pattern for 8 × 8 PQFN (Dimensions in mm)

The source and gate pads are larger than the package lead to allow toe filleting of the solder. The pads are also wider than the leads, providing allowance for variation in board fabrication and component placement during assembly. Combined, these tolerances can stack up to 0.10 mm.

The land pad for the exposed thermal pads is identical to the size of the exposed pad. This large connection between the board and the component allows the strong surface tension of the molten solder to pull the component so that it perfectly aligns with the land pad. Correct PCB layout will ensure that the Dual Cool packages are consistently aligned during production.

In power applications where a large amount of heat is generated during operation, the Cu land pattern provides a larger area for heat to be dissipated into the PCB itself.

On the thermal characterization of PQFN 8 × 8 Dual Cool packages, there is significant improvement in the thermal resistance from junction to ambient if the Cu registration on the printed circuit board is increased from a minimum pad to a larger (say 1 in^2) Cu pad connected to the solder-mask-defined land pad.

Therefore, it is recommended that the drain pad on the board be routed and connected to a large Cu area on the board for heat dissipation.

Summary

Clearly the combination of PowerTrench technology with the Dual Cool packaging concept addresses the two fundamental challenges of modern power design; operating as efficiently as possible to minimize heat generation and then transmitting what heat is generated as efficiently as possible from the semiconductor junction to the ambient environment.

In some applications, the package can be used without additional cooling and, where additional cooling is required, a heatsink can be mounted easily to provide substantial thermal performance gains.

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