JFET and Combo JFET User Guide

Operation Tips for the **onsemi** SiC JFET and Combo JFET

UM70113/D

Scope

This document explains example circuits for using **onsemi** SiC JFETs and Combo JFETs in semiconductor-based circuit protection and relays.

Introduction

onsemi offer discrete SiC JFETs and Combo JFETs, which contain the same SiC JFET and a low-voltage silicon MOSFET connected in series and with each gate accessible at a package pin. The on-resistance of **onsemi** SiC JFETs and Combo JFETs is low enough to replace electromechanical breakers and relays as a current switching element. Increased safety, service life, and controllability motivate this transition, enabling new functionality such as remote switching, load scheduling, and data acquisition. While the SiC JFET has significant advantages, particularly lowest on-resistance for a given chip area, known as R_{DS}·A, and no parameter drift even after repeated high energy transients, it is quite different from competing technologies.

This user guide covers both SiC JFETs and Combo JFETs offered by **onsemi** and is intended to help equipment manufacturers to successfully utilize them to their fullest advantage. Simple drive circuits are presented that apply to both JFETs and Combo JFETs and minimize conduction loss while reverting to normally off state in the absence of control power. For further background on how the **onsemi** SiC JFETs and Combo JFETs are constructed and operate, please refer to the SiC JFET Primer and SiC Combo JFET Technical Overview.

onsemi SiC JFET Basics

Familiarity with the output characteristics, transfer and gate characteristics, and capacitances is helpful to understand how to use the SiC JFET and Combo JFET.

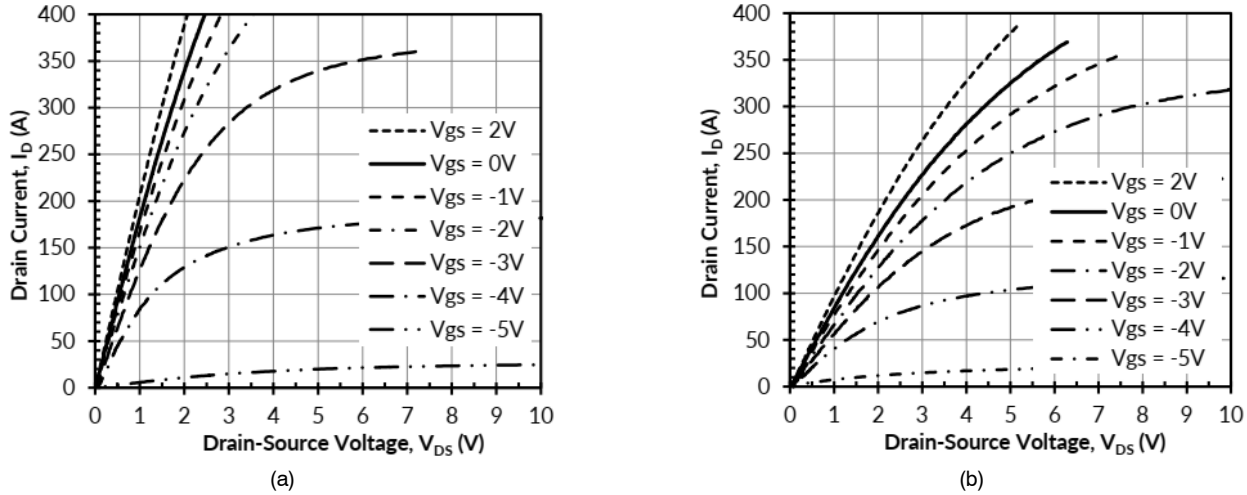

Figure 1. UJ4N075004L8S SiC JFET Output Characteristics at (a) 25 °C, and (b) 175 °C

Figure 1 shows the output characteristics with various gate-source voltages at room temperature (a) and maximum operating temperature (b) of a 750 V, 4.3 mΩ SiC JFET in a TOLL (MO-229) package, part number UJ4N075004L8S. The negative threshold voltage is evident in these graphs, with a typical value of −6 V for this JFET. A gate-source voltage at least 2 V less than the minimum threshold voltage is needed to keep the JFET off. The UJ4N075004L8S has a minimum $V_{G(th)}$ of −8.3 V, so a maximum keep-off voltage would be −10.3 V, whereas −12 V or less is recommended.

The ohmic (straight line) area of the graphs in Figure 1 show that conductivity increases (resistance decreases) with increasing V_{GS}. The JFET is considered fully on with V_{GS} = 0 V, but on-resistance decreases by 15% by further increasing V_{GS} to about 2 V. This reduced on-resistance is "low hanging fruit" that is easily harvested, as will be shown. But first, another observation from Figure 1 is the temperature dependance of $R_{DS(on)}$, which is 1.63 times higher at 125 °C versus 25 °C, and 2.18 times higher at 175 °C versus 25 °C. This temperature coefficient (TC for short) of $R_{DS(on)}$ is mostly due to the bulk SiC material in the JFET. The $R_{DS(on)}$ TC must be considered when selecting a SiC JFET part number and deciding how many to parallel.

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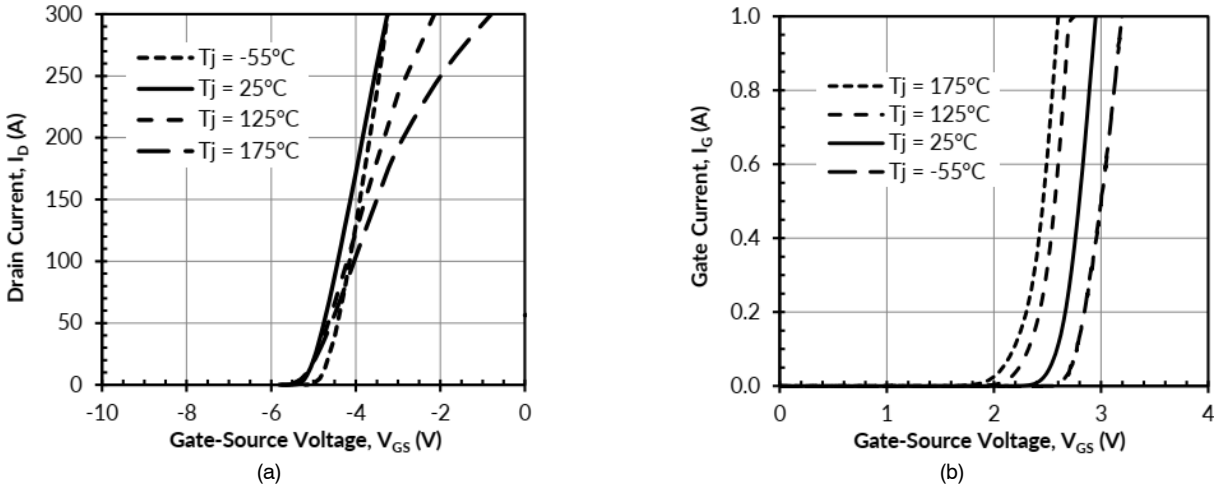

Figure 2. UJ4N075004L8S (a) Transfer Characteristics and (b) Gate Current versus Voltage

Figure 2(a) shows the UJ4N075004L8S transfer characteristics. From the slopes of the straight-line portions of the curves, the transconductance at 25, 125, and 175 °C is 164, 113, and 90 A/V respectively. There is very little crossover of the 25, 125, and 175 °C transfer characteristic curves, which is due to the quite flat threshold voltage temperature coefficient (TVTC) of only −1.8 mV/°C for this **onsemi** Gen4 SiC JFET. A flat TVTC greatly reduces a chance of a thermally unstable hot spot forming on the chip during active mode operation and high current switching. This is one of the reasons the **onsemi** SiC JFET is so reliable. Another is no degradation or parameter drift, thanks to the simple electrical structure of the JFET. Please refer to the JFET Active Mode Application Note for further details.

Figure 2(b) shows the UJ4N075004L8S gate current versus V_{GS}, where the SiC JFET gate-source diode is forward biased. The temperature-dependent diode "knee voltage" is plain to see, and the slope corresponds to the JFET gate resistance, which for this part is 0.4 Ω. Notice that V_{GS} is in a range of about 1.8 to 2.6 V with I_G in the milliamps range, with temperature spanning from −55 to 175 °C. Also gleaned from this graph is the JFET's gate-source diode forward voltage temperature coefficient, which is about −3.4 mV/°C. This parameter can be used to sense the JFET chip temperature.

There are a few points to consider regarding forward-biasing the JFET gate. First, it is safe for the JFET unless the gate current exceeds several Amps continuously. More obvious is the fact that an external gate resistor is required to limit the gate current; the internal JFET gate resistance is too low for this. Third, the reduction in $R_{DS(on)}$ by forward-biasing is due to the further widening of the JFET channel rather than carrier injection, as explained in the JFET Primer. On-resistance can be even further reduced by injecting enough gate current to result in bipolar current flow (electrons and holes), but any benefit from this would be countered by the high gate drive power required. Finally, the values of I_G and V_{GS} during forward-bias are not critical. Simple drive circuitry allows I_G and V_{GS} to vary with temperature while remaining within completely safe ranges.

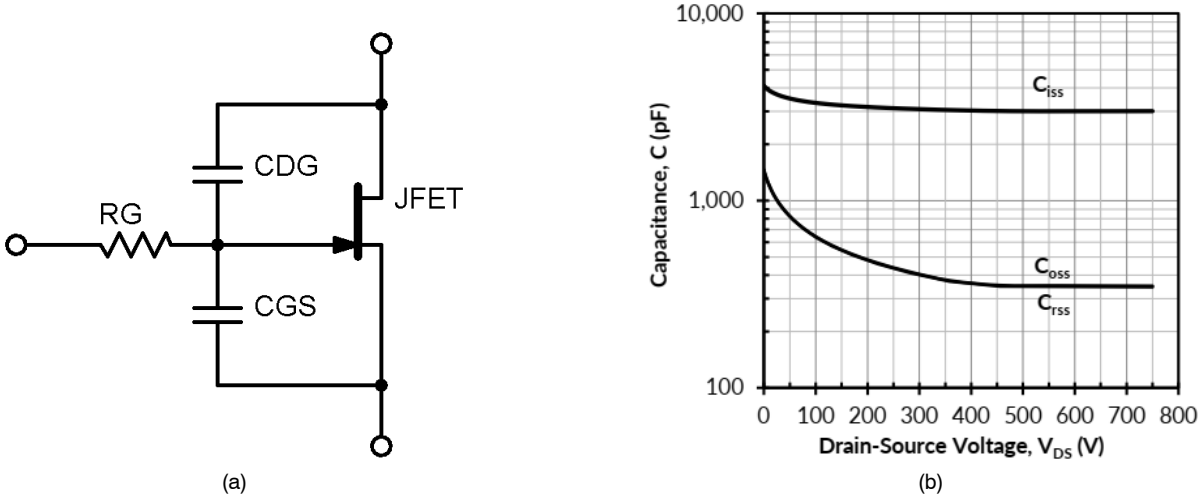

Figure 3. (a) onsemi SiC JFET Symbol with Intrinsic Capacitances and Gate Resistance (b) UJ4N075004L8S Capacitances versus V_{DS}

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Figure 3(a) shows a JFET symbol with drain-gate capacitance (CDG), gate-source capacitance (CGS), and on-chip gate resistance (RG). The input capacitance C_{iss} in the graph of Figure 3(b) is the parallel combination of the drain-gate (same as C_{rss}) and gate-source capacitances, and we see that most of the input capacitance is from the gate-source capacitance. A unique feature of **onsemi** Gen3 and Gen4 SiC JFETs is the lack of drain-source capacitance, resulting from no P−N junction in the drain-source current path and no body diode feature. Output capacitance C_{oss} is the parallel combination of drain-source and drain-gate capacitances, and it is directly related to chip size regardless of technology (JFET, MOSFET, IGBT, etc.). Because the drain-source capacitance is practically zero, all the output capacitance is from the drain-gate capacitance, designated as C_{rss}. This is why C_{oss} and C_{rss} are equal in the capacitance graph in Figure 3(b). This is a desirable feature for circuit protection and relay applications, and it has significant implications for switch-mode applications.

Gate Drive of onsemi SiC JFETs for Circuit Breakers and Relays

Requirements for a semiconductor circuit breaker (SCB) or relay commonly include the following:

- Low power loss
- Bidirectional blocking
- Normally off state
- Off-the-shelf components
- Reliable
- Simple
- Low cost

Low power loss and low cost are opposite each other on a tradeoff circle that has shrunk enough for commercialization of SCBs based on low $R_{DS(on)}$ SiC JFETs from **onsemi**. The SiC JFET is the centerpiece of a SCB or relay, supported by readily available, low-cost components in a simple, reliable design. Most SCB applications require a normally off state during power-up, whereas some semiconductor relays require a normally on state. The normally on **onsemi** SiC JFET works well for both because it is kept in a normally off state with the addition of a few simple components, even without control power.

There are many possible drive circuits for a JFET in a SCB or relay. This user guide shows examples with “overdrive” to positively bias the JFET gate and hence minimize the on-resistance. Bypass capacitors, pulldown resistors, and other components are omitted for clarity. Component and circuit values are recommendations only and are not mandatory values.

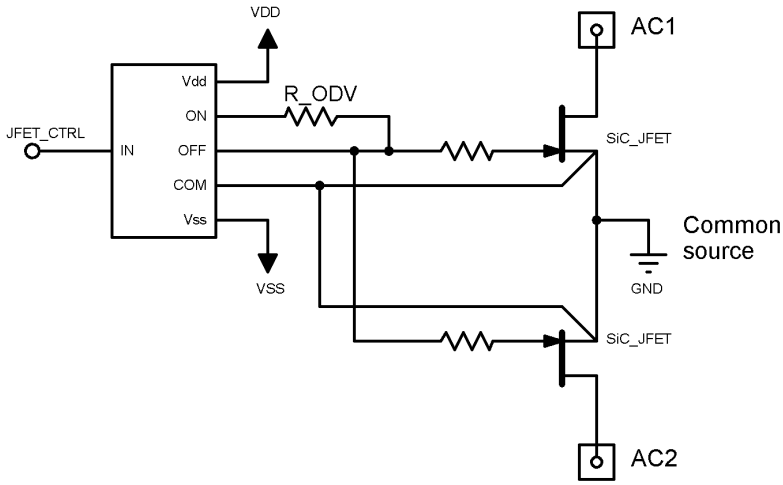

Figure 4. Direct Drive Circuit with Bidirectional Blocking and Normally On State

Normally on state is desirable for some semiconductor circuit protection and relay applications. Figure 4 shows an example of a bidirectional blocking configuration with simple overdrive of the JFETs. This circuit is normally on, meaning that in the absence of gate drive power the JFETs are on. An off-the-shelf gate driver directly drives the gate of each JFET. The Kelvin-source of each JFET is connected to the common pin (COM) of the gate driver, which also connects to the gate drive power supply common (not shown). JFET switch-on is through a large value gate resistor, labeled R_ODV. No voltage regulation is required. You can think of R_ODV combined with the JFET gate-source diode acting as a simple voltage regulator. The example circuit in Figure 4 shows a gate driver with separate ON and OFF connections, but a single-output gate driver would also work with an additional steering diode to use R_ODV only for switching and keeping the JFETs on. The value of R_ODV depends on the desired JFET gate current in the on state.

Suppose that in the example circuit in Figure 4, the gate driver supply voltages V_{DD} and V_{SS} are ±15 V and that R_ODV = 1 kΩ. With gate current in the milliamp range, the JFET V_{GS} is about 2.3 V at room temperature. The approximate gate driver current is therefore

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$\frac{15\,V - 2.3\,V}{1020\,\Omega} = 12.5\,mA$ total. The corresponding gate drive power consumption would be 15 V · 12.5 mA = 0.19 W. Approximately 6.2 mA flows into each JFET gate. This is a good amount for both on-resistance reduction and on-chip temperature sensing in the lowest $R_{DS(on)}$ JFETs and Combo JFETs. A current of at least 1 mA is sufficient to forward-bias the JFET gate and reduce the $R_{DS(on)}$, whereas 5 to 10 mA is recommended for easy temperature sensing. Note that switch-on speed is slow with the large on-state gate resistance, at least relative to switch-mode applications, but this is desirable for many SCB and relay applications.

The JFET gate driver negative supply voltage can range from the minimum allowed, which is usually −30 V, to a recommended maximum of −12 V for V_{SS}, or as mentioned before, an absolute maximum of 2 V below the SiC JFET's minimum threshold voltage value found in the datasheet. The positive supply voltage depends on the selected gate driver's undervoltage lockout (UVLO) rating. For example, the MOSFET driver UCC5304 can have as little as 6 V for V_{DD}, in which case the on-state gate resistance can be correspondingly adjusted.

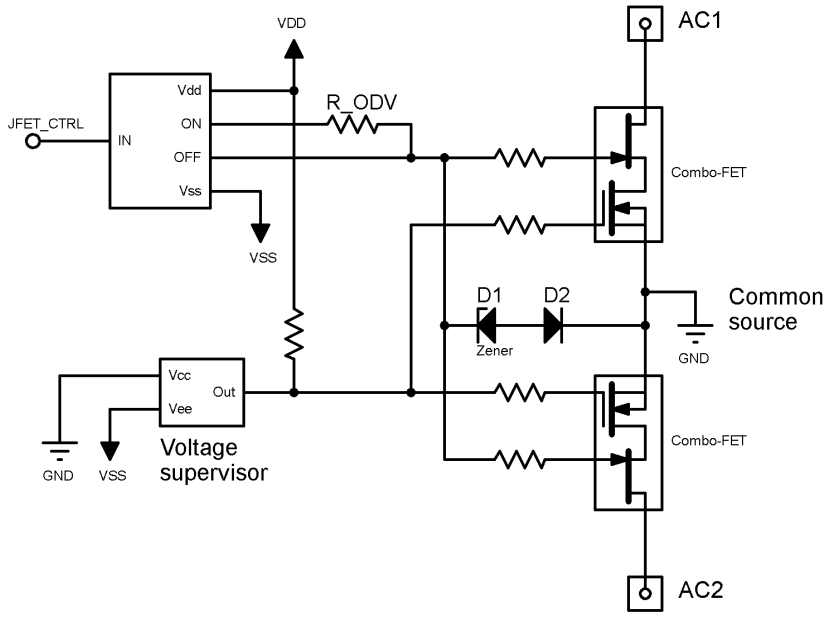

Figure 5. Direct Drive Circuit with Bidirectional Blocking and Normally Off State

Figure 5 shows an example of a bidirectional blocking configuration with simple overdrive of the JFETs. Normally off state is achieved by connecting a low voltage silicon MOSFET in series with each JFET and connecting each JFET gate to its MOSFET source with a Zener diode (and an anti-series diode). Each JFET is packaged with a MOSFET in Figure 5, which is a Combo JFET. If we use separate JFETs and MOSFETs instead of Combo JFETs, the voltage rating range for the silicon MOSFET is 20 to 30 V. An off-the-shelf gate driver directly drives the gate of each JFET, whereas each MOSFET is controlled by a voltage supervisor, keeping the MOSFETs on whenever the gate drive supply voltage is within operating range. The "block diagram" voltage supervisor in Figure 6 monitors the negative gate drive voltage so that the MOSFET remains off until the JFET can be reliably switched off by the JFET gate driver. This voltage supervisor could just as well be replaced by a gate driver so that the MOSFETs and JFETs are separately controlled.

JFET switch-on and overdrive is through a large value gate resistor R_ODV. This makes switch-on slow, but this is usually desirable for circuit breakers and relays. Adding a speedup capacitor plus diode between the gate drive ON output and the JFET gate effectively increases switch-on speed. The JFET gate-source diodes have a temperature-dependent forward voltage up to about 2.6 V when extremely cold. This means that the Zener diode D1, with a BV of at least 3 V, will not activate with the MOSFETs on, and small current flows into each JFET gate as desired.

The diode D2 in anti-series with the Zener diode allows the gate driver to pull the JFET gates negative. Note that D2 could be a Zener diode. Its BV must exceed $|V_{g(JFET_th,min)} + BV_{D1}|$ by a few volts. During normal switch-off, the MOSFETs are kept on, and it is as if the Zener diode is out of circuit. Its sole purpose is to switch off the JFETs in the absence of gate drive power, such as during startup. In this circumstance, with rising voltage across the AC power terminals, voltage rises across the MOSFETs, which are normally off. When this voltage exceeds the Zener BV plus the magnitude of the JFET threshold voltage, the JFETs are off, so no current flows, even if the voltage across the AC terminals reaches hundreds of Volts.

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An important point about this direct drive circuit is that the MOSFETs do not avalanche, and therefore they have very little stress. They are simply left on and treated as an enable. Their only function is to keep the JFETs off in the absence of control power should there be high voltage present at the power terminals. Furthermore, there is direct control of both di/dt and dv/dt during switching simply by adjusting the JFET gate resistance. Note that the gate driver's negative supply voltage V_{ss} must be sufficiently negative to switch off the JFET. A value of −12 V or less is recommended, or at most 2 V below the minimum JFET gate threshold voltage.

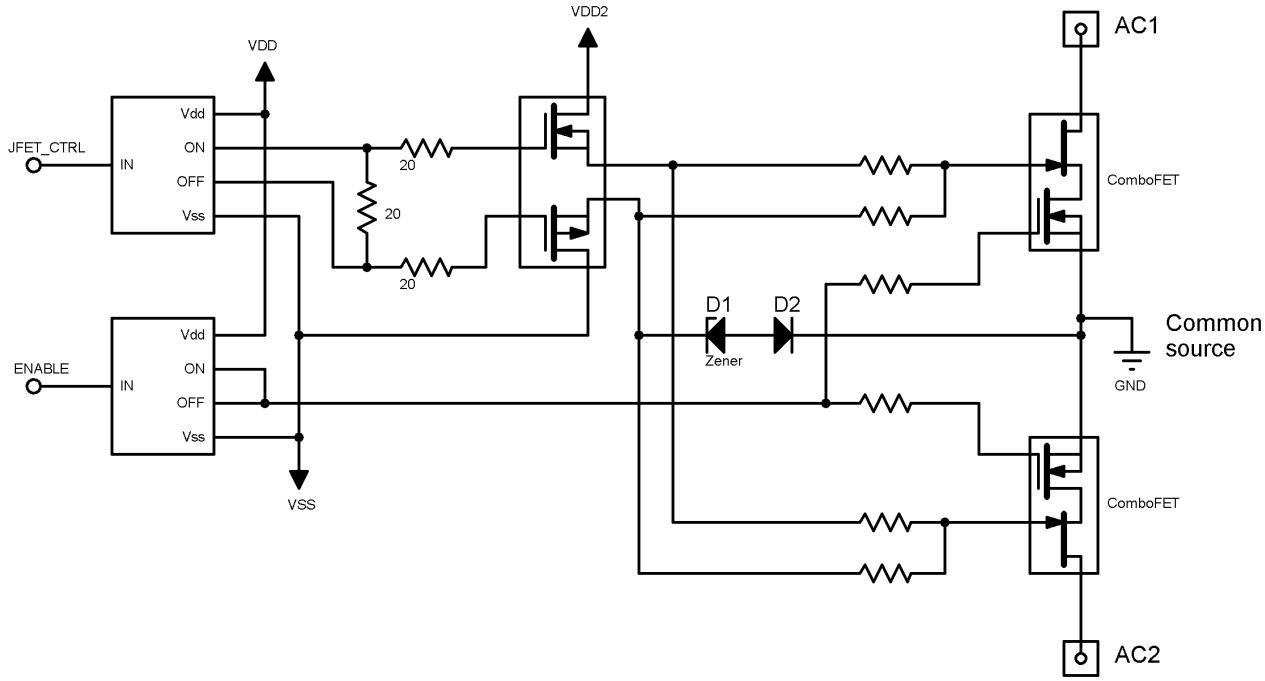

Figure 6. Modified Direct Drive Circuit Example

Figure 6 shows three modifications to the example circuit in Figure 5. First, the voltage supervisor is replaced by a separate gate driver for the MOSFETs. The MOSFET and JFET gate drivers can share the same power supplies. Second, the high-value on-state resistor R_ODV is replaced by an N-channel source-follower MOSFET (top MOSFET in the box) with a lower voltage V_{DD2} connected to the drain. With V_{DD2} in the range of 2.5 V to 5 V, there is no need for a large gate resistance. A reduced V_{DD2} alters the tradeoff between switch-on speed and current injected into the JFET gates compared to the drive circuit in Figure 5. The upper source-follower MOSFET acts as a voltage shifter, with its gate driven to a typical range of 6 to 15 V (V_{DD}) depending on the selected gate driver but supplying 2.5 V to 5 V (V_{DD2}) to the gate resistors of the JFETs. This MOSFET can also act as a buffer for higher gate current capability. Third, a switch-off P-channel source-follower MOSFET is added, which is needed to isolate the required gate pulldown resistor that switches off the N-channel source-follower MOSFET. This P-channel MOSFET also acts as a current buffer. This buffered drive circuit could also be useful for switch-mode applications such as motor drives.

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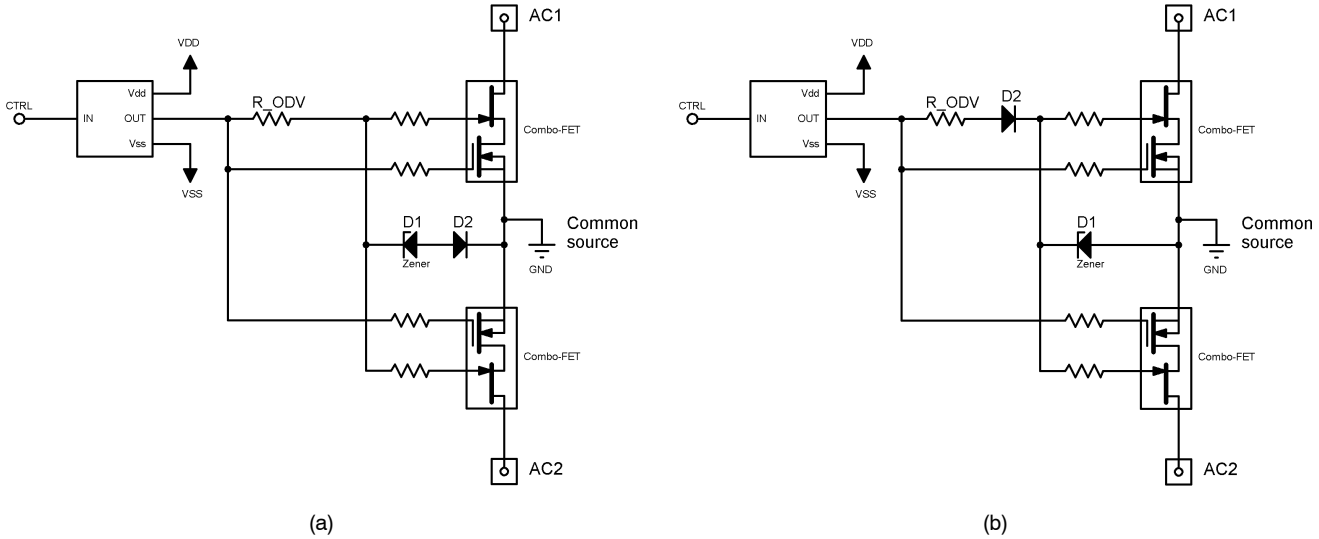

Figure 7. Quasi-cascode Drive Circuit with Bidirectional Blocking and Normally Off State

Figure 7 shows an example of a bidirectional blocking configuration, again with simple overdrive of the JFETs. Normally off state is achieved by connecting a low voltage silicon MOSFET in series with each JFET in a quasi-cascode configuration. Figure 7 shows Combo JFETs that contain both the SiC JFET and silicon MOSFET in a single package, but this and other circuits function identically with the MOSFETs separate from the JFETs with instead. When using separate JFET and MOSFET, the voltage rating of the silicon MOSFET can be in the range of 20 to 30 V; it must avalanche below 45 V. An off-the-shelf gate driver directly drives the gate of each MOSFET and overdrives each JFET. This simple drive circuit is part of a provisional patent application P241546-US-PRV.

As the control signal switches on, some gate current continuously flows through R_ODV into the JFET gate. In (b), as each MOSFET switches on, some additional JFET gate current flows through the corresponding series MOSFET, through the Zener diode D1, and finally through the corresponding JFET gate resistor into the JFET gate. This happens until the JFET completes its V_{DS} transition (if any, by switching other than at a line-voltage zero crossing), and then the current through the Zener diode decays to zero. In (a), switch-on gate current flows only through R_ODV, therefore switch-on speed is slightly slower than for (a). Note that the MOSFET switches on faster than the JFET due to the large value of R_ODV and typically lower MOSFET versus JFET gate charge. The steady-state JFET gate current is limited to the desired value based on V_{DD} of the gate driver and the value of R_ODV. The JFET gate-source diodes have a temperature-dependent forward voltage of 1.8 V to 2.6 V, therefore the Zener diode, with a BV of 3 V or more is reverse biased.

In (b), the JFET switches off entirely by cascode action. The MOSFET V_{DS} increases, which increases the JFET source potential past $|V_{(G(th)}| + BV_{Zener}$ and switches off the JFET. JFET gate current flows out of the gate through the JFET gate resistor and in reverse direction through the Zener diode. The optional diode D2 in series with R_ODV prevents current from backflowing through the Zener diode and R_ODV and wasting gate drive power. In (a), additional switch-off gate current can flow through R_ODV, therefore switch-off speed is slightly faster than for (b). For both circuits, there is no need to worry about JFET versus MOSFET switch-off timing. The JFET automatically switches off with the MOSFET.

If the voltage between the JFET drain and the common source point exceeds the breakdown voltage of the MOSFET (as when away from the AC zero crossing), then the MOSFET will avalanche during JFET switch-off. An exception is if the JFET gate resistance is extremely small, but this results in unacceptably fast switch-off for circuit breakers and relays. This raises three important points. First, switching at the AC zero crossing reduces the switching stress on the JFET and MOSFET, but waiting for a zero crossing may be undesirable during a fault condition. Second, the MOSFET must be capable of high current, single pulse avalanche. Many low-voltage Si MOSFETs have this, and the MOSFETs in Combo JFETs are 100% tested for this. Third, the higher the JFET gate resistance is, the longer the MOSFET is in avalanche. This is one factor putting an upper limit on JFET gate resistance. Another factor is the energy in wire or cable inductance that must be absorbed during switch-off. Too large a JFET gate resistance causes excessive switch-off energy in the JFET chip, which can cause a failure. On the other hand, too small a JFET gate resistance causes high voltage transients that are difficult to absorb with external components. See Table 1 for maximum switching energy recommendations.

The JFET output capacitance is charged by current through the JFET gate resistor, providing excellent control of voltage slew rate (dv/dt) and damping when switching. However, with this quasi-cascode configuration, there is significantly less change in current slew rate (di/dt) versus

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JFET gate resistance compared to other drive methods. For example, the quasi-cascode JFET gate resistance could be a factor of three or more higher than that of direct drive to achieve the same switch-off di/dt. Increasing gate resistance of course increases the switching delay time, which can be significant. Two ways to further reduce di/dt and hence peak voltage when switching off high current are:

- Decrease the voltage rating of the MOSFET. The MOSFET must avalanche at a voltage that is greater than the magnitude of the minimum JFET gate threshold voltage. When using separate MOSFET and JFET, the recommended voltage rating for the MOSFET is 20 to 30 V, and it must *avalanche* below 45 V. A 20 V versus 30 V rated MOSFET results in lower di/dt because of lower magnitude voltage to the JFET gate-source. Note that the MOSFET in a Combo JFET is designed to avalanche at about 25 V.
- Increase the MOSFET gate resistance, which decreases di/dt in this quasi-cascode drive circuit, but it has very little effect on dv/dt. In contrast, changes in the JFET gate resistance in the quasi-cascode drive circuit has little effect on di/dt, but it has a strong effect on dv/dt.

Since switch-off in this simple drive circuit is by cascode action there is no need for the gate driver V_{SS} to be more negative than the JFET $V_{G(th)}$. In fact, V_{SS} can be zero. Opinions differ on an optimal value for V_{SS}. The author recommends −3 to −5 V to improve noise immunity. Even though circuit breakers and relays switch rarely (unlike switch-mode circuits), the switching events ***must be clean*** to maximize reliability. Furthermore, the threshold voltage of low $R_{DS(on)}$, low voltage Si MOSFETs is typically low, often less than 2 V at room temperature. The counter argument supporting zero V_{SS} is the absence of dv/dt induced switch-on (a.k.a. parasitic turn-on) because it is not a half-bridge circuit.

Except for R_ODV, gate resistance should be next to each gate to maximize damping of ringing. This is especially important when paralleling. Also, avoid connecting gates directly together when paralleling. This applies to both the MOSFETs and the JFETs.

Snubber

A semiconductor circuit breaker may require a snubber and metal oxide varistors (MOV) or transient voltage suppressors (TVS) connected across the AC power terminals to absorb energy in electric wires and cables. The snubber has multiple functions. First, it allows time for MOVs to activate, which typically require 10 to 20 ns. Second, it provides damping that quenches ringing in both drain and gate voltages. Finally, when the JFETs are off and blocking high voltage, their output capacitance is low, so drain voltage is more susceptible to noise. A snubber absorbs such system noise coming in through the wires to the breaker or relay.

In back-to-back configurations, a snubber can be connected across the power terminals, or from each power terminal to the common source point. A recommended snubber capacitance per JFET is at least 5x the JFET output capacitance at operating voltage. The corresponding snubber resistance connected in series with the snubber capacitor is 5 to 10 Ohms. When paralleling, JFETs or Combo JFETs can share snubbers. See the FET User Guide for information about recommended snubber components.

Kelvin-Source Pin

When using separate JFETs and MOSFETs, the JFET Kelvin-source terminals must not connect to the common pin (if any) of the gate driver nor to the gate driver power supply common point because this would create a short across the MOSFETs. This situation exists with any common source cascode configuration, including the quasi-cascode in Figure 7 and direct drive in Figures 5 and 6. When driving a JFET without a series MOSFET, the Kelvin source can and should be connected to the gate driver common pin (if any, as in Figure 4) and to the gate drive power supply common point. Finally, the Kelvin-source pin of the JFET should not be directly shorted to the other source pin(s) because it has a smaller diameter bond wire connection to source inside the package. This bond wire is not intended for the high load currents that the other source pin(s) carry. If you want to avoid a floating pin, you can connect the Kelvin-source pin to the source pin(s) with either a large value resistor or a small capacitor.

On-Chip Temperature Sensing

As mentioned before, the JFET gate-source PN junction forward voltage decreases linearly with increasing temperature. See Figure 2(b). It is therefore possible to sense the temperature of the JFET chip by measuring V_{GS} while overdriving the JFET gate. There are some obvious advantages to this:

- It senses the temperature across the chip itself, so it is highly accurate.
- Response is quick.
- Readily available off-the-shelf components are all that is needed.
- Very little space is required.

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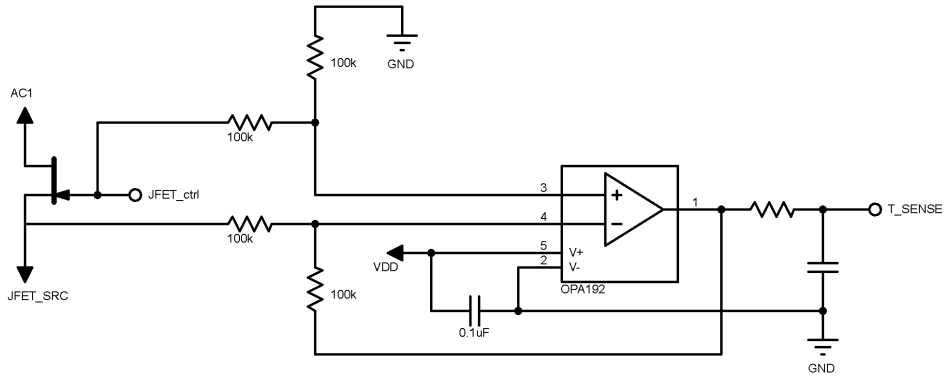

Figure 8. Simple Differential Amplifier Temperature Sense Circuit

The simple differential amplifier (diff-amp) circuit shown in Figure 8 senses the JFET temperature. It has unity gain and an output voltage range of 1.80 to 2.56 V corresponding to a temperature range of 175 down to −55 °C for the UJ4N075004L8S JFET. The problem is that the voltage swing is only about 0.76 V over the entire temperature range. With a 100 °C change in temperature, the voltage at the analog to digital converter (ADC) changes only 0.33 V. A typical ADC has an input voltage range of 3 or 3.3 V. Using such a small portion of the ADC input voltage range causes noise susceptibility and requires heavy filtering. It would be good to amplify the signal to the ADC, but with the signal already close to the maximum ADC input voltage, the gain must be very limited.

Subtracting V_{GS} from a reference voltage would allow amplification. The question however is where to reference this voltage. The JFET source is the ideal place, but with the JFET connected in series with a MOSFET, the JFET source potential changes with respect to the common source point, which is where all other circuitry is referenced to. It could be possible to work around this, but there is another simple, elegant solution.

Figure 9 shows two diff-amps, each measuring a JFET to MOSFET source voltage. A single reference voltage attaches to the common source point, from which each V_{GS} is subtracted by the diff-amps. Imagine that the MOSFETs and JFETs are switched on and current flows from AC1 to AC2, as indicated in Figure 9. The current creates a voltage drop across each MOSFET. The output of each diff-amp is:

$$T_{sense1} = \frac{R_2}{R_1} \cdot \left[V_{ref} - \left(V_{GS,JFET} + V_{DS,}MOSFET\right)\right], \text{ and}$$

$$T_{sense2} = \frac{R_2}{R_1} \cdot \left[V_{ref} - \left(V_{GS,JFET} - V_{DS,}MOSFET\right)\right]$$

Assuming equal voltage drop across the MOSFETs, which is reasonable, when we add Tsense1 and Tsense2, the MOSFET voltage drops cancel out. Then dividing by 2 results in the amplified average JFET V_{GS}.

$$T_{sense,ave} = \frac{T_{sense1} + T_{sense2}}{2} = \frac{R_2}{R_1} \cdot \left(V_{ref} - V_{GS,JFET,ave}\right)$$

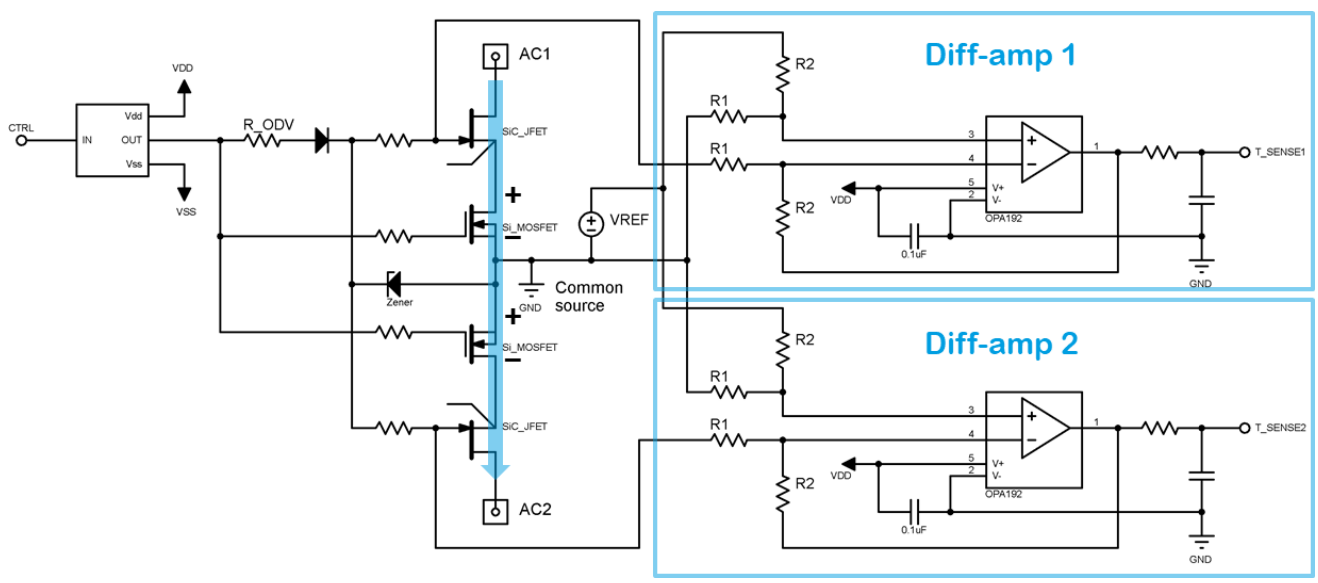

Figure 9. Recommended Temperature Sense Circuit

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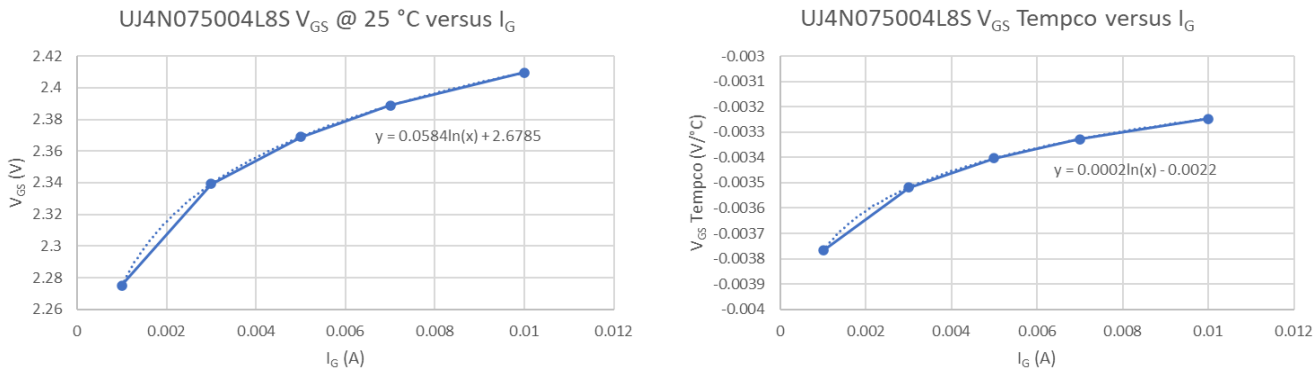
With each R1 of equal value, and likewise R2, then the gain is the ratio $\frac{R2}{R1}$. By setting V_{REF} close to the nominal V_{GS}, the gain can be much higher. For example, again using UJ4N075004L8S, with V_{REF} = 2.5 V, $I_G \approx$ 5 mA, and a gain of 5, V_{ADC} = 0.29 V at 25 °C, and the ADC voltage range over 0 to 175 °C temperature range is 2.98 V, which is very easy to process. The minimum measurable temperature would be −17 °C with V_{ADC} = 0 V.

About 1 mA gate current is sufficient to reduce the on−resistance, and while it is possible to sense the temperature with such a low gate current, there is less noise susceptibility with 5 to 10 mA gate current. Higher gate current corresponds to a higher I_G versus V_{GS} slope, see Figure 2(b). Therefore, V_{GS} varies less with any change (noise) in I_G.



(a) (b)

Figure 10. For UJ4N075004L8S: (a) V_{GS} versus I_G at 25 °C, and (b) V_{GS} Temperature Coefficient versus I_G

Figure 10(a) shows a curve fit version V_{GS} versus I_G in the mA range at 25 °C for UJ4N075004L8S, and (b) shows the V_{GS} temperature coefficient versus I_G. A subtle but important point must be made here. There is a curve fitting error associated with Figure 10, which we will call the nominal error. Also, when driving the gate through a resistor instead of with a constant current source, as in the previous example circuits, there is variation in I_G due to the temperature-related change in V_{GS}. This change in I_G is greater the closer the positive drive voltage is to V_{GS}. For example, the change in I_G is greater with a V_{DD} = 5 V compared to 15 V. This change in I_G causes a corresponding change in the T_J measurement.

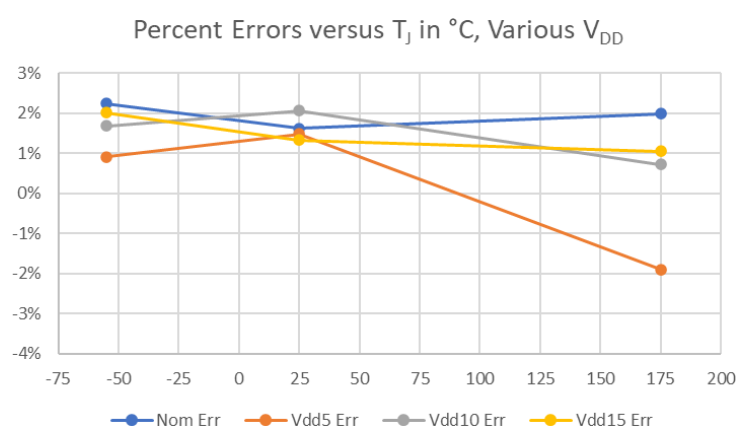


Figure 11. Nominal and V_{DD} / R_ODV Errors for UJ4N075004L8S versus T_J

Figure 11 shows the nominal (curve fit) error, and errors for V_{DD} = 5, 10, and 15 V with standard precision resistors values used to set I_G as close as possible to 5 mA at 25 °C. The change in T_J at V_{DD} = 10 or 15 V is noticeably smaller versus V_{DD} = 5 V, however, all errors are reasonably small.

JFET as Current Sensor

Now that we know the JFET chip temperature, we know the $R_{DS(on)}$, at least its typical value, unless we calibrate it. Therefore, we can sense the drain-source current by measuring the JFET V_{DS}.

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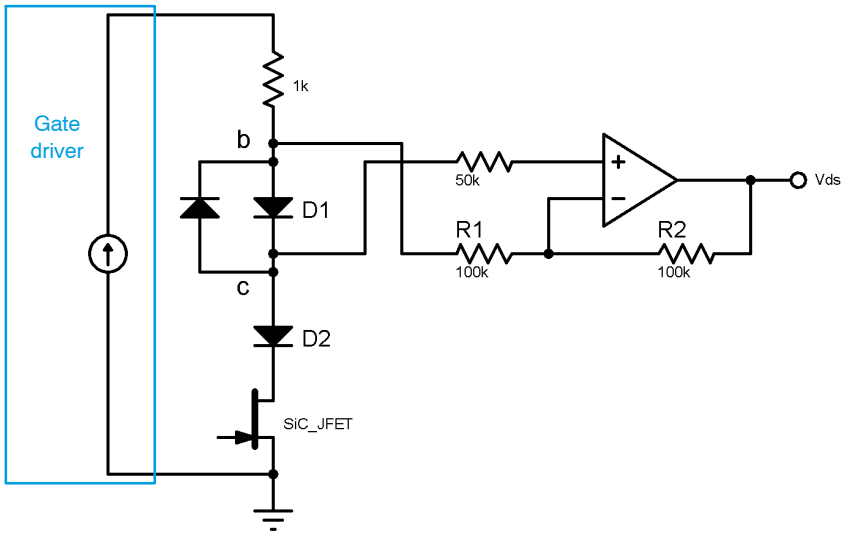

Figure 12. Recommended V_{DS} Sense Circuit Using Gate Driver with DESAT Function

Figure 12 shows a constant current source that is inside a DESAT sensing gate driver, and all remaining components are not part of the gate driver. Any IGBT gate driver works fine for this circuit. Diode D2 blocks high voltage when the JFET is off. D1 is used as part of the V_{DS} measurement, as will be explained. It has an anti-parallel diode to prevent high voltage from developing across it. Pro tip: D1 and D2 can each be implemented as two series diodes to spread out the high voltage that D2 must block, but for simplicity, they are shown as single diodes in Figure 12.

We want to implement $V_{DS} = V_c - V_{F,D2}$. The key here is the reasonable assumption that the V_F of diodes D1 and D2 are equal, and therefore we subtract the V_F of D1 (which is $V_b - V_c$) instead of the V_F of D2 because D2 blocks high voltage. Thus, $V_{DS} = V_c - V_{F,D1} = V_c - (V_b - V_c)$. Rearranging and adding $\frac{R_2}{R_1}$ where $R_1 = R_2$: $V_{DS} = V_c + \frac{R_2}{R_1} \cdot (V_c - V_b)$ This is implemented with a non-inverting op-amp circuit as shown in Figure 12. You can easily prove this by writing and rearranging the node equations with the output of the amplifier denoted as V_{out}.

$$\frac{V_- - V_{out}}{R_2} = \frac{V_+ - V_{out}}{R_2} = \frac{V_c - V_{out}}{R_2} = \frac{V_b - V_-}{R_1} = \frac{V_b - V_c}{R_1}, \text{ so } \frac{V_c - V_{out}}{R_2} = \frac{V_b - V_c}{R_1}.$$

With $R_1 = R_2$, this becomes $V_c - V_{out} = V_b - V_c$, and finally $V_{out} = 2 \cdot V_c - V_b$, which as before, equals V_{DS}. This signal is then amplified before routing to an ADC for processing.

Adding D1 enables this simple measurement technique. Note that it compensates for the temperature effects of D2 because it is the same type of diode mounted thermally close to D2. It also reduces the DESAT trip voltage (if used), which could be desirable anyway.

As with the temperature sensing, it might be impractical to directly measure the JFET V_{DS}, but measuring the voltage from each JFET drain to MOSFET source (common source point) is possible. In this case, the temperature-dependent $R_{DS(on)}$ of the MOSFET simply adds to that of the JFET if they are installed thermally close to each other.

What a simple and elegant solution this is, using the JFET itself as both temperature and current sensor, and implementing these functions with simple op-amp circuits.

Paralleling

There are three concerns when paralleling any power semiconductor:

- Parasitic oscillation
- Static current sharing
- Dynamic current sharing

When paralleling **onsemi** SiC JFETs, parasitic oscillation would only be a concern if each gate resistance is close to zero. With all the output capacitance between the drain and gate ($C_{oss} = C_{rss}$), the **onsemi** SiC JFET switching speed is easily controlled by adjusting the gate resistance. The tradeoff is higher gate charge, and the design and layout of the gate drive loop is critically important.

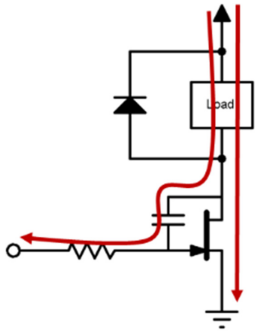

Figure 13. onsemi SiC JFET Showing Output Capacitance Switching Off with a Clamped Inductive Load

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Figure 13 shows a **onsemi** SiC JFET switching off with a clamped inductive load. As the JFET switches and its V_{DS} changes, current diverts from the JFET channel and flows through the drain-gate capacitance, gate resistor, and the gate driver (not shown). All charge to/from the output capacitance is supplied/removed by the gate driver through the gate resistor, and practically none by the load current. This results in excellent switching speed control by simply adjusting the gate resistance, and there is maximum damping of ringing that could otherwise initiate parasitic oscillation. To cancel source inductance that can cause gate ringing, it is recommended to add a gate-source capacitor, with a value about three times the C_{rss} value measured at operating voltage, although more capacitance is okay.

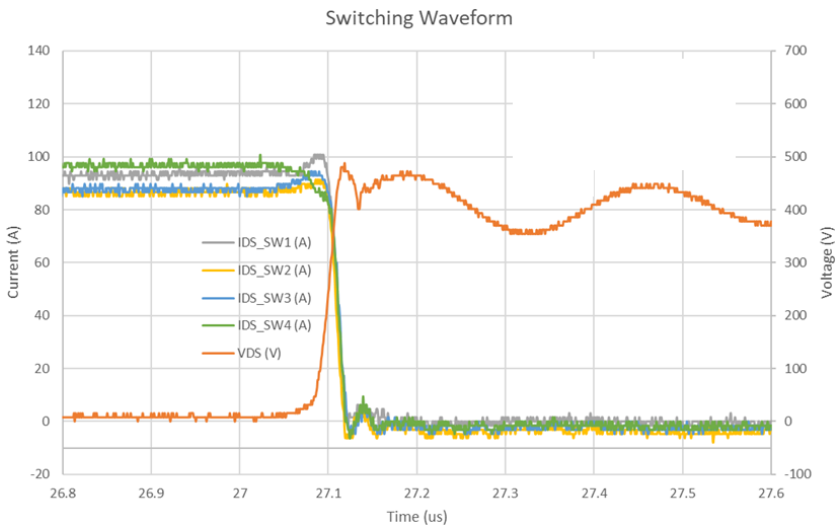

Figure 14. Four Parallel 750 V, 9 mΩ JFETs Switching Off a Clamped Inductive Load, R_G = 3.3 Ω, $V_{GG,off}$ = −25 V

Static current sharing is good because of the inherently narrow $R_{DS(on)}$ distribution of **onsemi** SiC JFETs, but some static current mismatch is to be expected. Figure 14 shows the switching waveforms of four parallel 750 V, 9 mΩ SiC JFETs, each conducting and then switching off an average of 90 A. The current sharing range is about ±7%. A safe margin for paralleling is to add 20% to the required total current.

As can be seen in Figure 14, dynamic current sharing is excellent, with some initial mismatch in current due to threshold voltage differences, but all JFETs switching off the bulk of the current together. With symmetrical power layout, dynamic current mismatch is not a concern.

Maximum Energy and Gate Bias Recommendations

If a circuit breaker or relay switches off a high current, it is desirable for the JFETs to safely absorb as much energy as possible, with the rest going into a snubber and MOVs or TVS. The circuit is effectively unclamped inductive switching (UIS) with inductance from the wires to/from the breaker or relay. Although **onsemi** JFETs and Combo JFETs are 100% avalanche tested, it is best to avoid avalanche. Part-to-part variation in avalanche voltage causes poor avalanche current sharing when paralleling. Current sharing during switching (without avalanching) is much better. It is therefore recommended to set the switch off speed with the JFET gate resistance such that each JFET absorbs a safe amount of energy. The table below shows the recommended maximum switching energy by part number. Please note that there is a significant safety margin in these values but exceeding them should be done only after verification testing.

Table 1. MAXIMUM SWITCHING ENERGY AND BIAS CURRENT RECOMMENDATIONS BY PART NUMBER

Part Number	Max. Eswitch (J)	Min. I_G Bias (mA)	Typical I_G Bias (mA)
UJ3N065025K3S	0.2	0.44	2.2
UJ3N065080K3S	0.065	0.14	0.72
UJ4N075004L8S	0.45	1	5
UG4SC075005L8S			
UJ4N075005K4S			
UG4SC075006K4S			
UG4SC075009K4S	0.23	0.51	2.56
UG4SC075011K4S	0.19	0.43	2.15
UF3N120007K4S	.71	0.5	2.5
UG3SC120009K4S			
UJ3N120035K3S	0.16	0.11	0.57
UJ3N120065K3S	0.092	0.06	0.32
UJ3N120070K3S	0.092	0.06	0.32
UF3N170400B7S	0.03	0.02	0.11

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Summary

- The **onsemi** SiC JFET's very low R_{DS}·A make it especially attractive for SCB and relay applications.
- Adjusting the gate resistance is very effective for controlling the switching speed, and it also facilitates paralleling.
- The quasi-cascode and direct drive circuits allows overdriving the JFET gate for minimal conduction loss while maintaining a normally off state, all with readily available components.
- A snubber is highly recommended.
- A Kelvin-source connection cannot be used in cascode configurations.
- The JFET itself can act as both temperature and current sensor with simple op-amp circuitry.

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