



Self-Service **plecs** Model Generator (SSPMG)

User Guide

Outline of User Guide

1

Introduction to Self-Service PLECS Model Generator:
What is it and What are the benefits

2

Step by Step Tool Flow

3

Deploying PLECS Models in Elite Power Simulator and
PLECS Stand Alone

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PLECS Basics

- PLECS is a system level simulator that facilitates the modeling and simulation of complete systems with optimized device models for maximum speed and accuracy. PLECS is not a SPICE-based circuit simulator, where the focus is on low-level behavior of circuit components .
- Power transistors are treated as simple switches that can be easily configured to demonstrate losses associated with conduction and switching transitions.
- The PLECS models, referred to as “thermal models”, are composed of lookup tables for conduction and switching losses, along with a thermal chain in the form of a Cauer or Foster equivalent network.
- During simulation, PLECS interpolates and/or extrapolates using the loss tables to get the bias point conduction and switching losses for the circuit operation. Access the onsemi Elite Power Simulator powered by 

www.onsemi.com/elite-power-simulator

onsemi's State-of-the-Art PLECS Models:

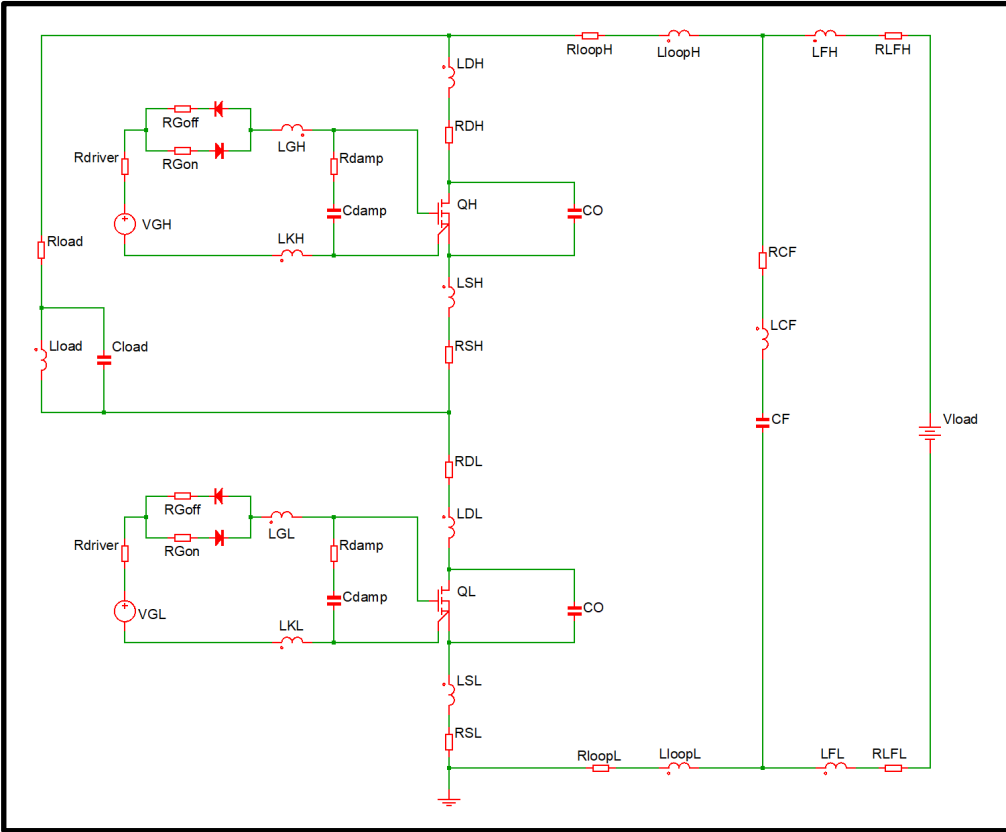
- Typical industry PLECS models are composed of measurement based loss tables that are consistent with datasheets provided by the manufacturer.

There are four major problems with this approach:

1. The switching energy loss data is dependent on the parasitics of the measurements set ups and circuits.
 2. The conduction and switching energy loss data is limited and thus is often not dense enough to ensure accurate interpolation and minimal extrapolation by PLECS.
 3. The loss data is based on nominal semiconductor process conditions only.
 4. The switching energy loss data comes from datasheet double pulse generated loss data. This means the PLECS models are only valid for hard switching topology simulation. The models are highly inaccurate if used in soft switching topology simulation.
- onsemi's Self-Service PLECS Model Generator (SSPMG) provides solutions to all four problems.
 - Ultimate power is delivered to the user to build PLECS models tailored for the user's application. Unleash the power here: www.onsemi.com/self-plecs-generator

Measurement Parasitics Influence on Switching Performance

Switching Schematic with Parasitics



Example Datasheet

Parameter	Switching Loss
Eon [uJ]	490
Eoff [uJ]	221
Ettotal [uJ]	711



Customer Application

Parameter	Switching Loss
Eon [uJ]	415
Eoff [uJ]	231
Ettotal [uJ]	646

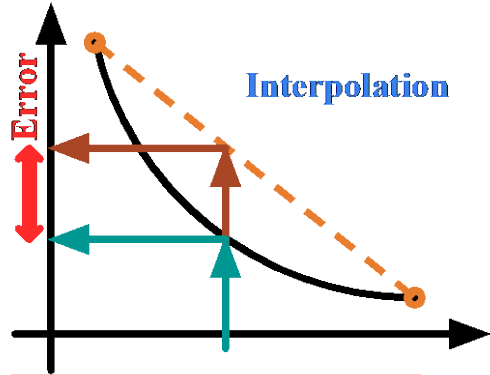
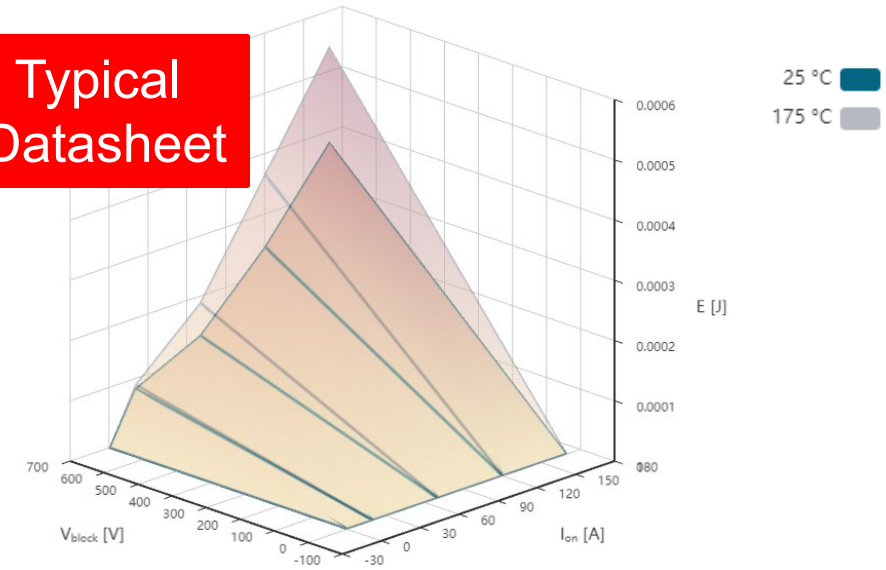
- Crucial to understand that the lab test circuit's passives, parasitics, gate driver performance, etc. all affect losses.
- Where does this leave the user for a PLECS model? The user application will surely have a different environment than any of the component supplier's lab and board setups.



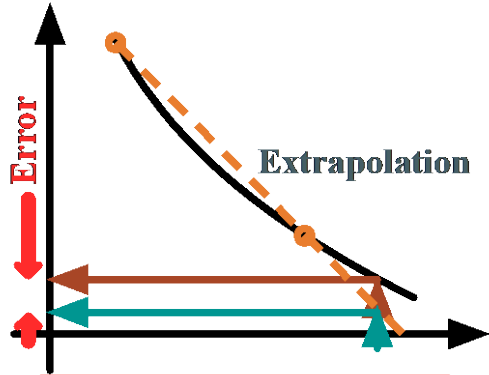
Loss Table Density and Limits Influence Results

- Datasheet data is often not dense enough to ensure accurate interpolation by PLECS in nonlinear environments.
- Datasheet data limits often do not bound the entire operating range causing highly inaccurate extrapolation by PLECS.

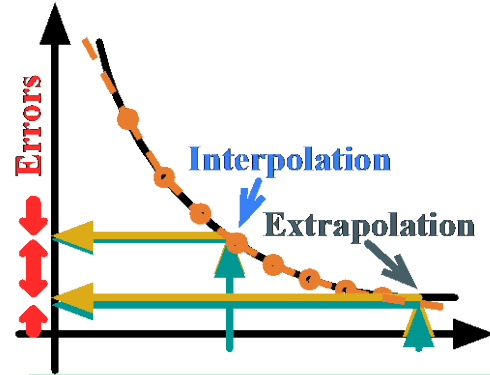
Typical Datasheet



Interpolation with small data set

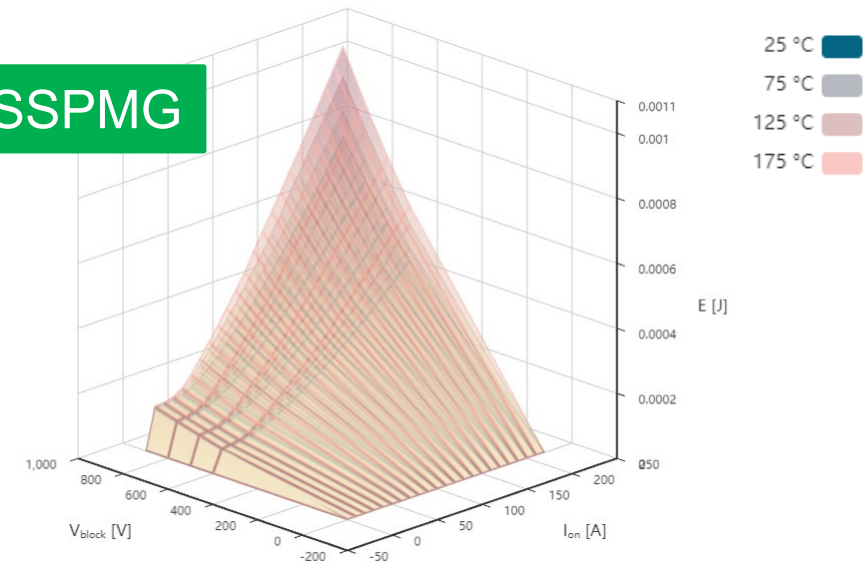


Extrapolation with small data set



Interpolation & Extrapolation with large data set

SSPMG



Corner PLECS Models

- Conventional PLECS models based on measurements are only valid for the typical or nominal process case in manufacturing. onsemi has developed accurate corner PLECS models based on real manufacturing distribution.
- Physics dictates that worst case conduction and switching losses do not happen simultaneously for example.
- Depending on the application, the influence of conduction and switching energy losses on the overall system performance will vary. The onsemi corner PLECS models provide the user the flexibility to investigate the entire correlated space.
- Corner models currently only available for EliteSiC products. FS7 IGBT corner models are coming soon.
- Accurate corner and statistical modeling covered in detail in
 - SiC MOSFET Corner and Statistical SPICE Model Generation – Proceeding of International Symposium on Power Semiconductor Devices and ICs (ISPSD), pp. 154-147, September 2020

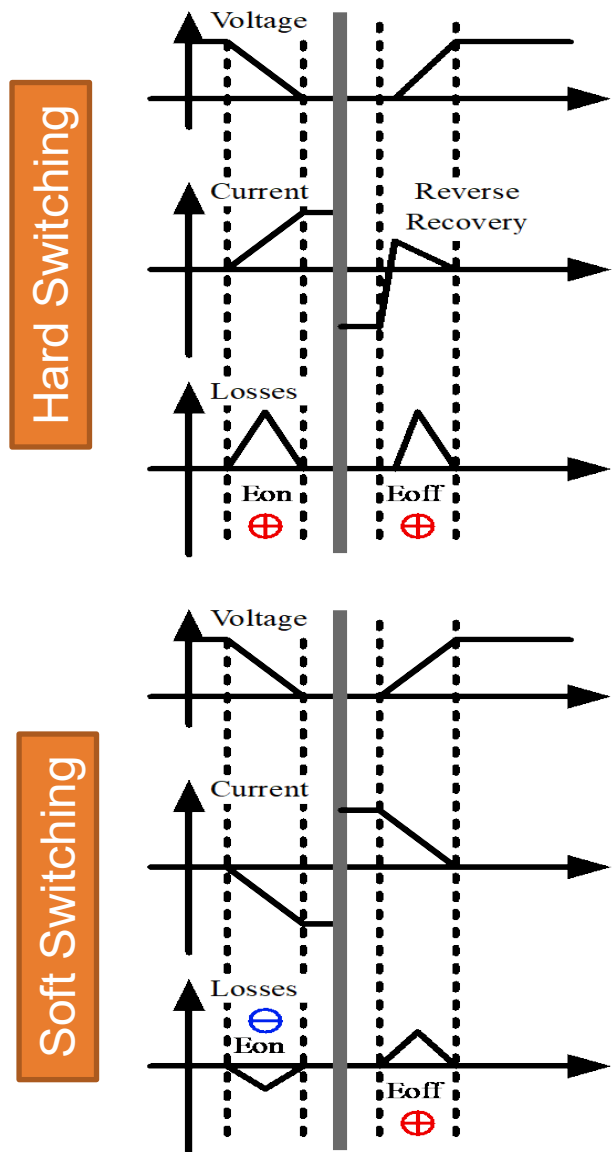
Process Condition	R_{DSon} , V_{th} , BV	Capacitance, Device RG	Conduction Loss	Switching Energy Loss
Nominal	Nominal	Nominal	Nominal	Nominal
Best Case Conduction Loss, Worst Case Switching Loss	Low	High	Low	High
Worst Case Conduction Loss, Best Case Switching Loss	High	Low	High	Low

Soft Switching Energy Losses

Soft Switching Simulation*

onsemi provides **industry first** PLECS models valid for soft switching simulation of applications such as DC-DC LLC and CLLC Resonant, Dual Active Bridge, and Phase Shifted Full Bridge.

The Double Pulse Test is **NOT** representative of Soft Switching. Using double pulse switching energy losses in the simulation of a Soft Switching Topology is highly inaccurate.



Access SSPMG with MYON Account

MyON is required to use the SSPMG

MYON Login

The screenshot shows the onsemi website header with navigation menus (Products, Solutions, Design, Support, Company, Careers) and a search bar. A user profile icon in the top right is highlighted with an orange box. Below the header, a dark blue banner promotes account creation with the text "Supercharge your onsemi experience by creating an onsemi account". To the right, a white login modal is displayed, featuring a "Login" header, a "Returning User" label above an email input field, a password input field with a visibility toggle, a "Forgot Password?" link, an orange "Login" button, and a "Register Now" link for "First Time User". A "Do not have an account?" label is positioned to the left of the "Register Now" link. An orange arrow points from the user profile icon to the "Returning User" label. The bottom of the page features a dark grey navigation bar with links for "Upcoming Tradeshow", "PRT+ Interactive Charts", "Technology Webinars", and "New SiC Technology".

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Getting Started

Go to landing page
www.onsemi.com/self-plecs-generator
and select Generate Model

Generate Model

Link to Elite Power Simulator

onsemi Self-Service PLECS Model Generator

Home

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Support

1 Product Selection

2 Process Condition

3 Switching Type

4 Characteristics

5 Circuit Schematic



Select Your Preferred Product


Filter by selecting product type, technology, and voltage

User Guide and
Detailed Application Note

Step 1: Select Product

Home Requests User Guide Application Note Elite Power Simulator Support

1 Product Selection 2 Process Condition 3 Switching Type 4 Characteristics 5 Circuit Schematic

 **Select Your Preferred Product**
Filter by selecting product type, technology, and voltage

Product Type* Discrete	Discrete or Module
Product Technology M3 (SiC MOSFETs)	Device Type* & Technology Generation
Product Voltage 1200V	Blocking Voltage
Product* NTH4L022N120M3S	Product list filtered based on previous choices

*EliteSiC MOSFETs and Field Stop 7 (FS7) IGBTs are supported.

Next Step

Step 2: Set Process Condition

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Support

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2 Process Condition

3 Switching Type

4 Characteristics

5 Circuit Schematic



Preferred Process Condition

What is your preferred process condition?

Process Condition

Nominal

Corner models currently only available for EliteSiC products. FS7 IGBT corner models are coming soon.

Previous Step

Reset

Next Step

Process Condition	R_{Dson} , V_{th} , BV	Capacitance, Device RG	Conduction Loss	Switching Energy Loss
Nominal	Nominal	Nominal	Nominal	Nominal
Best Case Conduction Loss, Worst Case Switching Loss	Low	High	Low	High
Worst Case Conduction Loss, Best Case Switching Loss	High	Low	High	Low

Step 3: Set Switching Type

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Switching Type

What is your preferred switching type?

Switching Type

Hard

Hard or Soft

High Side Choice *

NTH4L022N120M3S

Option for half bridge or quarter bridge with ideal diode or EliteSiC Schottky diode

[Previous Step](#)[Reset](#)[Next Step](#)

- Choose the switching type based on the intended application or topology.
- If hard switching chosen, user has choice for high side device to be in half bridge configuration or quarter bridge with ideal diode or EliteSiC Schottky diode on the high side.
- Example Soft Switching Topologies include DC-DC LLC and CLLC Resonant, Dual Active Bridge, and Phase Shifted Full Bridge.
- Subsequent step 4 “Characteristics” change slightly based on the Switching Type.

Step 3: Quarter Bridge with EliteSiC Schottky Diode

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Switching Type

What is your preferred switching type?

Switching Type *
Hard

High Side Choice *
SiC Diode

Technology (SiC Diode)
D3

Technology Generation

Voltage (SiC Diode)
1200V

Blocking Voltage

Product (SiC Diode) *
NDSH50120C

Product list filtered based on previous choices

[Previous Step](#)[Reset](#)[Next Step](#)

- User should make sure EliteSiC Schottky diode current rating is suitable to switch with the low side EliteSiC MOSFET.

Step 4: Set Characteristics (Hard Switching)

- Drain current can be in 1st and/or 3rd quadrant, so positive and/or negative.
- Diode Current is for diode forward conduction mode. Values are given in absolute scale.
- If $(\text{Stop}-\text{Start})/(\text{Step Size}) \neq \text{Integer}$

Then the last point=Stop. Example:

Start=1 Stop=9 Step Size=3

Simulated points are: 1 4 7 9

- Gate drive High VGS must be $\geq 10\text{V}$ for SiC MOSFETs/IGBTs to ensure current carrying capability
- Gate drive Low VGS must be ≤ 0 to ensure full device turn off.

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Characteristics
All fields in this step are required!

Descriptive fields guide user.

Gate Drive

Low VGS (V)
Value * (<= -3)
-3

High VGS (V)
Value * (>= 12)
18

Conduction Characteristics

Transistor Current (A)
Start *
-50

Stop * (> Start)
50

Step Size *
5

Diode Current (A)
Start * (>= 0)
0

Stop * (> Start)
50

Step Size *
5

Switching Characteristics

Current (A)
Start * (> 0)
5

Stop * (> Start)
50

Step Size *
5

Load Voltage (V)
List of values separated by space *
600 750 900

Temperature(°C)
Fill in list of values, separated by space *
25 75 125 175

Previous Step Reset Next Step

Step 4: Set Characteristics (Soft Switching)

- Soft Switching Changes:
 - Drain current can be in 1st and/or 3rd quadrant, so positive and/or negative when a switching event happens
- Soft Switching Additions:
 - **di/dt**: in the resonant inductor when the switching event happens. This di/dt is directly linked to the resonant inductor voltage by the Faraday's law of induction $E=L*di/dt$. "di/dt" is a PLECS circuit parameter passed into the PLECS model to evaluate the losses in soft switching.
 - **Max Delay**: maximum dead time allowed between high side and low side switches for the resonant transition to occur
 - **Resonant Inductor**

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1 Product Selection 2 Process Condition 3 Switching Type 4 Characteristics 5 Circuit Schematic

Characteristics

All fields in this step are required!

Gate Drive

Low VGS (V)
Value * (<= -3)
-3

High VGS (V)
Value * (>= 12)
18

Conduction Characteristics

Transistor Current (A)
Start *
-20

Stop * (> Start)
20

Step Size *
1

Diode Current (A)
Start * (>= 0)
0

Stop * (> Start)
20

Step Size *
1

Switching Characteristics

Current (A)
Start * (< 0)
-20

Stop * (> Start)
20

Step Size *
1

di/dt (A/μs)
Start *
-10

Stop * (> Start)
10

Step Size *
2

Max Delay (ns)
250

Resonant Inductor (μH)
50

Load Voltage (V)
List of values separated by space *
400 800


Temperature (°C)
Fill in list of values, separated by space *
25 100 175

Previous Step Reset Next Step

Step 5: Circuit Schematic (Half Bridge Discrete)

- Table of parameters matches circuit schematic.
- Default parameters are generally 0, allowing user to just enter needed values.
- Min and Max Gate Resistance parameter facilitate RG scaling in the PLECS model.
- Gate drive signal can be modeled through Rdriver, TF, and TR.

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Switching Circuit Schematic
Please fill in circuit parameters

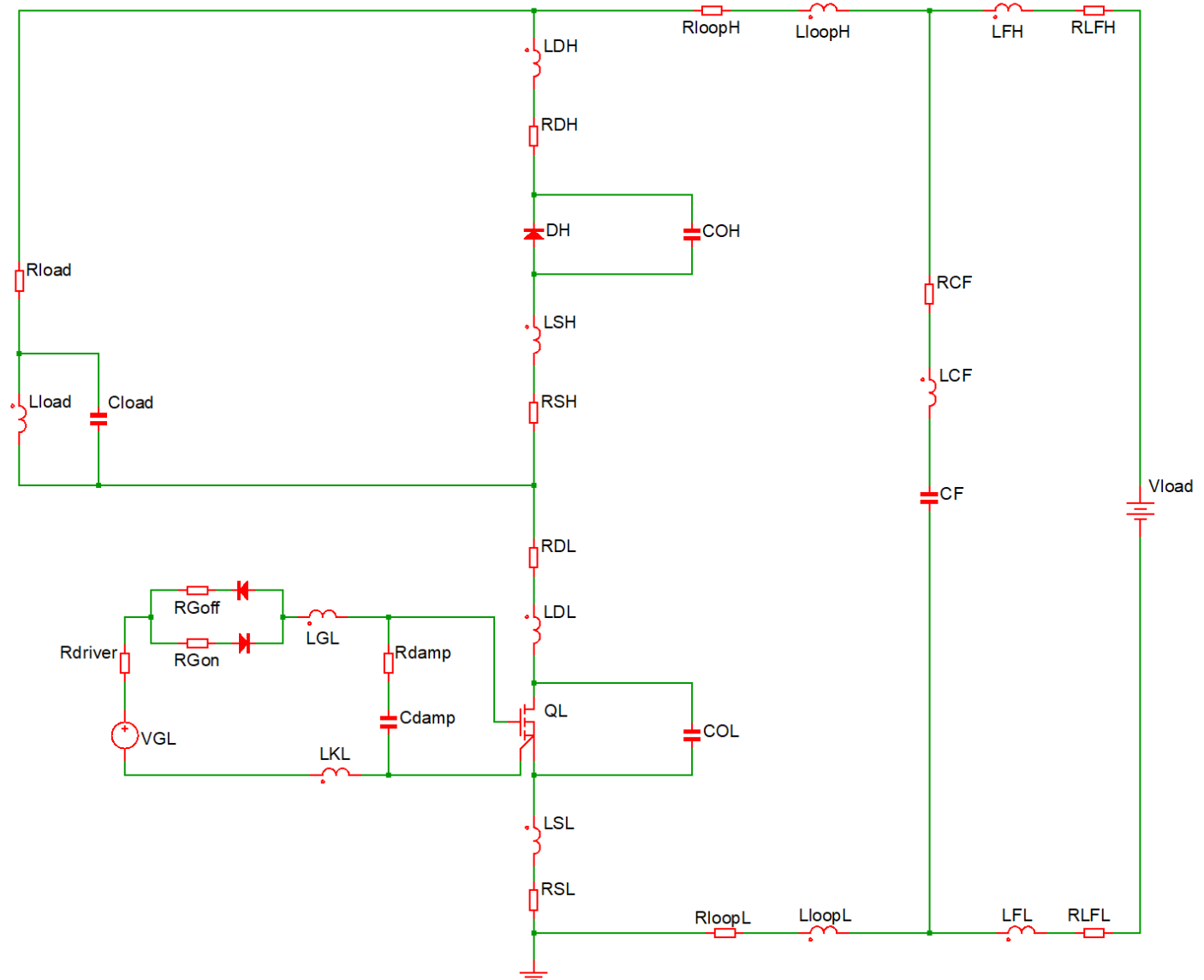
Descriptive fields guide user

Category	Parameters
Gate Driver	
Rdriver (Gate driver internal resistance, Ω)	<input type="text" value="1"/>
TR (Gate driver rise time, s)	<input type="text" value="50n"/>
TF (Gate driver fall time, s)	<input type="text" value="50n"/>
Gate Drive Circuit	
EMI Damping	
Load Inductor Parasitics	
Rload (Ω)	<input type="text" value="80m"/>
Cload (F)	<input type="text" value="50p"/>
Devices Layout Parasitics	
Switching Loop Parasitics	
RloopH (Ω)	<input type="text" value="0"/>
LloopH (H)	<input type="text" value="16n"/>
RloopL (Ω)	<input type="text" value="0"/>
LloopL (H)	<input type="text" value="0"/>
RDC (Ω)	<input type="text" value="0"/>
LDC (H)	<input type="text" value="0"/>
Input Filter	
Current Measurement	

Previous Step
Reset
Submit Request

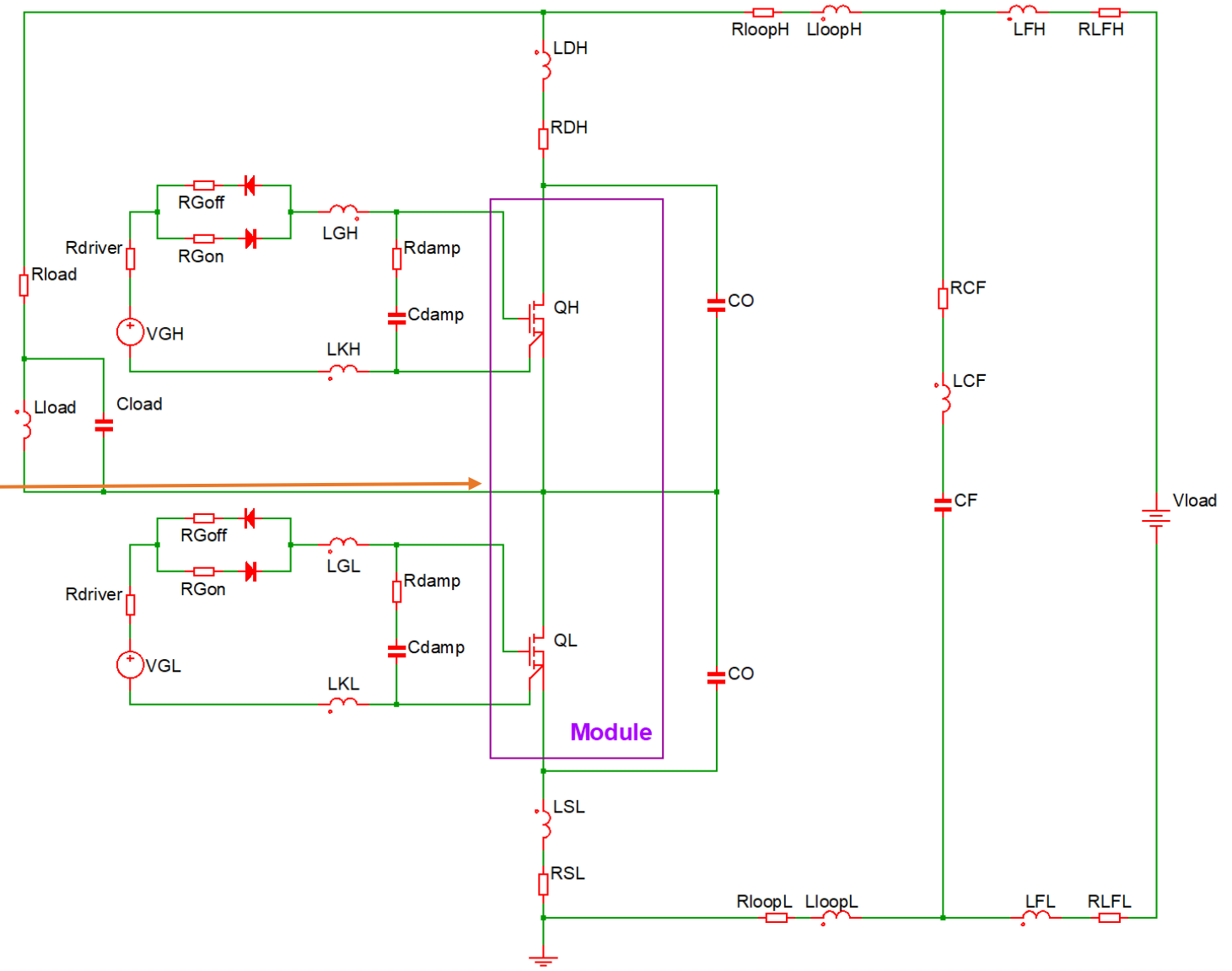
Step 5: Circuit Schematic (Quarter Bridge Discrete)

- High side choice can be:
 - Ideal diode with capacitance=0
 - EliteSiC Schottky diode
- Parasitic output capacitor is split into high side (COH) and low side (COL).



Step 5: Circuit Schematic (Half Bridge Module)

- All module parasitics are included in power module SPICE model.
- Remaining parameters are the same as discrete version.



Step 5: Circuit Parameters – Full list

Input Filter	
RCF (Ω)	0.2m
LCF (H)	2n
CF (F)	3n
LFH (H)	5n
RLFH (Ω)	0.1m
LFL (H)	5n
RLFL (Ω)	0.1m

Switching Loop Parasitics	
RloopH (Ω)	0.1m
LloopH (H)	2n
RloopL (Ω)	0.1m
LloopL (H)	2n

Gate Drive Circuit	
RGoff (Default OFF Gate Resistance, Ω)	2
RGon (Default ON Gate Resistance, Ω)	2
RGoffMIN (Min OFF Gate Resistance, Ω)	2
RGoffMAX (Max OFF Gate Resistance, Ω)	10
RGonMIN (Min ON Gate Resistance, Ω)	2
RGonMAX (Max ON Gate Resistance, Ω)	10
LGH (H)	5n
LKH (H)	5n
LGL (H)	5n
LKL (H)	5n

Load Inductor Parasitics	
Rload (Ω)	5m
Cload (F)	22p

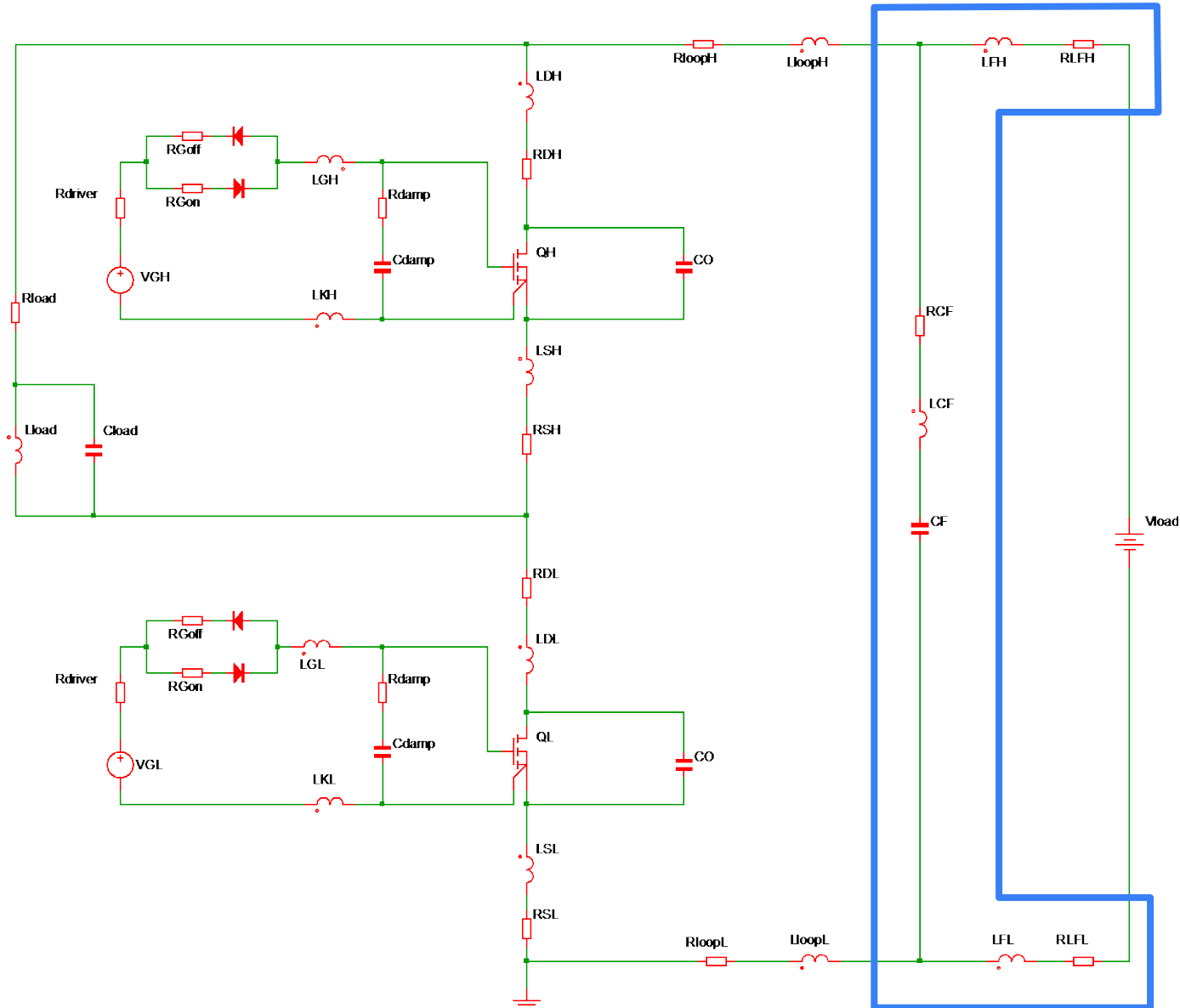
Devices Layout Parasitics	
LDH (H)	2n
RDH (H)	0.1m
LSH (H)	2n
RSH (Ω)	0.1m
RDL (Ω)	0.1m
LDL (H)	2n
LSL (H)	2n
RSL (Ω)	0.1m

EMI Damping	
Rdamp (Ω)	100
Cdamp (F)	100p
CO (F)	47p

Gate Driver	
Rdriver (Gate driver internal resistance, Ω)	1
TR (Gate drive rise time, s)	50n
TF (Gate drive fall time, s)	50n

Current Measurement	
Rshunt (Ω)	1m
Rshunt Location	RSL

Step 5 : Input Filter Parameters

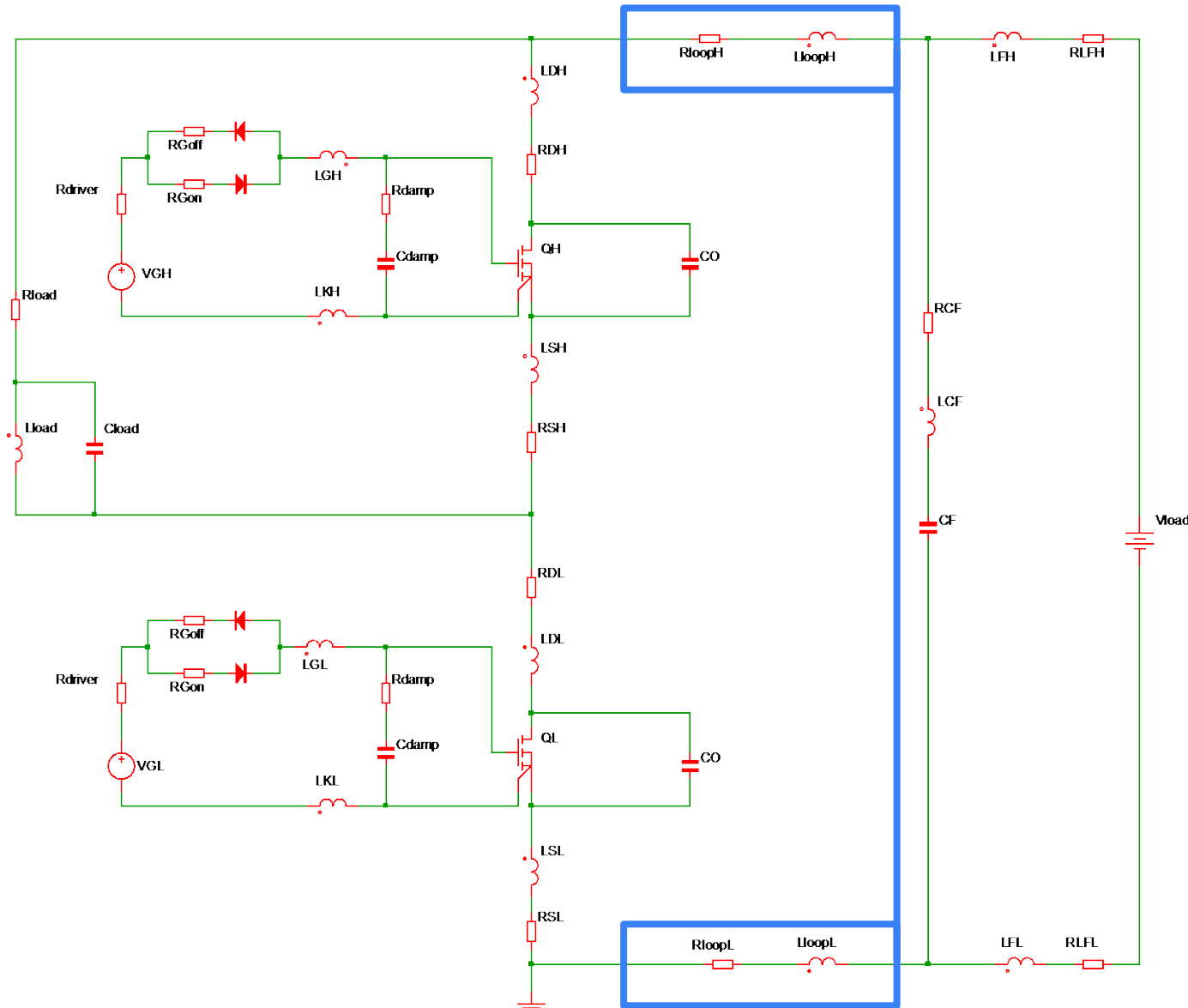


Input Filter	
RCF (Ω)	0.2m
LCF (H)	2n
CF (F)	3n
LFH (H)	5n
RLFH (Ω)	0.1m
LFL (H)	5n
RLFL (Ω)	0.1m

LFx (with RLFx as series resistance) is the PCB leakage inductance or a discrete filtering inductor.

The filter capacitor or decoupling capacitor CF includes ESL and ESR parameters.

Step 5 : Switching Loop Leakage Inductances

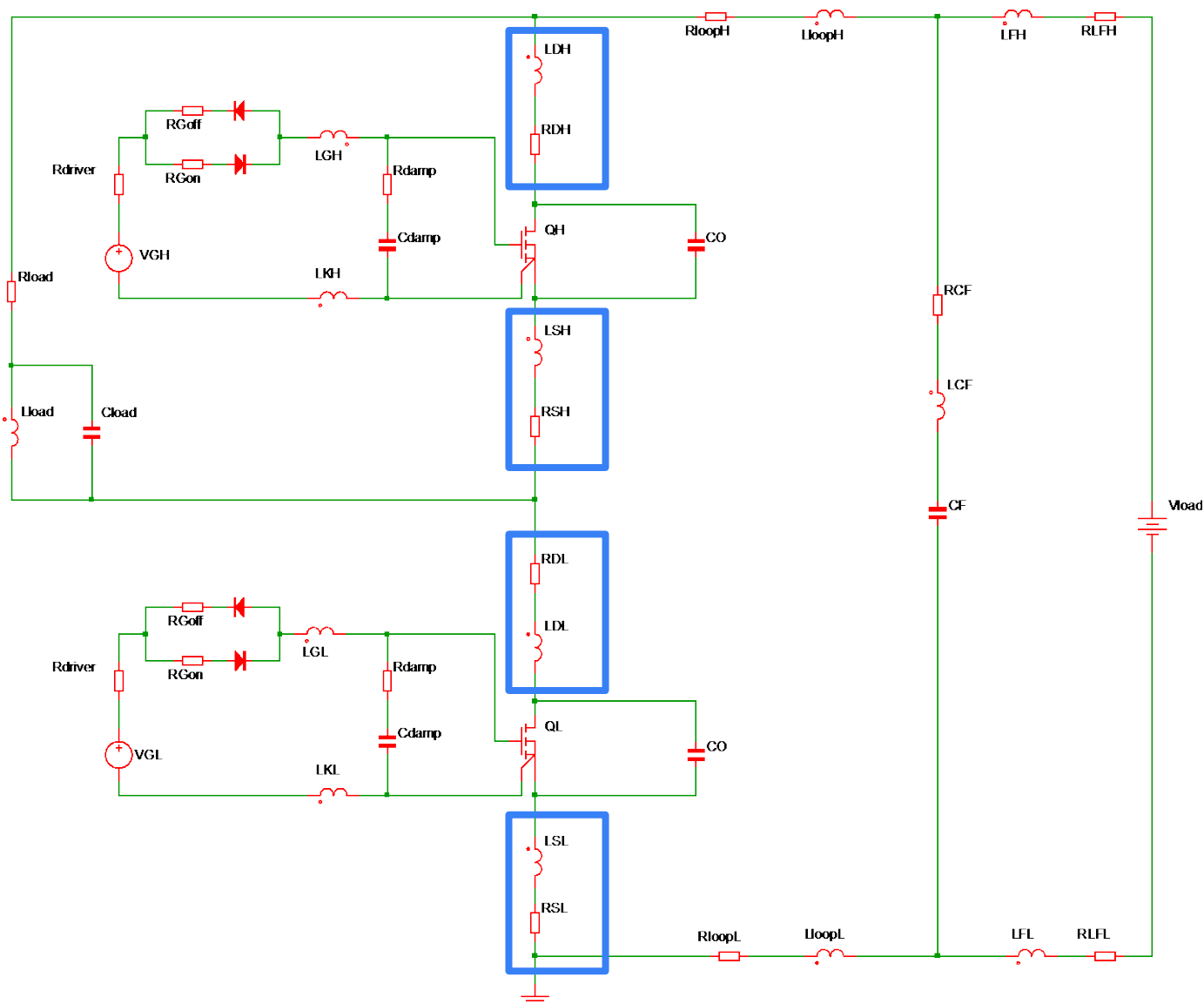


Switching Loop Parasitics

RloopH (Ω)	0.1m
LoopH (H)	2n
RloopL (Ω)	0.1m
LoopL (H)	2n

The switching loop inductance (in between the decoupling capacitor and the switching cell) is represented by L_{loopx} (with R_{loopx} as series resistance) on the positive and negative branch.

Step 5 : Interconnections leakage inductances

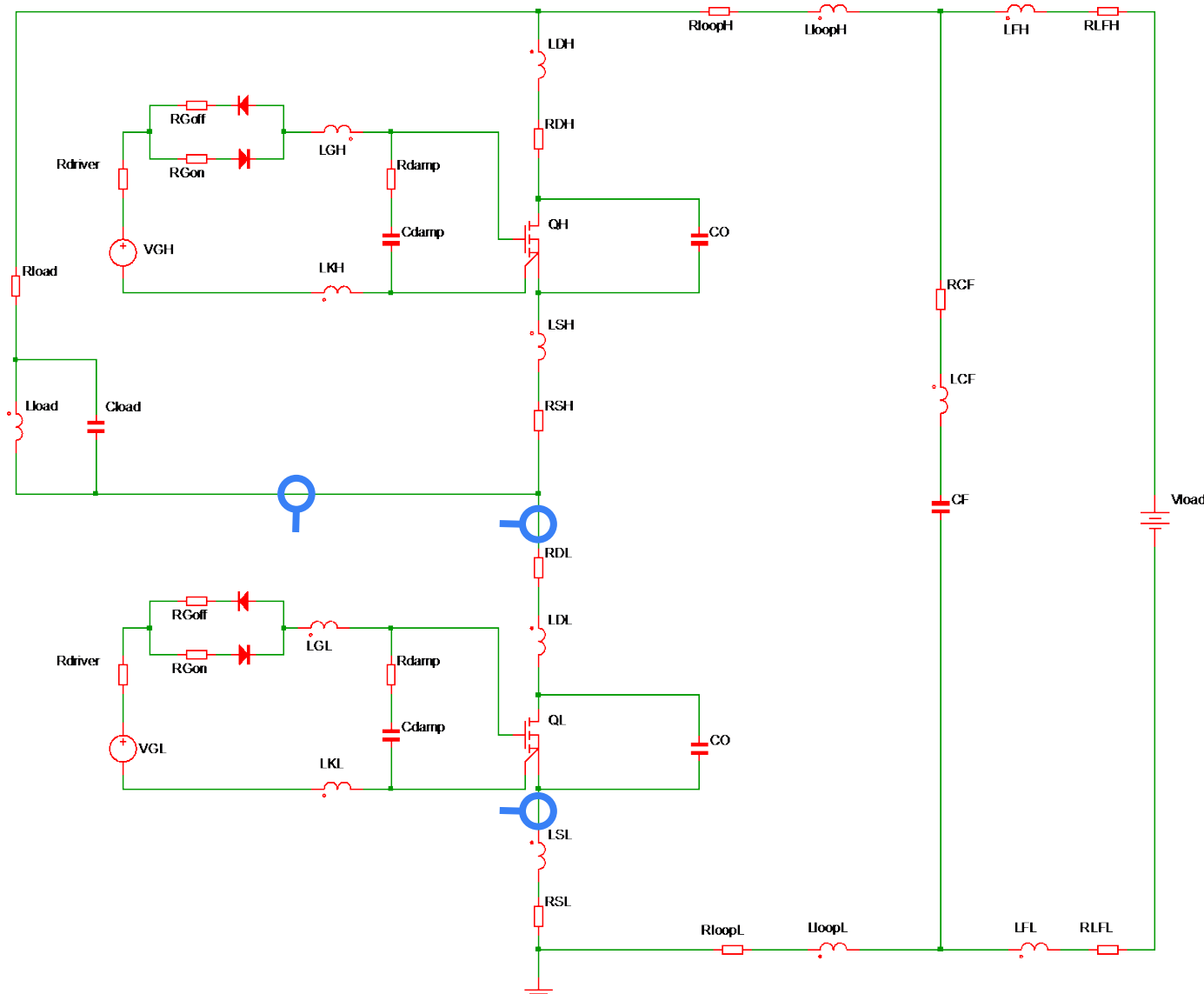


Devices Layout Parasitics

LDH (H)	2n
RDH (H)	0.1m
LSH (H)	2n
RSH (Ω)	0.1m
RDL (Ω)	0.1m
LDL (H)	2n
LSL (H)	2n
RSL (Ω)	0.1m

Drain and Source interconnections can also be modeled by inductances (with series resistances). There are 4 in total for the two switching devices.

Step 5 : Input Filter parameters



Current Measurement

Rshunt (Ω)

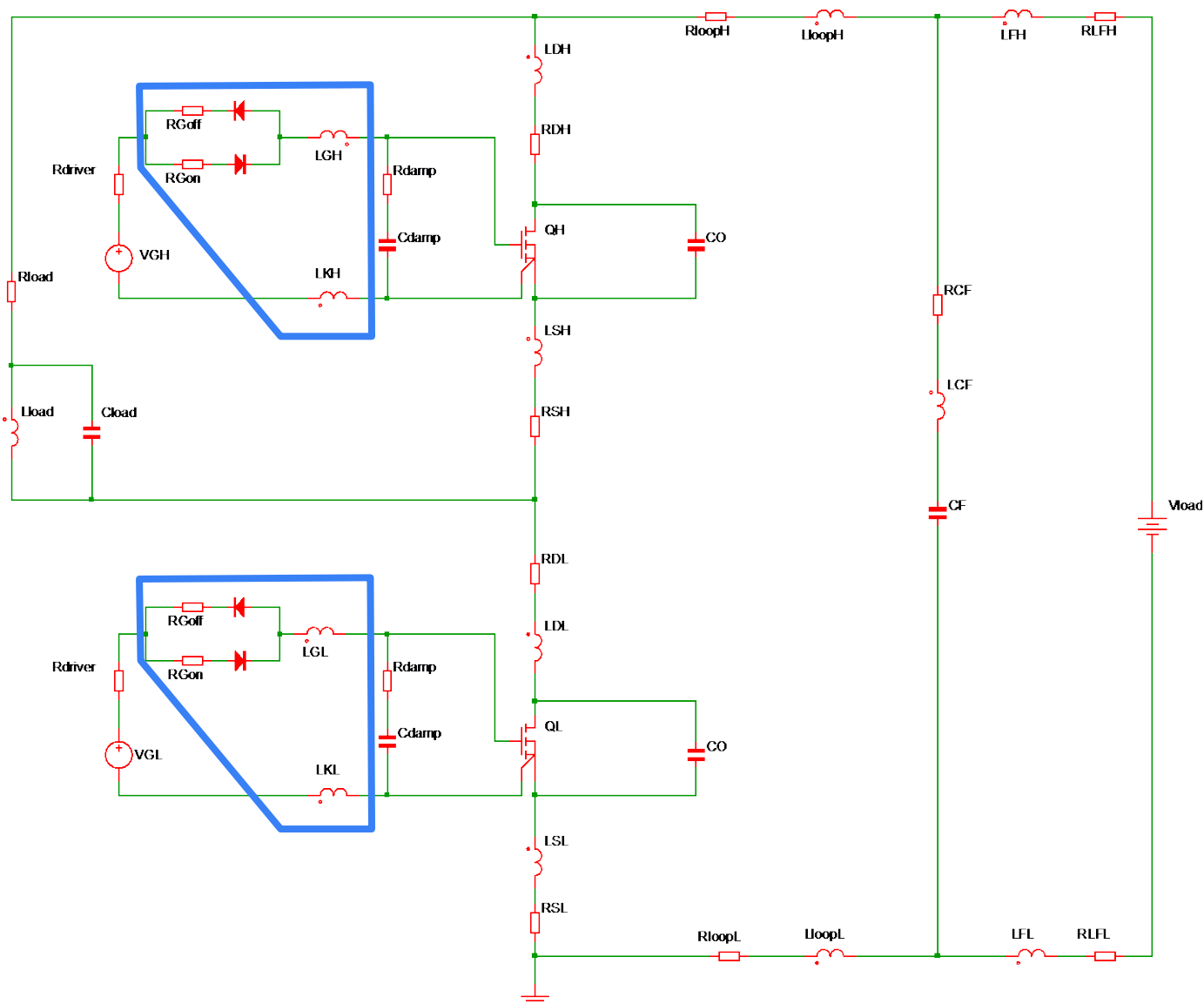
Rshunt Location

A current sense measurement based on a shunt resistor can be included in the loop in various place :

- in switching device Drain,
- in switching device Source
- in switching inductor

If the shunt is located in the other device drain or source, the interconnection series resistance can be increased accordingly.

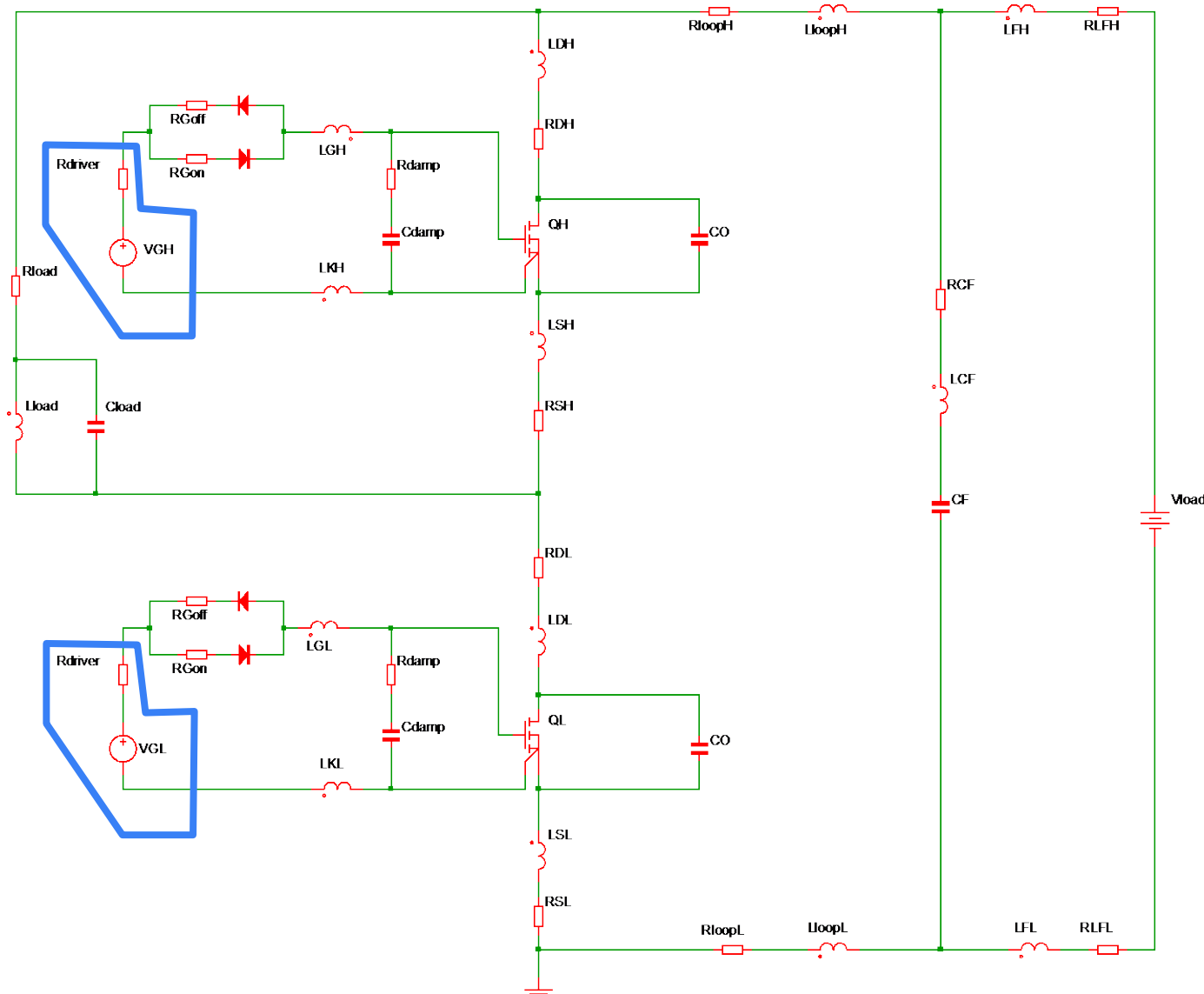
Step 5 : Gate Drive Circuit parameters



Gate Drive Circuit	
R _{Goff} (Default OFF Gate Resistance, Ω)	2
R _{Gon} (Default ON Gate Resistance, Ω)	2
R _{GoffMIN} (Min OFF Gate Resistance, Ω)	2
R _{GoffMAX} (Max OFF Gate Resistance, Ω)	10
R _{GonMIN} (Min ON Gate Resistance, Ω)	2
R _{GonMAX} (Max ON Gate Resistance, Ω)	10
L _{GH} (H)	5n
L _{KH} (H)	5n
L _{GL} (H)	5n
L _{KL} (H)	5n

The gate drive circuit includes two parasitic inductances LGx and LKx for interconnection and split gate resistors (RGon and RGoff) to control turn-on and turn-off speed.

Step 5 : Driver extra parameters

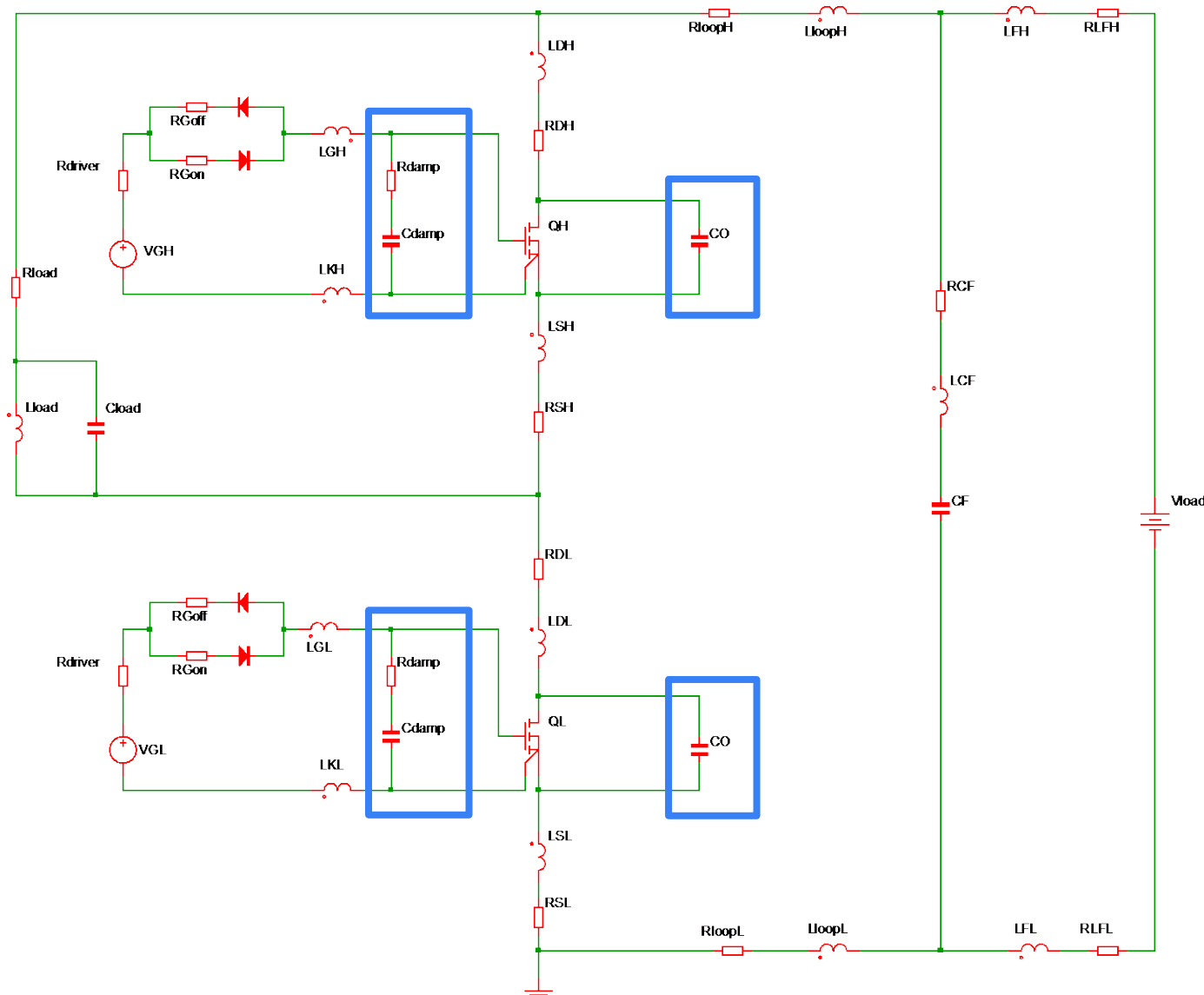


Gate Driver	
Rdriver (Gate driver internal resistance, Ω)	1
TR (Gate drive rise time, s)	50n
TF (Gate drive fall time, s)	50n

The driver is model by a pulse voltage source with Minimum and Maximum (ON and Off) voltage defined in Step 4.

In Step 5, the user defines the Rise (TR) and Fall (TF) times. The user can also give the driver internal resistance value Rdriver.

Step 5 : EMI Damping parameters



EMI Damping	
Rdamp (Ω)	100
Cdamp (F)	100p
CO (F)	47p

For EMI reduction, two damping circuits can be added.

Between Drain to Source, a parallel capacitor linearizes the switching device output capacitor.

Between Gate and (Kelvin) Source, an R-C series damping network will damp the Miller effect ringing.

Step 6: Submit Request

- From the 5 Circuit Schematic Tab, once all circuit parameters are entered, **Submit Request** button becomes active.
- User clicks on **Submit Request** and is brought to the Request Details page
- Requests take several minutes to complete depending on the density of the input characteristics.
- Modules take longer due to higher complexity compared to discretés.

The screenshot displays the 'Switching Circuit Schematic' interface. At the top, a navigation bar includes 'Home', 'Requests', 'User Guide', 'Application Note', 'Elite Power Simulator', and 'Support'. Below the navigation bar, the title 'Switching Circuit Schematic' is followed by the instruction 'Please fill in circuit parameters'. The main area is divided into two sections: a schematic diagram on the left and a parameter configuration table on the right.

The schematic diagram shows two half-bridge circuits. The top half-bridge is driven by a voltage source V_{GH} and includes a gate driver with internal resistance R_{driver} , gate-to-off resistance R_{Goff} , gate-to-on resistance R_{Gon} , and gate inductor L_{GH} . The MOSFET is modeled with parasitics R_{DH} , R_{SH} , R_{DL} , and R_{SL} , and a snubber network with R_{snub} , C_{snub} , and C_{damp} . The load is represented by R_{load} and C_{load} . The bottom half-bridge is driven by V_{GL} and has similar parasitics and components.

The parameter configuration table on the right is organized into categories:

Category	Parameters
Gate Driver	
R_{driver} (Gate driver internal resistance, Ω)	1
T_R (Gate driver rise time, s)	50n
T_F (Gate driver fall time, s)	50n
Gate Drive Circuit	
EMI Damping	
Load Inductor Parasitics	
R_{load} (Ω)	80m
C_{load} (F)	50p
Devices Layout Parasitics	
Switching Loop Parasitics	
R_{loopH} (Ω)	0
L_{loopH} (H)	16n
R_{loopL} (Ω)	0
L_{loopL} (H)	0
R_{DC} (Ω)	0
L_{DC} (H)	0
Input Filter	
Current Measurement	

At the bottom of the interface, there are three buttons: 'Previous Step', 'Reset', and 'Submit Request'. An orange arrow points from the 'Submit Request' button in the screenshot to the corresponding bullet point in the text on the left.

Step 7: Review Request Details Page

- The Request Details page provides user with
 - Details of the input parameters
 - Plots of the simulation results
 - Status field:
 - Pending – simulation in queue
 - Running – simulation running
 - Done – simulation completed
 - PLECS Model (XML File) download
 - Recall button: Enable users to recall the current request into a new request where changes can be made before submitting the new request. The current request is maintained.

Home Requests User Guide Application Note Elite Power Simulator Support

Request #1693
Characteristics for this request.

Status: Done [XML File](#) [Recall](#)

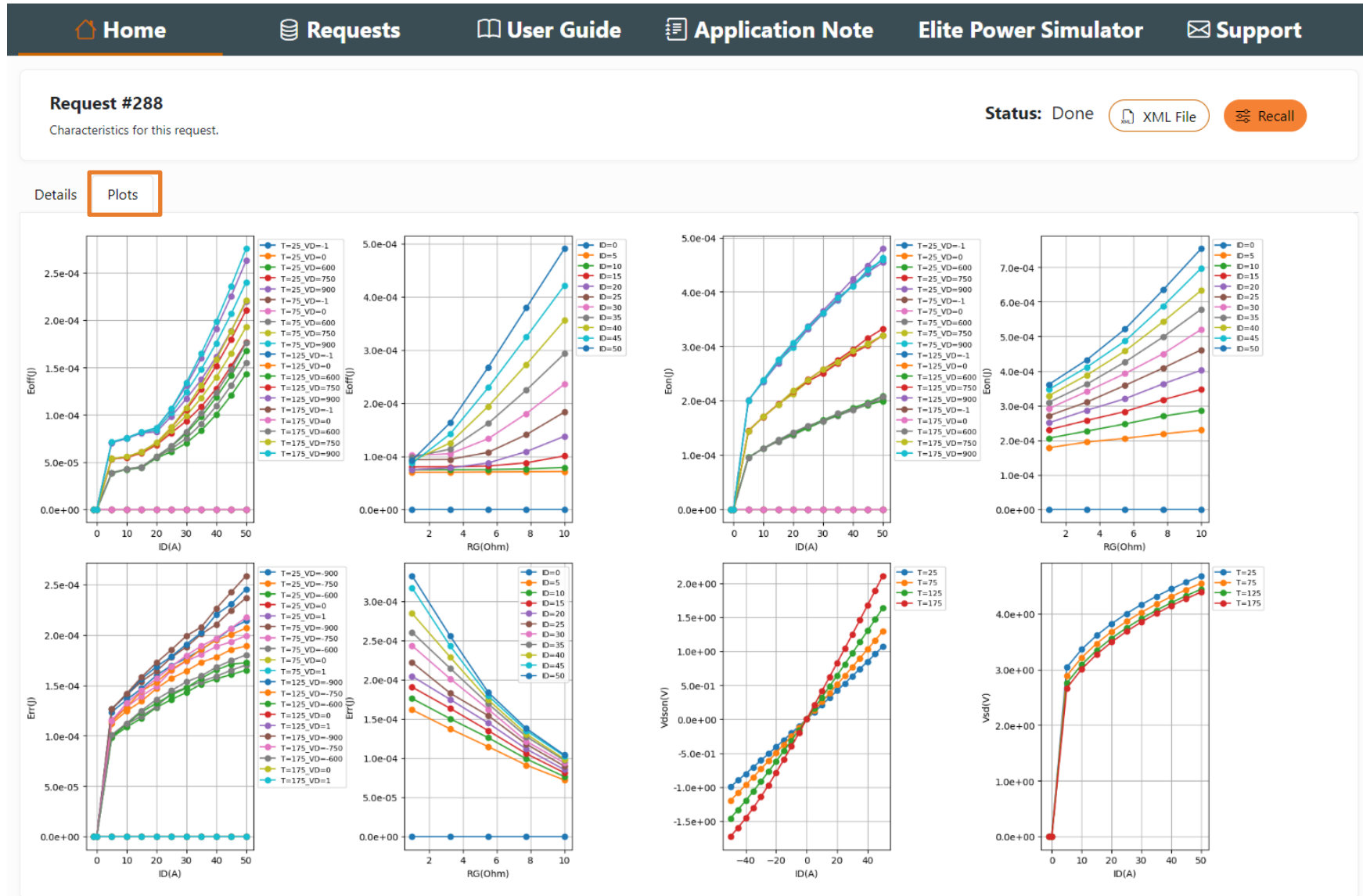
Details Plots

PLECS Model Download

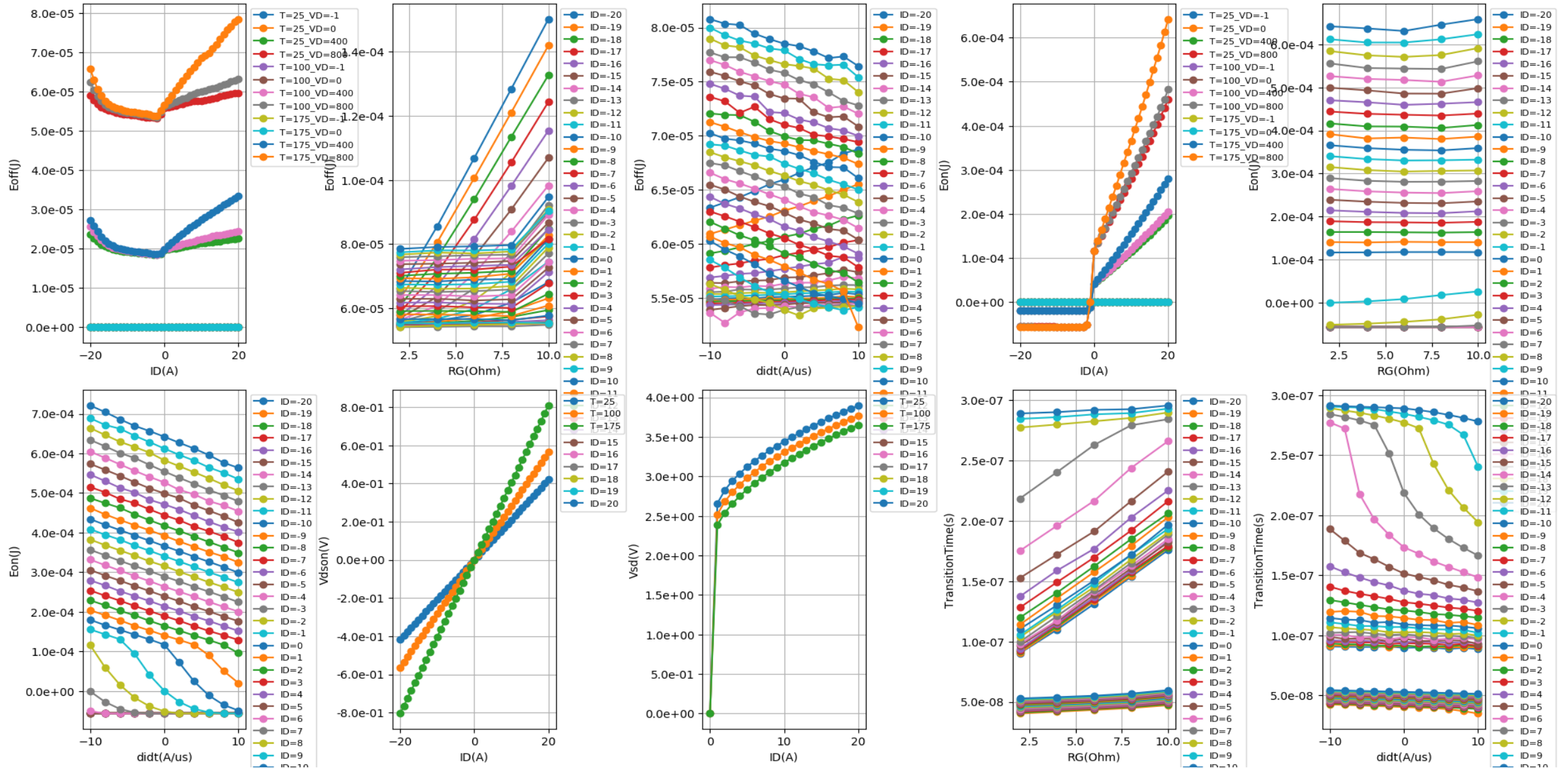
Category	Parameters
Product Information	^
Product Number	NTH4L022N120M3S
Product Type	discrete
Product Technology	M3
Product Voltage	1200V
Process Condition	Nominal
Switching Type	hard
Gate Drive Conditions	^
Conduction Parameters	^
Switching Parameters	^
Temperature List	25 75 125 175
Gate Driver	^
Gate Drive Circuit	^
EMI Damping	^
Load Inductor Parasitic	^
Device Layout Parasitics	^
Switching Loop Parasitics	^
Input Filter	^
Current Measurement	^

Step 7: Review Request Details Page – Plots Tab

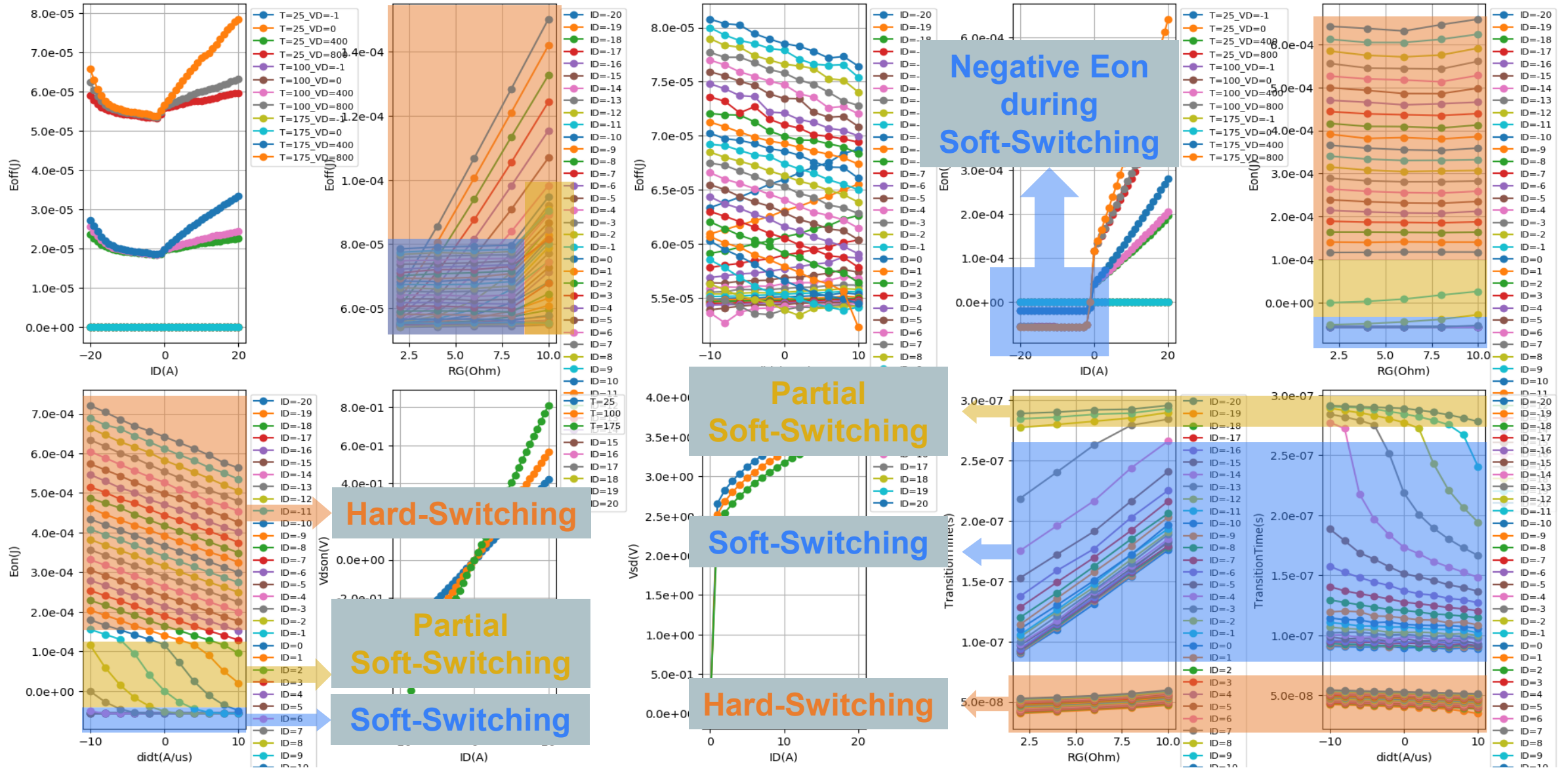
- The Plots tab provides users with multiple plots representing the data in the XML file.
 - Eoff, Eon, Err vs. ID (current) for different temperatures and voltage @default RG
 - Eoff, Eon, Err vs. RG for different currents @maximum temperature and voltage.
 - Transistor conduction plot VDSon vs. ID for different temperatures.
 - Diode conduction plot Vsd vs. ID for different temperatures.



Example Soft Switching Model Results

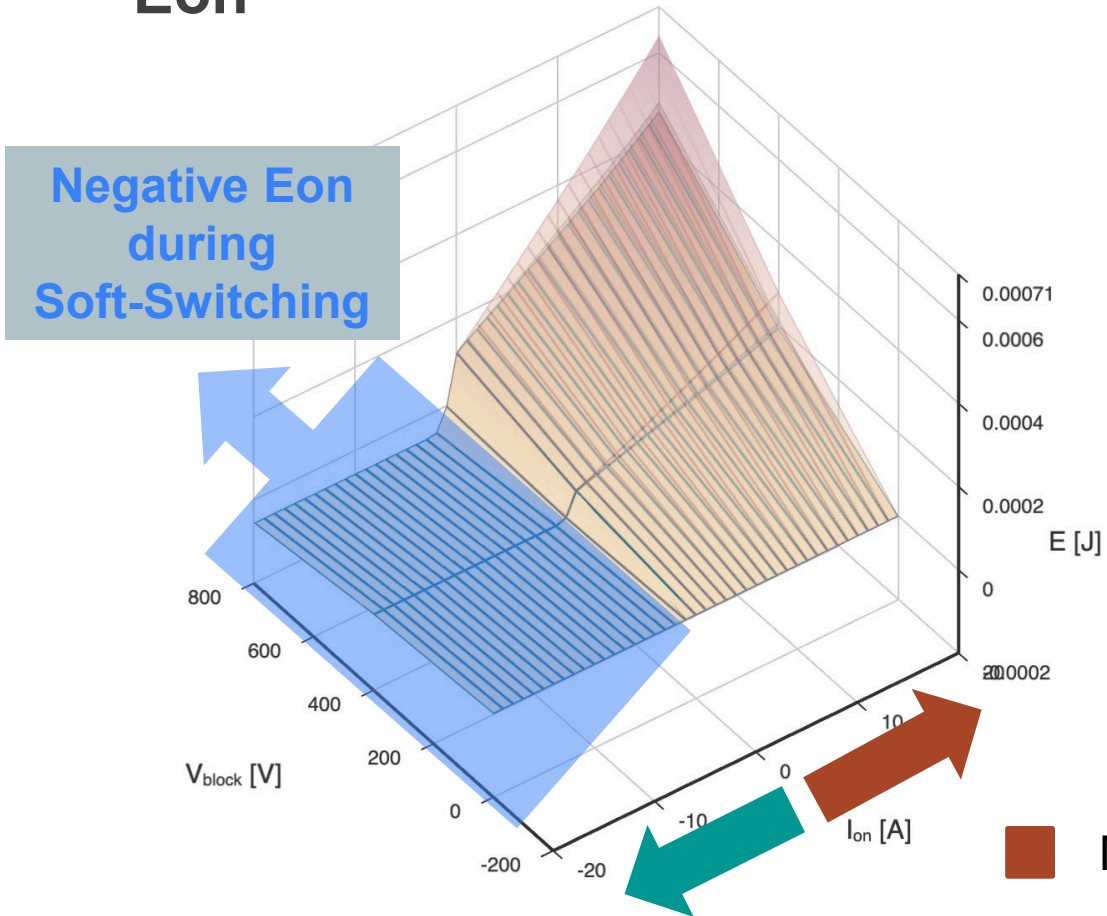


Example Soft Switching Model Results

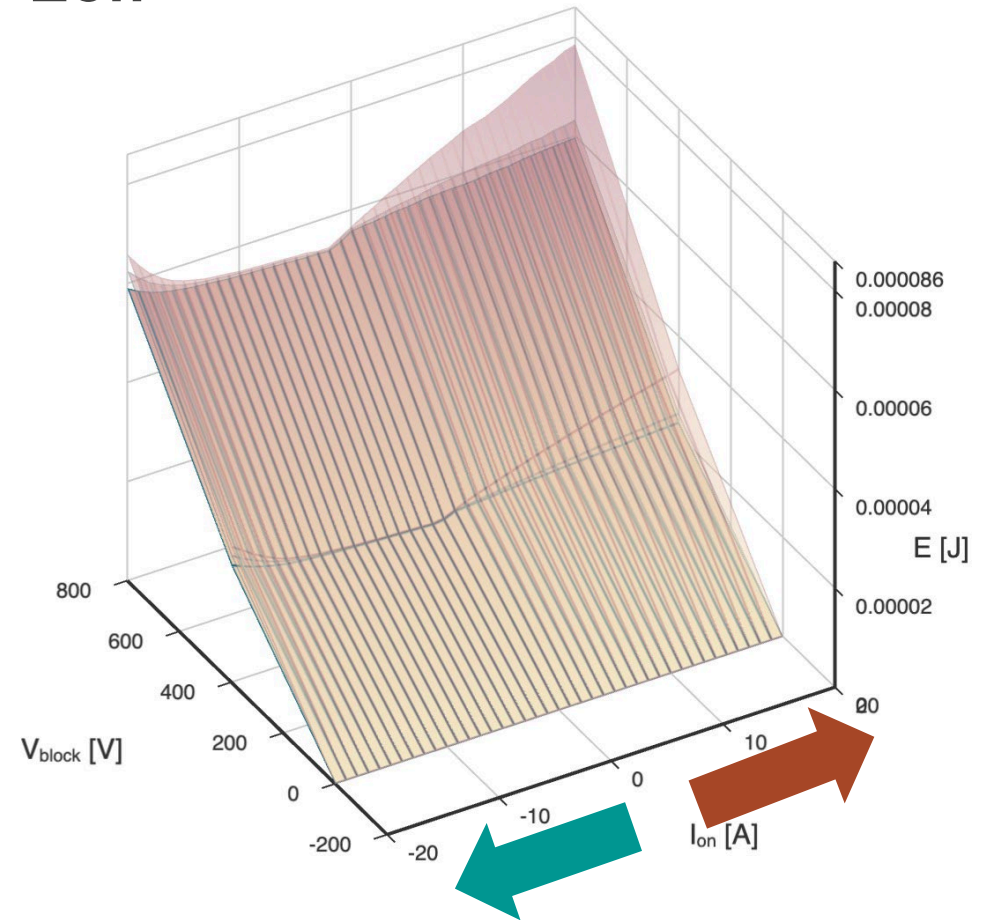


Example Soft Switching Model Results: 3D View

- E_{on}



- E_{off}



Step 8: Review Requests Summary Page

Home **Requests** User Guide Application Note Elite Power Simulator Support

Request List
Search through the request list and find

Sort and Search these fields
Note* **User will only see their requests**

#	Requester	Product Type	Technology	Voltage	Device Name	Process Condition	Status	Last Update	Model Downloads	Recall
263	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done	2023-03-10 14:34:56	XML XML	Recall
262	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done	2023-03-10 13:32:19	XML XML	Recall
261	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done	2023-03-10 13:00:45	XML XML	Recall
254	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done	2023-03-10 12:33:25	XML XML	Recall
253	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done	2023-03-09 21:51:40	XML XML	Recall
251	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done	2023-03-09 21:40:24	XML XML	Recall
250	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done	2023-03-09 21:39:24	XML XML	Recall
249	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done	2023-03-09 21:09:28	XML XML	Recall
247	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done	2023-03-09 17:30:30	XML XML	Recall

Click on request # to access Request Details Page

Download XML Model

Recall request into new request

Page 1 of 4 20

View 1 - 20 of 66

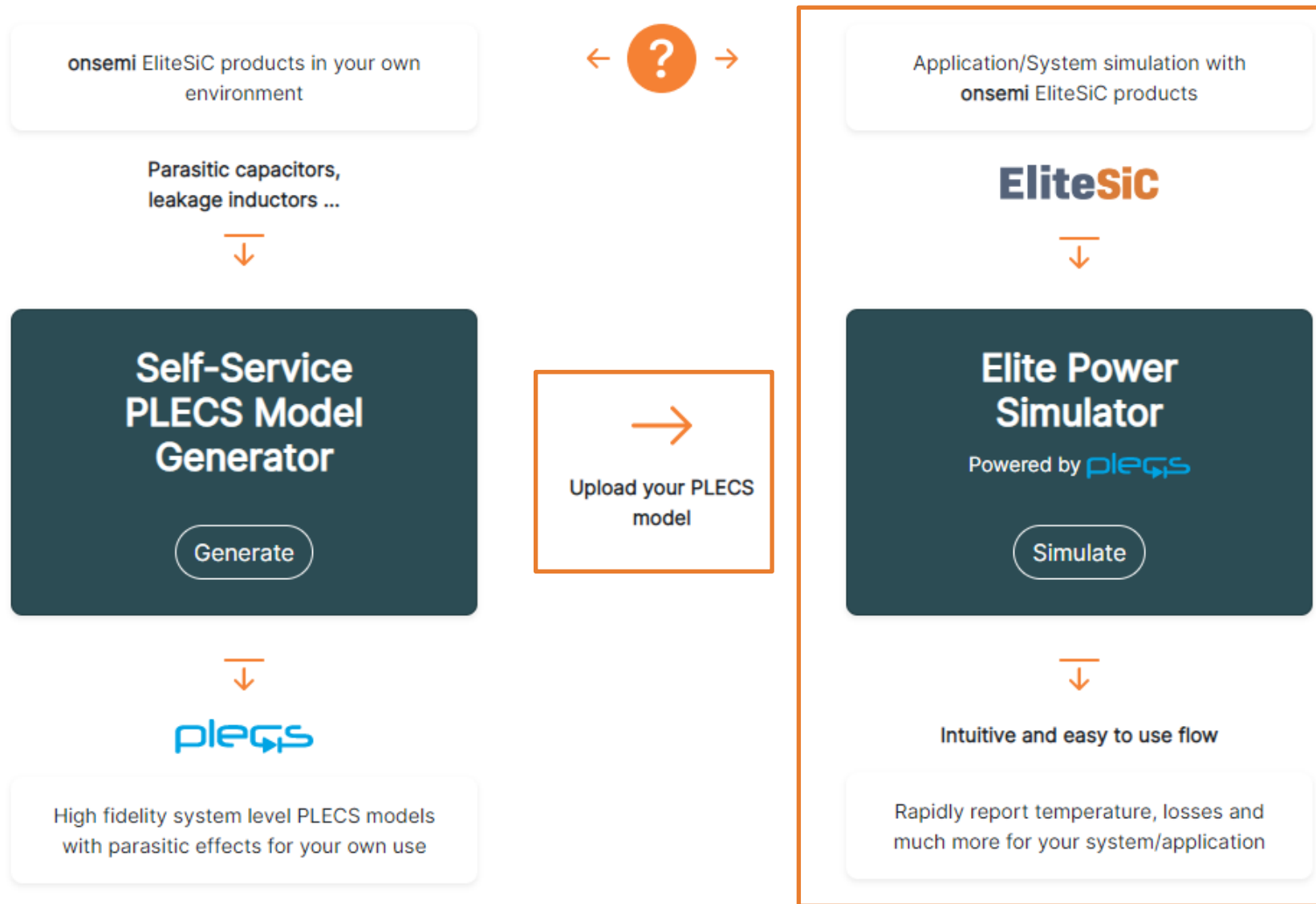
FAQ: Common Causes of SSPMG Failed Runs

- Very small switching current step ($<1A$) causing very long simulation times while not really improving the accuracy of the table model.
- Switching currents too close to 0 ($<1A$). In the EOFF extraction, 1% ID point by IEC standard will yield very small currents which can cause extraction errors due to leakage. For example, when $ID=0.1A$, the 1%ID will be only 1mA, which could be less than the leakage for some high temperature conditions.
- Switching load voltages are too low. Very low V_{load} can cause errors in the EON extraction, in which we need to measure 3%VDS by IEC standard.
- Switching load voltage too close to the device breakdown voltage BV can cause issues if there is overshoot of VDS in turn off. If the overshoot is higher than BV, the breakdown current will generate strange behaviors.
- For soft switching, users put very small negative current.. For these inputs, there would be only 1 or 2 points for negative current yielding poor results. There should be at least 3 points in the negative current range.
 - `lswitch_min=-1 lswitch_max=50 lswitch_step=5`
 - `lswitch_min=-10 lswitch_max=50 lswitch_step=5`
- Very large di/dt could cause convergence issues or very strange behavior.
- In general check ranges of parasitics. Unreasonable large inductors, resistors and capacitors can cause issues. For example, large CLOAD/CO could cause very long turn on/off edge.

Outline of User Guide

1	Introduction to Self-Service PLECS Model Generator: What is it and What are the benefits
2	Step by Step Tool Flow
3	Deploying PLECS Models in Elite Power Simulator and PLECS Stand Alone

Deploying PLECS Models in Elite Power Simulator



Load SSPMG models into Elite Power Simulator

In Device Configuration Tab, user can select to upload SSPMG generated model

Application — Device Selection — **3 Device Configuration** — 4 Circuit Parameters

MOSFET configuration

Device name: NTH4L022N120M3S

Number of parallel devices
Value *
1

Turn-on gate resistance $R_{g-on,ext}$
Value *
4.5

Turn-off gate resistance $R_{g-off,ext}$
Value *
4.5

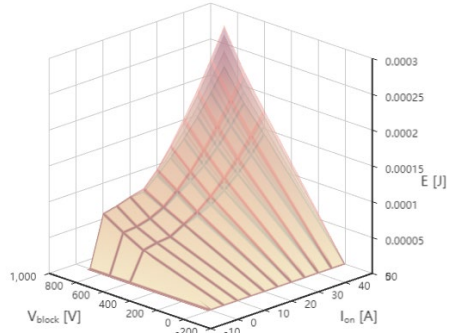
Loss model type

Nominal loss data Best case conduction loss/worst case switching loss Worst case conduction loss/best case switching loss Upload PLECS custom loss model from onsemi's SSPMG tool

Model data file

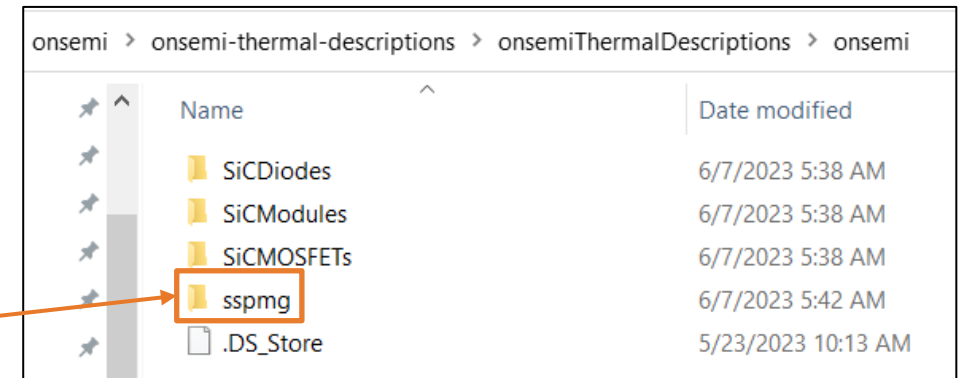
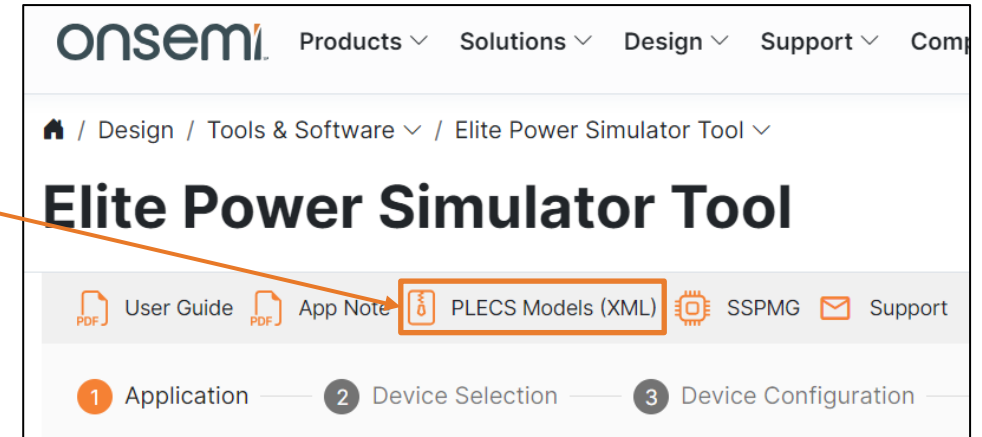
Select model file **Browse for SSPMG XML file**

Previous Step



Load SSPMG models into PLECS Stand Alone

- First download PLECS models from Elite Power Simulator and follow instructions in "Install.txt" file.
 - *To install the onsemi SiC library components and corresponding thermal descriptions (XML files), simply add this directory (containing the "onsemiThermalDescriptions/" folder, "onsemiComponentLibrary_public.plecs" PLECS model, and "info.xml" file) into the list of thermal description search paths in the Thermal tab of the PLECS Preferences window. Click the Refresh button on the left side of the list and click OK to load the onsemi files into PLECS. Then a new entry in the PLECS Library Browser should appear "onsemi Block Library" containing several components that can be dragged into your own circuit models and directly be used with the provided thermal descriptions.*
- Create subfolder sspmg here and place SSPMG XML files in this directory. Note folder can be any name.



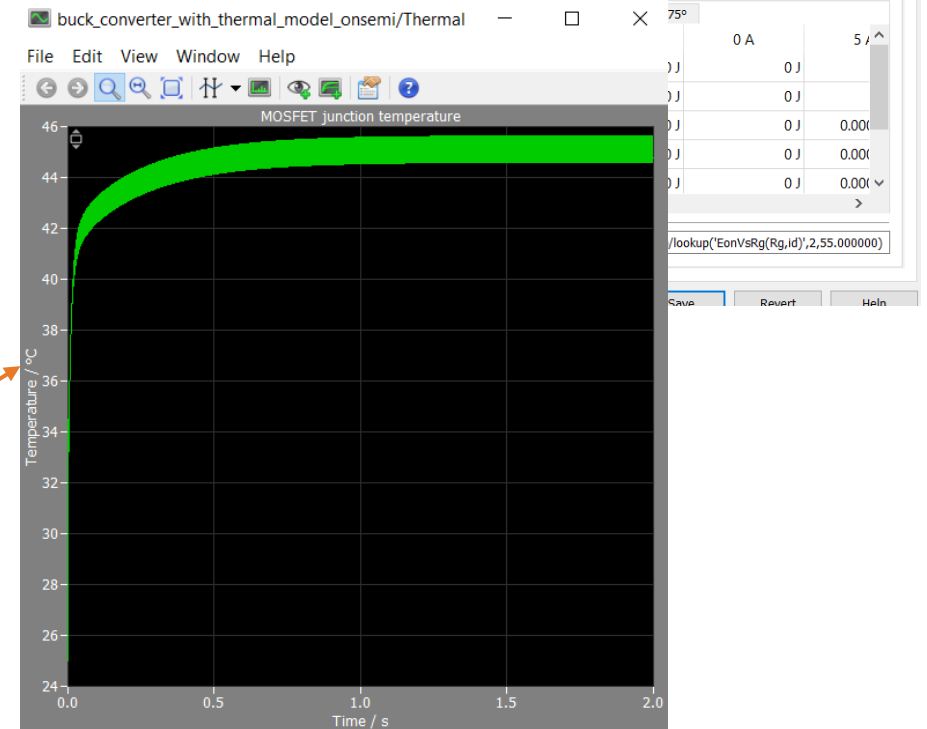
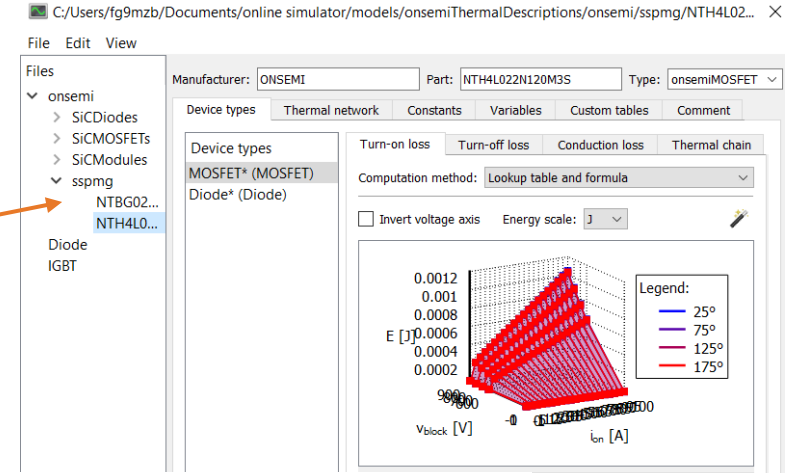
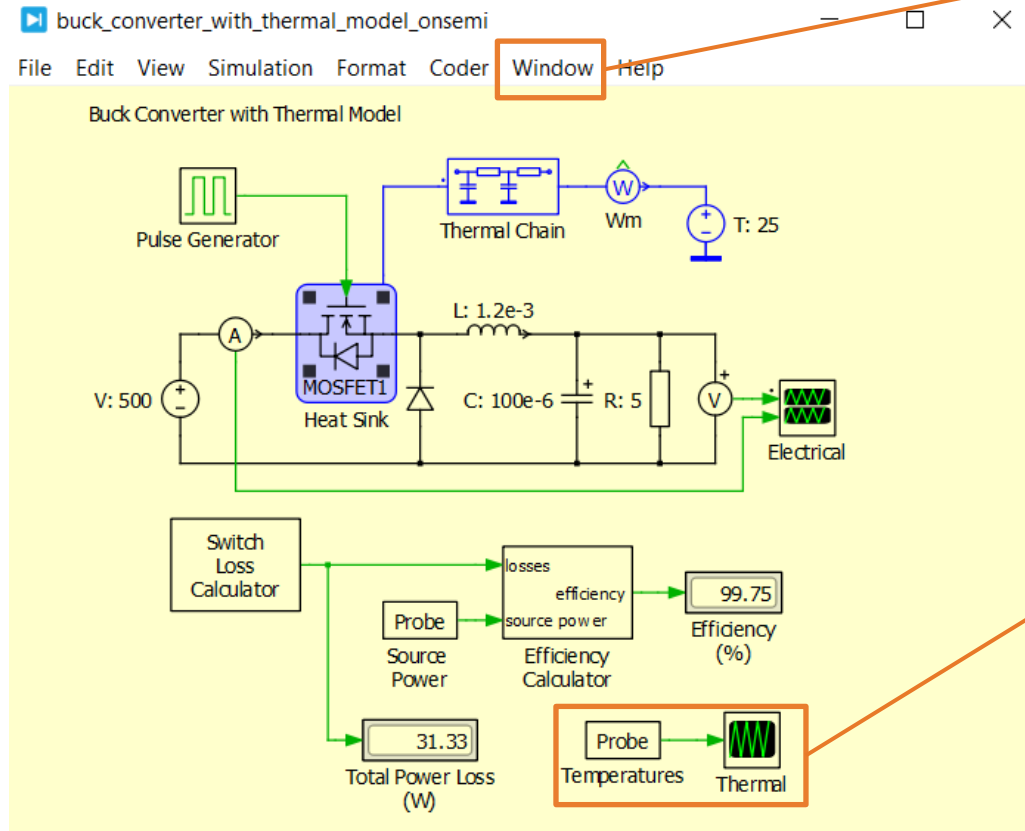
Load SSPMG models into PLECS Stand Alone

- Place an onsemi SiC-Si MOSFET or Si IGBT in PLECS schematic.
- Double click MOSFET/IGBT symbol and browse for SSPMG XML file.

The image displays the PLECS software interface. On the left is the 'Library Browser' window showing the 'onsemi Block Library' with 'onsemi SiC-Si MOSFET' selected. The main workspace shows a schematic titled 'Buck Converter with Thermal Model'. The schematic includes a Pulse Generator, a MOSFET block (MOSFET1) connected to a Heat Sink, an inductor (L: 1.2e-3), a capacitor (C: 100e-6), a resistor (R: 5), and a 500V source. A Thermal Chain block is connected to the MOSFET and Heat Sink, with a thermal node T: 25. Below the schematic are several analysis blocks: a Switch Loss Calculator, a Probe for Source Power, an Efficiency Calculator showing 99.75% efficiency, a Probe for Total Power Loss (W) showing 31.33, a Probe for Temperatures, and a Thermal block. On the right, the 'Block Parameters' dialog for 'onsemi SiC-Si MOSFET (mask) (link)' is open. It contains instructions on how to use the component and a 'MOSFET' field where the file path 'onsemi/sspmg/NTH4L022N120M3S_nominal_sspmg584' is entered. An orange arrow points from the selected MOSFET in the library to the MOSFET block in the schematic, and another orange arrow points from the MOSFET block to the file path field in the dialog.

Load SSPMG models into PLECS Stand Alone

- Review XML data under Window → Thermal Library Browser
- Run simulation



Questions?

Have questions, comments, or need support with your Self-Service PLECS Model Generator needs? We're here to help! Write us an email at sspmg@onsemi.com.

- Self-Service PLECS Model Generator:
www.onsemi.com/self-plecs-generator
- Elite Power Simulator:
www.onsemi.com/elite-power-simulator

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