NCV760040 Automotive Satellite Camera Power Distribution Reference Design

TND6463/D

Power Distribution in Automotive Applications

With the increasing number of electronic devices and systems in modern vehicles, efficient and reliable power distribution is more important than ever. In a zonal architecture, the idea is that electrical power can be distributed more efficiently among the zones, thus reducing losses and improving overall vehicle efficiency. The example of such approach is demonstrated in Figure 2.

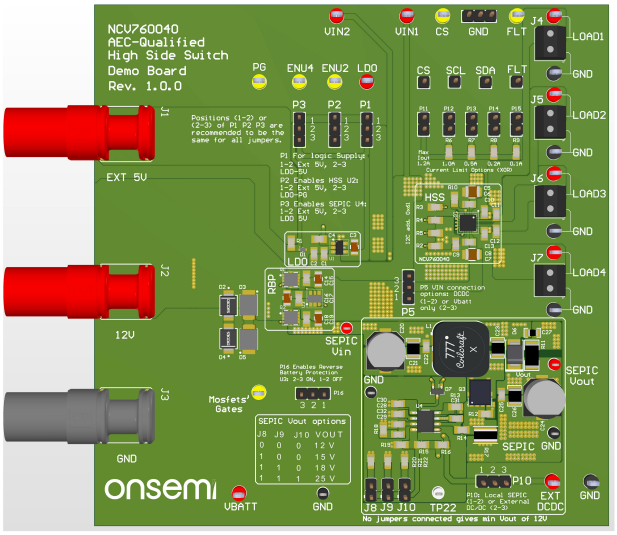

Figure 1. onsemi's NCV760040 Reference Design

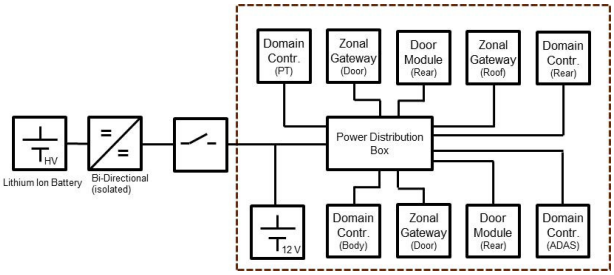

Figure 2. Typical BEV Power Architecture

Safety Features for Zonal Power Architectures

onsemi's next generation integrated circuits (IC) are designed to address the needs of future advanced driver assistance systems (ADAS) by introducing state-of-art intelligent ASIL-relevant features directly at the sensing front-end, i.e., by incorporating the diagnostics into the load-switching IC. Some of the features found in **onsemi**'s portfolio are:

- Multichannel Load Control,
- Communication with MCU via I^2C or SPI,
- Sleep Mode,
- Safety Monitoring Features:
  - Under- & Over-Voltage Protection,
  - Current Sense & Adjustable Limit,
  - Over-Temperature Detection and Protection,
  - Short-to-Ground/-Battery Detection and Protection,
  - Open-Load Detection,
  - Fault & Enable Pin.

As a result, the zonal system gains additional diagnostic features directly at the load-switching level which offers following benefits:

- It prevents a hardware failure from propagating− fault containment− that could otherwise lead to the occurrence of safety-relevant event and eventually to a safety hazard.
- It reduces the reaction time of a preventive action− refer to Fault Tolerant Time Interval (FTTI).
- It simplifies the system design which increases its reliability, safety and reduces its overall cost.

ASIL-C Readiness

Modern automotive driver assistance systems such as Adaptive Cruise Control (ACC) require a minimum of ASIL-C level of ISO26262 compliance. The aforementioned safety monitoring features that can be found in **onsemi**'s quad-channel high-side switch NCV760040, were included to support the designers targeting the ASIL-C for their systems.

Introduction to the Reference Design & System Considerations

The focus of this document is the design, implementation and testing of a state-of-art design power management infrastructure for Advanced Driver Assistance Systems (ADAS).

ADAS hardware is typically designed as shown in Figure 3. It comprises the camera (or any other sensor), and the controller subsystem, referred to also as an ADAS domain controller or ADAS Electronic Control Unit (ECU). The red line corresponds to the power supply line, blue line to the data line. To reduce the complexity the data and power are transmitted between the controller and each camera subsystem over a single coaxial cable− the method is referred to as Power-over-Coax (PoC). Such an approach requires the use of (de)serializer and additional filtering.

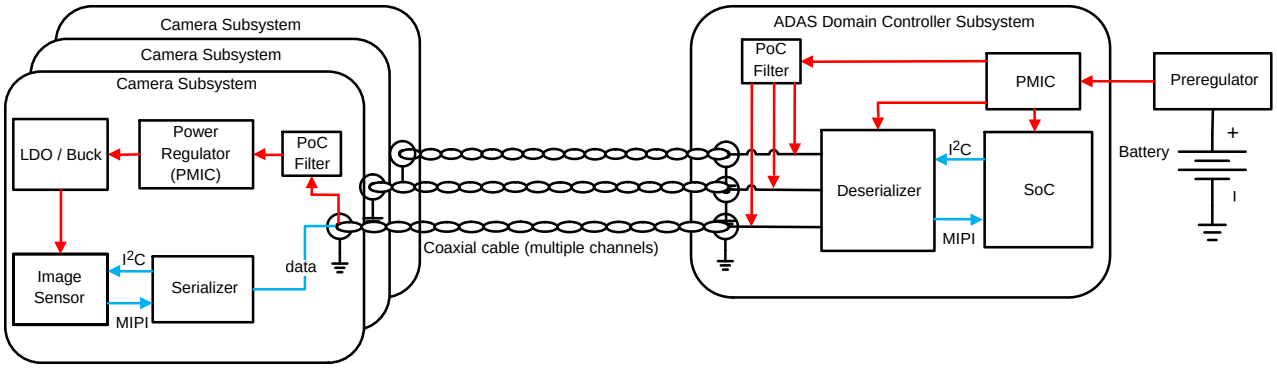

Figure 3. Power Distribution and Data Transfer Between the Camera and the Control Unit

The block diagram from Figure 4 shows the main elements of the reference design from Figure 1. Typically, the quad high side switch NCV760040 distributes, monitors and controls the power to each of the four loads at the domain controller end. The data path, including deserializer and SoC, is not in the scope of this reference design.

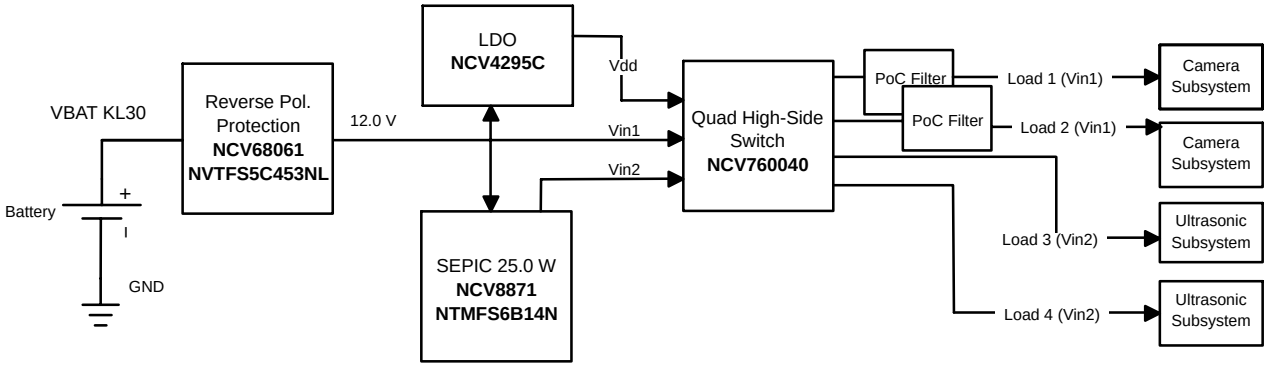

Figure 4. Block Diagram of the Reference Design − Power Source for Satellite Cameras and Ultrasonic

The ADAS Domain Controller is powered by the 12 V rail via the reverse polarity protection NCV68061− described below. The SEPIC is based on the NCV8871 Boost Controller and provides a stable output voltage of approx. 12 V. As the battery voltage can vary over a large range, a buck-boost topology is needed, to always ensure a stable output voltage.

Overview of Quad High-Side Switch Reference Circuit

Table 1. NCV760040 PARAMETERS

Parameter	Conditions	Symbol	Typ	Max	Unit
DC Output Current	1 channel ON	I_{out}	1000	1200	mA
	4 channels ON		529	854	
ON Resistance	Per channel	R_{DSON}	0.5	1.0	Ω
Quiescent Current	@ 13.2 V_{out}	I_g	1.0	5.0	μA

NCV760040 is an automotive-grade integrated driver that features four high-side switches, i.e., back-to-back N-Channel MOSFETs. It is designed for various applications, including ADAS and automotive Body Control systems.

The device offers adjustable current limit per channel and protection against over-temperature, short to battery, and loss of ground. It is controlled and diagnosed via an I^2C bus, which allows for output control and diagnostic reporting. It is available in a QFNW20 package with wettable flanks and includes an exposed pad to enhance thermal performance.

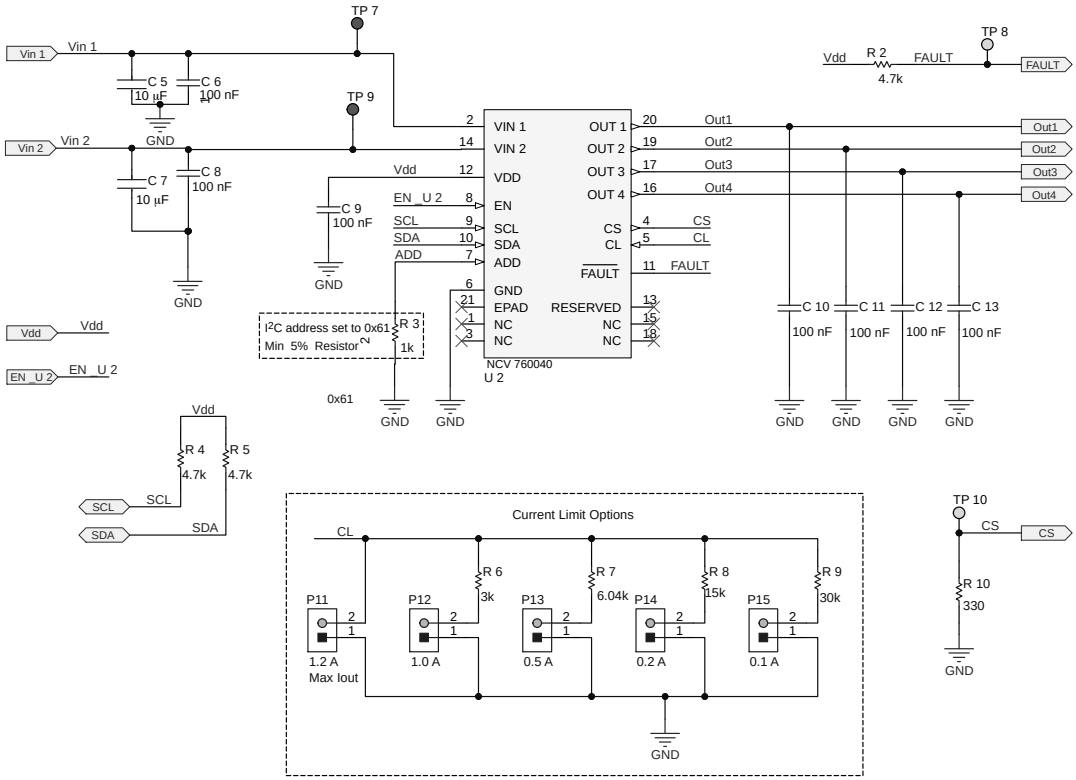

Figure 5. NCV760040 Reference Schematic

onsemi provides a dedicated graphical interface (GUI) (Figure 6) for the evaluation of the device. To use the GUI additional hardware is required to act as the communication interface between the computer and NCV760040. **onsemi** provides firmware that supports a limited number of microcontrollers (MCU). The GUI connects with the MCU via UART protocol whereas the MCU controls the NCV760040 via I^2C protocol. For the purpose of this document, Arduino Uno and Nano were used. The firmware is available upon request.

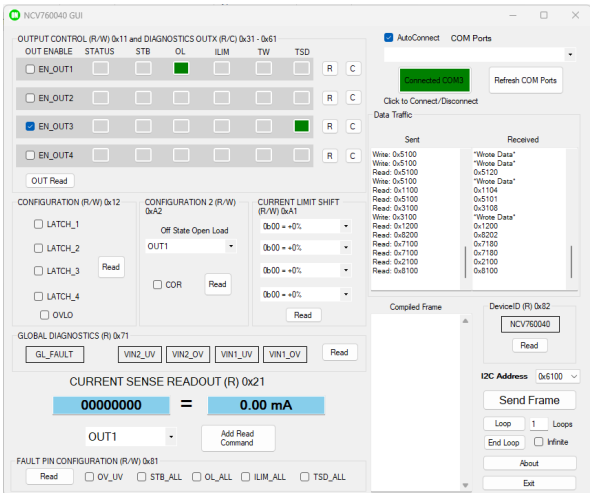

Figure 6. NCV760040 I^2C Register GUI

Current Limiting

The OC event detection time in case of less drastic OC event can be longer due to CS and CL front-end tolerances and voltage reference fluctuations as they impact the effective I_{LIM} value (eq.1 in datasheet). For the actual accuracy values, refer to Table 6 in the datasheet. It is critical to consider the limitations and the accuracies of those safety mechanisms while designing a safety-critical system.

Attached to the current limit (CL) input pin is an adjustable resistor ladder with maximum current setting at 1.2 A. See NCV760040 datasheet “Select Current Sense Resistor” paragraph. Table 2 assumes that no current limit shift is used (CL_SHIFT_X = 0b00).

Table 2. CL RESISTANCE (R_{CL}) VS. CURRENT LIMIT ($I_{OUT\ MAX}$)

R_{CL} [kΩ]	$I_{out\ max}$ [A]
2.5	1.2
3.0	1.0
6.0	0.5
15.0	0.2
30.0	0.1

The below figures demonstrate the behavior during the overcurrent (OC) event. The fault flag must be cleared under no-load condition to re-enable the power to the load.

In Figure 7 (5 ms/division) the red signal (Channel 2, 500 mA/div) is the load current of 2000 mA that causes the overcurrent (OC) event. The protection is triggered as soon as the current exceeds the maximum allowed value of 1200 mA (ILIM, CL pin shorted to ground) which is observed by the fall of output voltage (Channel 1 − yellow, 5.0 V/div). Within less than 20 ms − typical current limit shutdown time Tlatch0− the output current is switched off automatically by the NCV760040.

In Figure 8 (100 μs/div) the load current (red) is set to 1600 mA. In addition to the RCL resistor at the CL pin − the CL_SHIFT_X[1:0] register value, where X is the selected channel: 1,2,3,4 − is changed to 0b01 to shift the ILIM value by 30%, i.e., 1.56 A. For the comprehensive overview of the OC configurations and the resulting ILIM values, see Table 10 in NCV760040 datasheet.

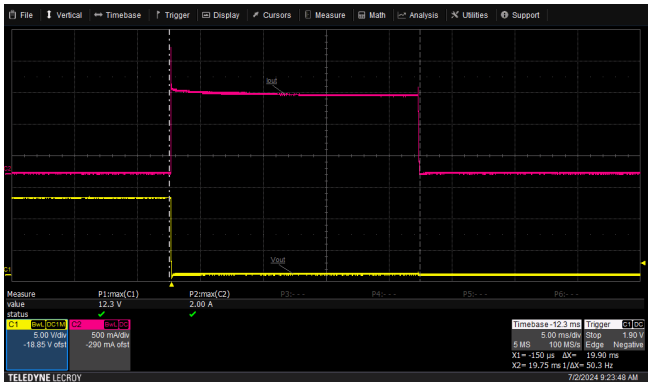

Figure 7. OC Event @ Load: 12 V, 2 A. ILIM − 1.2 A, CL Shift = 0%, CL Shutdown Time − 20 ms

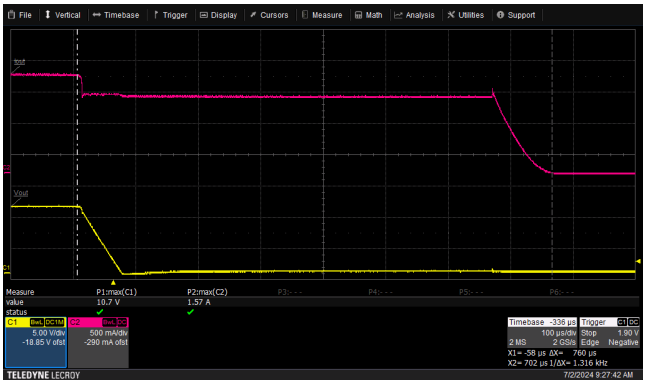

Figure 8. OC Detection (Dashed White Line) & Shutdown @ ILIM − 1.56 A, CL Shift = 30%

Overview of Single-Ended Primary-Inductor Converter (SEPIC) Circuit

Table 3. NCV887103 PARAMETERS

Parameter	Comments	Symbol	Min	Typ	Max	Unit
Op. Input Voltage	Load Dump: 45 V	U_{in}	3.2	–	40.0	V
Quiescent Current	Operating Mode	I_q	–	3.0	6.0	mA
Driving Voltage	See “Absolute Maximum Ratings”, “Typical Values” for NCV887103	U_{DRV}	–	8.4	12.0	V
Switching Frequency		f_{sw}	306	340	374	kHz
Current limit Threshold Voltage		U_{CL}	180	200	220	mV

For this reference design a SEPIC topology is selected due to its low component part count and good efficiency for the given output power. NCV8871 is an automotive-grade, non-synchronous controller used to drive an external N-channel MOSFET (here NTMFS6B14N). For more part-specific information see “Typical Values” and “Electrical Characteristics” tables in the datasheet.

Table 3 contains selected parameters of the part while Table 4 shows the possible output voltage (U_{out}) configurations that the reference design supports. The resulting duty cycle values were calculated according to formula (1). Refer to SEPIC Design Methodology paragraph of NCV8871 datasheet for more considerations on the SEPIC power stage design.

The below duty cycle formula (1) includes the forward voltage drop U_{fwd} (see Maximum Instantaneous Forward Voltage in the datasheet − 0.63 V for NRVBS360T3G) of the Schottky diode which typically accounts for additional 0.7 V drop at the output of the converter. The formula assumes Continuous Conduction Mode (CCM) – where inductor current never drops to zero during full-load operation− and 100 % efficiency. This offers more robustness for higher loads and is the optimal choice for wide input, wide output voltage designs such as here. It is not disadvantageous to assume such a scenario even if the device is going to be used for lighter loads, thus in Discontinuous Conduction Mode (DCM). If the intention is to design possibly the lowest-size converter, the DCM formulas shall be used when calculating the inductor size.

$$\frac{D}{1-D} = \frac{U_{out} + U_{fwd}}{U_{in}} = \frac{I_{in}}{I_{out}} \rightarrow D = \frac{U_{out} + U_{fwd}}{U_{out} + U_{in} + U_{fwd}} \quad \text{(eq. 1)}$$

The SEPIC circuitry is conceptualized such that it offers a range of four output voltages as shown in Table 4. These are the typical voltages in automotive sensing applications. Knowing that the output power (P_{OUT}) is constant, equal to 25 Watt, the resulting output current I_{OUT} is calculated.

Table 4. REFERENCE DESIGN INPUT – OUTPUT SIGNAL SPECIFICATION

Min. Input Voltage $U_{in(min)}$ [V]	Max. Input Voltage $U_{in(max)}$ [V]	Output Voltage U_{OUT} [V]	Max. Output Current I_{OUT} [A], 25 Watt	D_{min} ($U_{in(max)}$) [%]	D_{max} ($U_{in(min)}$) [%]
5	18	12	2.0	41.2 (buck)	71.6 (boost)
6		15	1.6	46.5 (buck)	72.3 (boost)
8		18	1.3	50.9 (buck-boost)	70.0 (boost)
9		25	1.0	58.7 (boost)	74.0 (boost)

Example:

The design supports 25 V output voltage U_{OUT} for the input voltage (U_{in}) ranging from 9 ($U_{in(min)}$) to 18 V ($U_{in(max)}$). On the other hand, for U_{OUT} = 12 V, the input voltage U_{in} can be as low as 5 V ($U_{in(min)}$) going up to 18 V ($U_{in(max)}$). Below the calculation of the duty cycles for U_{OUT} = 12 V in Table 4 is shown.

$$D_{min} = \frac{U_{out} + U_{fwd}}{U_{out} + U_{in(max)} + U_{fwd}} = \frac{12\ V + 0.63\ V}{12\ V + 18\ V + 0.63\ V} = 41.2\%$$

$$D_{max} = \frac{U_{out} + U_{fwd}}{U_{out} + U_{in(min)} + U_{fwd}} = \frac{12\ V + 0.63\ V}{12\ V + 5\ V + 0.63\ V} = 71.6\%$$

As per Table 4, the duty cycle is the lowest for the highest input voltage setting – in this case $U_{in(max)}$ = 18 V. The duty cycle (D) rises along as the input voltage (U_{in}) decreases, hitting 50 % at the 1:1 U_{in}−U_{OUT} voltage ratio, and further increasing as the SEPIC enters the boost mode.

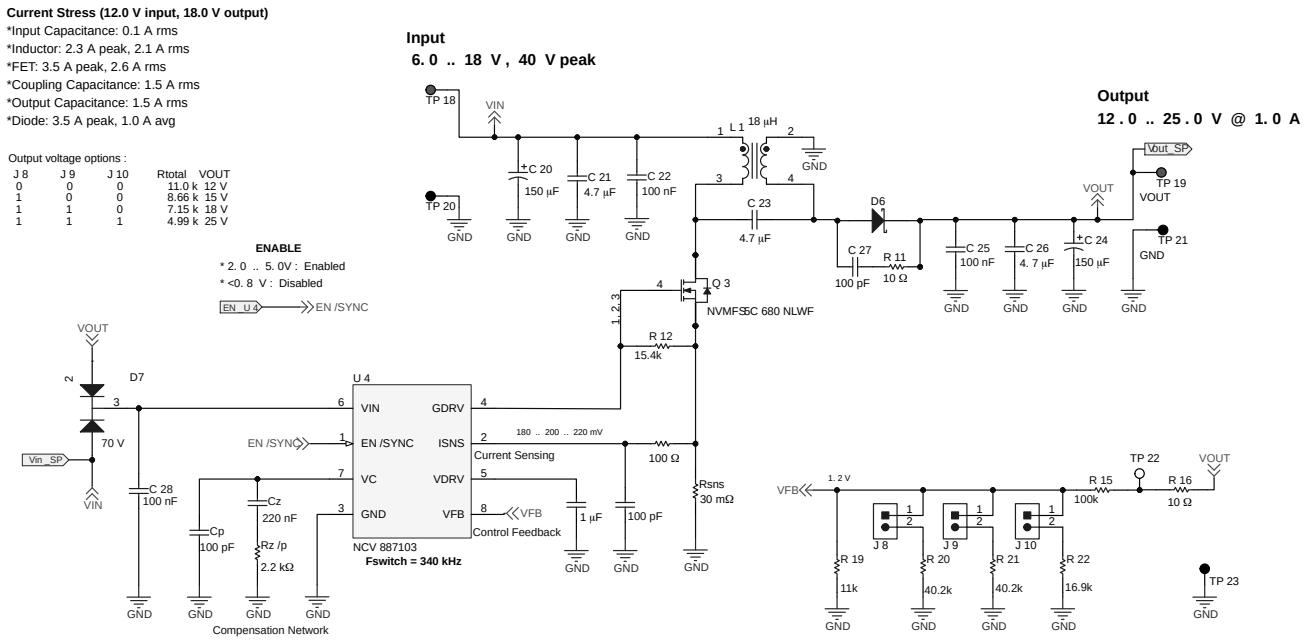

Figure 9. NCV887103 Reference Schematic

According to the datasheet, NCV8871 can handle a continuous input voltage U_{in} of up to 40 V and withstands peak voltage transients of up to 45 V. The Schottky diode (NRVBS360T3G) of the converter has a voltage rating of 60 V and is rated for a continuous current of 3 A.

There are 3 input signals of the NCV8871 that require special attention:

1. ISNS − The current limit threshold voltage (NCV871103 UCL) is max. 200 mV (see Typical Values for the specific NCV8871x variant).

a. A decoupling RC filter consisting of 100 Ω (R14 in series) and 100 pF (C31) is added.

2. VC − The compensation network is tuned for the stable and responsive operation of the switching regulator controller (see Current Mode Control in datasheet).

a. NCV8711 uses 2nd-order control model (Type II formed by two capacitors − C29, C32− and one resistor − R18) for its current mode compensation.

3. VFB − The feedback path consists of a resistor divider. Here a fixed 100 kΩ (R15 − R_{upper}) and a resistor ladder (R_{lower}) are used.

a. Refer to “7. Select Feedback Resistors” in the datasheet. By adjusting these values, the output voltage is modified.

Table 5. FEEDBACK LOOP RESISTANCE (R_{FB}) VS. OUTPUT VOLTAGE (U_{out})

Resistor Values [kΩ]	Total R_{FB} [kΩ]	U_{out} [V]
11.0	11.0	12.0 (min)
11.0, 40.2	8.66	15.0
11.0, 40.2, 40.2	7.15	18.0
11.0, 40.2, 40.2, 16.9	4.99	25.0 (max)

Current Sensing

The Designer needs to identify the boundary load conditions of the SEPIC’s current sensing subsystem to select the shunt resistor (R_{SNS}, see R17 on the schematic). To do this, one shall refer to the values from the SEPIC’s Electrical Characteristics table (provided also in Table 3) to find the minimal threshold voltage ($U_{min\ CL}$) at the current sense pin (ISNS) for which the current limit is triggered. In the case of NCV887103 variant used in this design, it is equal to 180 mV.

The shunt resistor is exposed to the high currents flowing from the input through the primary side of the inductor L1 and the switching node Q3 (NVMFS5C680NLWF). The maximum expected I_{OUT} for each U_{in}−U_{OUT} configuration was summarized in Table 4. We use these values together with the formula below to calculate the expected current at the shunt resistor.

As per Equation (2), maximum current at Q3 MOSFET ($I_{max\ FET\ Q3}$) can be approximated by conjugating the input current increased by the expected worst-case losses at the SEPIC (I’$_{in}$), output current (I_{out}) and L1 inductor’s ripple current ($I_{\Delta L}$). Typically for SEPIC, designers might assume up to 40% extra input current for inductor current ripple $I_{\Delta L}$. According to Figure 16 (U_{OUT} = 25), SEPIC’s regulation loop worst case efficiency η_{wc} = 85%.

The results are summarized in Table 6 per the expected worst-case current at Q3 is 9.5 A.

$$I_{in} = I_{out}\frac{D}{1-D},\ \text{see (1)}$$

$$I'_{in} = \frac{I_{in}}{\eta} =,\ \eta_{wc} = 85\%$$

$$I_{\Delta L} = 30\% \cdot I'_{in}$$

$$I_{max}\ \text{FET Q3} = I'_{in} + I_{out} + I_{\Delta L} \qquad \text{(eq. 2)}$$

Table 6. CALCULATION OF WORST-CASE SENSED CURRENT

Min. Input Voltage $U_{in(min)}$ [V]	Output Voltage U_{OUT} [V]	Max. Output Current I_{OUT} [A]	Resulting Input Current I_{IN} (D= D_{max}) [A]	Max Q3 FET Current $I_{max\ FET\ Q3}$ [A], see (2)
5	12	2.0	5.1	9.9
6	15	1.6	4.2	8.2
8	18	1.3	3.0	6.1
9	25	1.0	2.8	5.5

Example:

I_{OUT} = 1 A was assumed for the purpose of the circuit characterization. The passive (inductor, capacitors, diode) and active components (MOSFET) were selected accordingly. The resulting shunt value was rounded down in case of higher currents occurring thus providing an additional safety margin. More details on remaining component's selection are provided in a separate application note − AND90136.

$$I_{in} = I_{out} \frac{D}{1 - D} = 1\ A \frac{74\%}{1 - 74\%} = 2.85\ A,$$

$$I_{in}^{'} = \frac{I_{in}}{\eta} = \frac{2.85\ A}{95\%} = 3.35\ A,$$

$$\Delta I_L = 40\% \cdot I_{in}^{'} = 1.14\ A,$$

$$I_{max\ FET\ Q3} = I_{in}^{'} + I_{out} + \Delta I_L = 5.49\ A,$$

$$R_{SNS} = \frac{U_{min\ CL\ SEPIC}}{I_{max\ FET\ Q3}} = \frac{180\ mV}{5.5\ A} = 32.8\ m\Omega$$

Selected Shunt value: 30 mΩ.

Coupled Inductor

The value of a SEPIC inductor is calculated using the below formula. One can also refer to "Define Operational Parameters" from the NCV8711 datasheet. The formula considers the SEPIC-specific current ripple at the selected input-output voltage configuration.

$$L = \frac{U_{in(min)} \cdot D_{max}}{\Delta I_L \cdot f_{sw}} \quad \text{(eq. 3)}$$

Example:

Δ_{IL} – calculated above− 1.14 A.

$U_{in(min)}$ − see Table 4− 9 V.

D_{max} – see Table 4− 74%.

f_{sw}− see NCV887103 datasheet − 340 kHz.

$$L = \frac{U_{in(min)} \cdot D_{max}}{\Delta I_L \cdot f_{sw}} = \frac{9\ V \cdot 74\%}{1.14\ A \cdot 340\ kHz} = 17.20\ \mu H$$

Selected Inductor value : 18 μH

Minimal On Time

It is crucial that the following condition is fulfilled. SEPIC's gate pulses shall not be shorter than its minimal allowed value. For NCV887103, $t_{on,min}$ = 90 ns (see datasheet). In this case, the values are much above the minimal ones.

$$t_{on(min)} = \frac{D_{min}}{f_{sw}} > 90\ ns \quad \text{(eq. 4)}$$

Table 7. INDUCTANCE AND t_{ON} SUMMARY FOR ALL TESTED CONFIGURATIONS

Min. Input Voltage $U_{in(min)}$ [V]	Output Voltage U_{OUT} [V]	D_{max} [%]	Inductance L [mH] @ 1 A Output	D_{min} (U_{in} = 18 V) [%]	Min. time ON $t_{on\ min}$ [ns]
5	12	71.6	5.2	41.2	1213
6	15	72.2	7.6	46.5	1367
8	18	70.0	13.6	50.9	1496
9	25	74.0	17.2	58.7	1728

Compensation Network

Crossover frequency is a measure of how quickly the power supply recovers from a step change in the load. The higher the crossover frequency, the faster the step response in time domain. One needs to know the crossover frequency to ascertain the stability margins.

The relative stability of the control loop is analyzed using Gain and Phase measurements with a network analyzer. As the phase margin reduces, the system's behavior becomes more and more oscillatory. For a perfect oscillator the phase margin is 0°− to be associated with a perfect oscillator thus synonymous with unstable. A certain (phase) margin is needed before hitting these oscillations.

The gain margin on the other hand is analyzed by identifying the frequency at which the phase is −180°− which is again a state of a perfect oscillator. The gain at this frequency relative to 0 dB indicates the margin before system enters the oscillations. Such methodology shall assure enough phase and gain margin for the given range of the input-output voltage.

NCV8711 has two internal resistors (after VC input) forming a divider at its compensation network input− R_{esd} = 502 Ω (ESD protection) and R_0 = 3 MΩ (attenuation).

Typically, in a system design with fixed input-output signal requirements, the designer selects the components for the compensation network such that zero, crossover and pole are placed 1 decade apart from each other thus providing just enough bandwidth to amplify the relevant signal and discard all the remaining noise.

In the proposed reference design, the situation is different. The bandwidth of the control loop shall be much wider to support the proposed range of input-output voltages and output currents. To achieve this, the zero frequency f_{z1} is defined as per the aforementioned rule, however the pole f_{p2} is shifted as far to the front as possible. It was found that with C_{P2} = 100 pF the system reacts robustly in all cases with relatively low overall losses− see Efficiency section.

$$f = \frac{1}{2\pi \cdot C \cdot R} \qquad \text{(eq. 5)}$$

Table 8. SELECTED VALUES FOR COMPENSATION NETWORK

	C_{P2} (C32)	C_{Z1} (C29)	$R_{Z/P}$ (R18)
Value	100 pF	220 nF	2.2 kΩ

Example:

The below values are calculated as per equation (5).

- Zero frequency f_{z1} = 340 Hz,
- Crossover frequency f_c = 3.4 kHz.
- Pole frequency f_{p2}= 723 kHz

The compensation network was tuned using a calibrated Omicron Bode Analyzer 100. To verify the correctness of the selected zero and pole values (R_{zp}, C_p, C_z) the loop response of the SEPIC was examined. Additional measurements have been performed to ensure stability overall operating conditions, see Table 9.

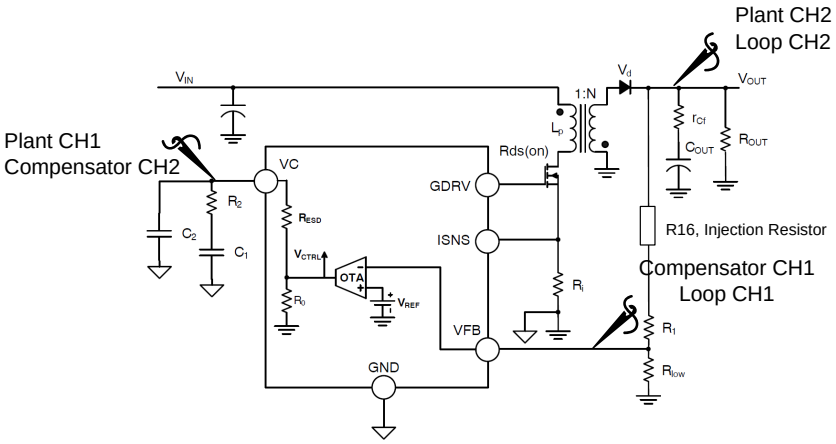

Figure 10. Probe Position for the 3 Types of Frequency Response Measurement

The frequency response measurement can be performed in 4 steps. Refer to test points from Figure 10:

1. *Bode Analyzer calibration − required.*
   Connect the CH1 with CH2 of the analyzer via the injection transformer− the resulting frequency response should remain at 0 dB across the whole measured frequency spectrum.
   Here 100 – 120000 Hz.
2. *Loop response measurement – required.*
   See Figure 11.
   It analyses the overall behavior of the converter, which includes both the compensator and the plant.

a. Here, the frequency sweep signal is injected into the feedback loop (CH1 probe at test point TP22) and measured at the output of the SEPIC (CH2 at Vout test point TP19). Between the two probes an injection resistor (R16, 10 Ω) is placed. Typically, not more than 20 Ω.

3. *Plant response measurement– optional.*
   The plant in a power supply system is the part that converts the input power to the desired output. It includes components like the power stage (e.g., transformers, inductors, capacitors) and the PWM (Pulse Width Modulation) stage. The plant response describes how these components react to changes in input and how they affect the output voltage.

a. To measure it, attach CH2 to TP22 the same way as for the loop response− to TP22− whereas CH1 probe is placed at the VC input of the SEPIC, i.e., compensator network.

4. *Compensator response measurement – optional.*
   The compensator is a control element designed to improve the stability and performance of the power supply. It adjusts the PWM signal to correct any deviations from the desired output. The compensator's response involves the transfer function of the error amplifier and the compensation network, which typically includes resistors and capacitors.

a. To measure it, attach CH1 the same way as for loop response− to TP21-whereas CH2 probe is placed directly at the VFB input, i.e., behind the compensator network.

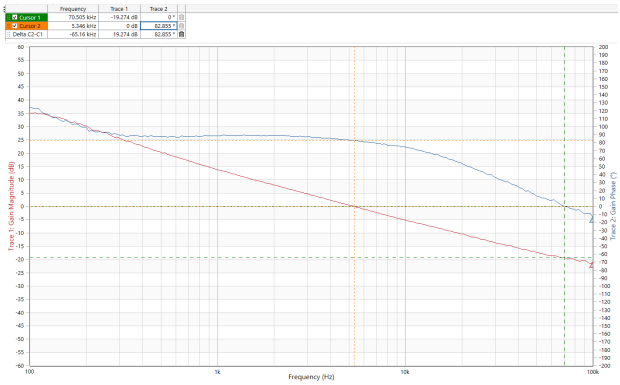

Figure 11. Loop Response over Frequency (Bode Plot) for Input: 12 V − Output Load: 12 V, 1A. See Table 9 for Details

A minimum requirement for a stable loop is typically 60° of phase margin (PM) and −10 dB gain margin. Table 9 reflects the expected behavior where the highest gain and phase margin corresponds to the buck mode (step-down voltage conversion) of the SEPIC− low duty cycle. Conversely, the results show that the system is expected to perform least efficiently in boost mode. Lastly, the slope of the gain at the crossover frequency is expected to decrease ideally by −20 dB per decade. Too rapid change of the slope indicates that the system can hit the oscillations much faster. Overall, a stable loop response across all the tested configurations is assured.

Table 9. FREQUENCY RESPONSE OF NCV887103 SWITCHING REGULATOR

Input [V]	Output [V]	Phase Margin [°]	Gain Margin [dB]	Crossover Freq (f_c) [kHz]
5.0	12.0	68.3	−10.0	2.5
8.0		78.6	−13.4	4.2
12.0		82.9	−19.3	5.3
18.0		88.1	−20.8	6.8
6.0	15.0	73.7	−13.2	2.1
8.0		79.7	−16.1	2.8
12.0		86.4	−17.4	4.0
18.0		88.8	−22.3	4.9
8.0	18.0	80.1	−16.2	1.9
12.0		84.5	−18.4	2.9
15.0		88.5	−18.7	3.5
18.0		88.9	−24.7	3.6
9.0	25.0	79.1	−19.9	1.2
12.0		80.2	−20.0	1.8
15.0		83.3	−23.7	2.1
18.0		87.1	−22.7	2.5

Figure 12 shows the switching node's full load condition. The waveform shows moderate ringing and overshoot, which you would expect from a proper design and layout.

Figure 12. Switching Node (Q3 MOSFET) – Load Step Response @ Input: 12 V, Output Load: 18 V, 1.5 A

Efficiency

Figure 13, Figure 14, Figure 15 and Figure 16 are put side by side to compare the efficiency of the SEPIC in different input-output voltage configurations depending on the load current.

Lower efficiency in the buck mode takes place in the lower current region. Conversely, the boost mode performs well under lower current, but the efficiency drops to 87 % in the upper current region.

In general, efficiency stays between 85 and 91 % across all the configurations. In addition, higher losses tend to be related to the booster mode (step-up voltage conversion), above 0.5 A of the output current threshold. This is linked to higher switching losses of the SEPIC during the continuous conduction mode (CCM).

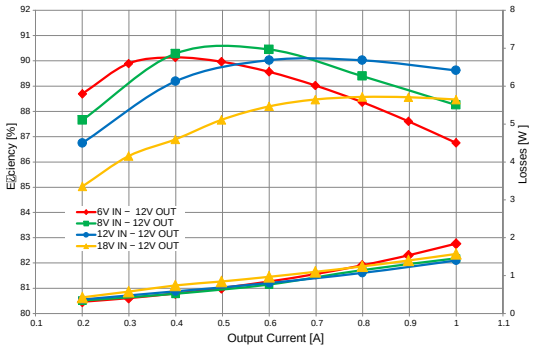

Figure 13. NCV871103 Efficiency & Losses− 12 V Output

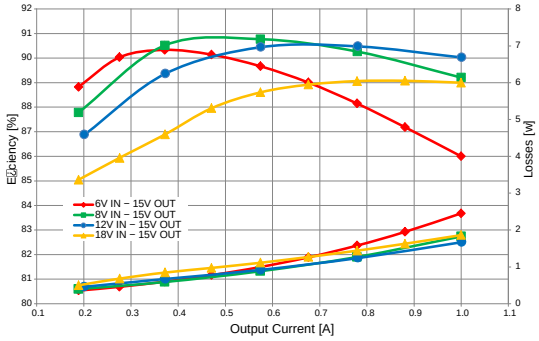

Figure 14. NCV871103 Efficiency & Losses− 15 V Output

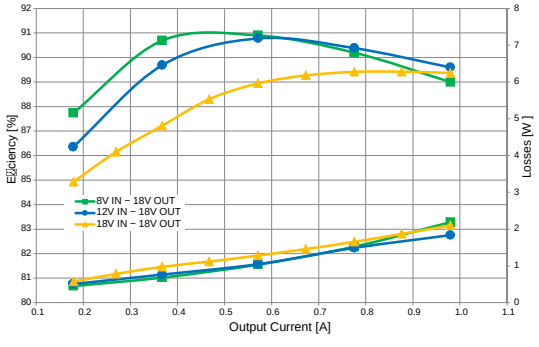

Figure 15. NCV871103 Efficiency & Losses− 18 V Output

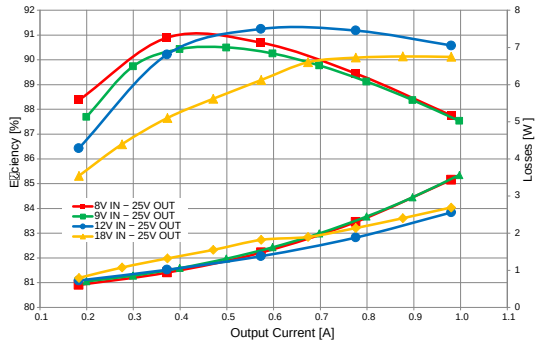

Figure 16. NCV871103 Efficiency & Losses− 25 V Output

Input and Output Ripple

The input ripple from Figure 17 is measured by connecting the probe to the test pins close to the input capacitors of the converter. One can observe the switching noise artifact superimposed onto the sinusoidal input ripple caused by the input current ripple. The ratio of Input and Output ripple's magnitude to the overall signal can be calculated as follows. $U_{peak\ ripple}$ is measured (see Figures below) and put into the provided formula. It is confirmed that the 150 μF input capacitor C20 sees fairly low ripple currents compared to its output counterpart.

$$\text{Ripple [\%]} = \frac{U_{rms\ ripple}}{U_{dc\ signal}}\ 100\% = \frac{U_{peak\ ripple}}{U_{dc\ signal}\sqrt{2}}\ 100\% \quad \text{(eq. 6)}$$

Example:

$$\text{Input Ripple} = \frac{U_{peak\ ripple}}{U_{dc\ input}\sqrt{2}}\ 100\% = \frac{29.3\ \text{mV}}{12\ \text{V}\ \sqrt{2}}\ 100\% = 0.2\%$$

The voltage ripple of the output capacitor is shown on Figure 18. The figure shows a characteristic charge-discharge profile of the 150 μF output capacitor C24. The output ripple factor is calculated as follows:

$$\text{Output Ripple} = \frac{U_{peak\ ripple}}{U_{dc\ output}\sqrt{2}}\ 100\% = \frac{173\ \text{mV}}{12\ \text{V}\ \sqrt{2}}\ 100\% = 1.0\%$$

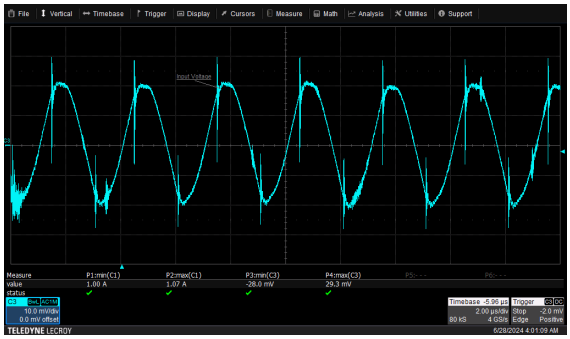

Figure 17. Input Ripple (2 μs/div): SEPIC 12 V IN – 12 V OUT

Figure 18. Output Ripple (2 μs/div): SEPIC 12 V IN – 12 V OUT

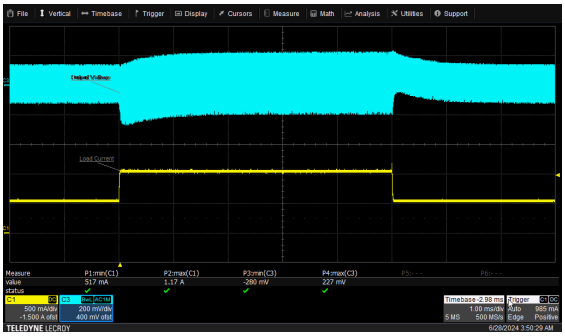

Figure 19. Step Response (1 ms/div): 12 V IN – 12 V, 1 A OUT. Voltage Transients: 400 mV Pk−Pk

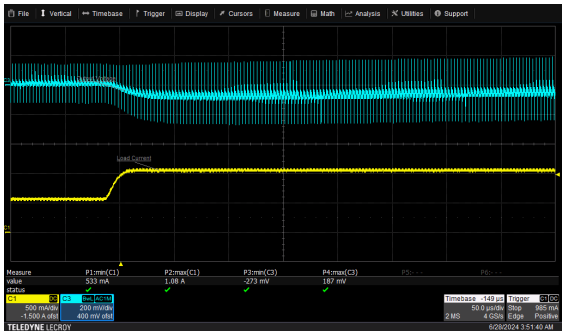

Figure 20. Step Response (50 μs/div): 12 V IN – 12 V, 1 A OUT

Thermal Measurement

Lastly, the test setup for the system's thermal behavior is demonstrated in Figure 21.

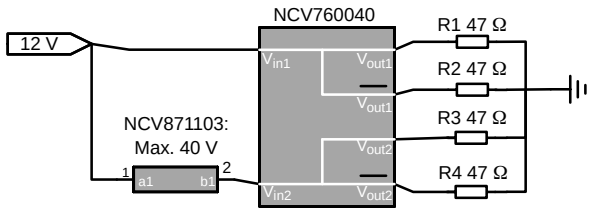

Figure 21. Thermal Response − Test Setup with 4 x 47 Ω

The below calculation demonstrates how to estimate the load distribution of the system. By attaching the resistors like on Figure 21 a cumulative current of 1.57 A is set.

$$I_{Load1} = I_{Load2} = \frac{12\ V}{47\ \Omega} = 255\ mA$$

$$I_{Load3} = I_{Load4} = \frac{25\ V}{47\ \Omega} = 232\ mA$$

$$I_{total} = 1.574\ mA,\ P_{total} = 32.72\ W$$

According to Figure 22 and Figure 23 the temperature of any component does not exceed 46 °C at 22 °C ambient temperature. As it was shown earlier− in the case of maximum current (1.2 A) setting for NCV760040, a minimum of 1.6 A on a single channel is a minimum value required for overcurrent protection to be triggered.

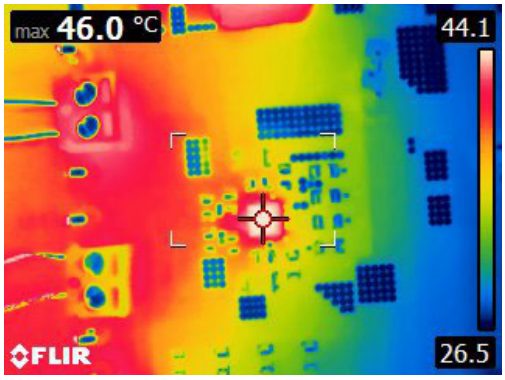

Figure 22. Thermal Measurement − NCV871103, 12 V IN – 12 V OUT, after 1 hour

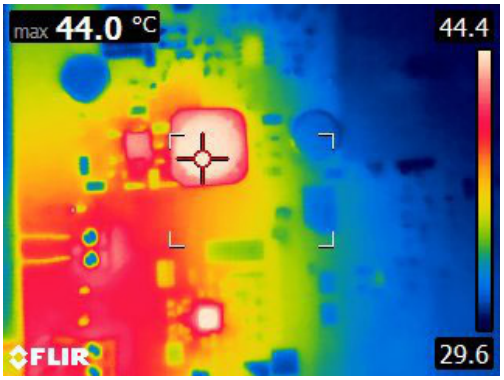

Figure 23. Thermal Measurement − Inductor 18 μH, 12 V IN – 12 V OUT, after 1 hour

Reverse Battery Protection (RBP)

The NCV68061 is designed to replace power rectifier diodes, lowering energy losses and operating well with lower forward voltage. In this reference design it provides protection against reverse current and voltage, which is especially important in battery-connected power supplies. Failing to integrate such protection in the system might lead to the potential damage propagating throughout all the remaining components in the system.

Table 10. NCV68061 PARAMETERS

	Comment	Symb.	Min.	Typ.	Max.	Unit
Input Supply Voltage	See "Maximum Ratings"	U_S	−18	−	45	V
UVLO	Source Voltage	U_{S_UVLO}	3.0	3.25	3.5	V
Quiescent Current	I_G = 0 mA, U_{SD} = 220 mV (Charge Pump active)	I_Q	−	215	295	μA
ON Resistance	During Discharge	R_{DSON}	1	2.2	5	Ω
Gate Current	Typical Peak Value during Discharge	I_{G_disch}	−	1.85	−	A

In any case, NCV68061 requires an external N-MOSFET, such as the NVTFS5C453NL. The ON/OFF state of the MOSFET is controlled by the G pin and depends on the source (S pin) to drain (D pin) differential voltage polarity. If the D pin is connected to the drain pin of the MOSFET (load) then the device becomes an ideal diode controller offering reverse current protection with a minimal voltage drop. By connecting the drain (D) pin to the ground, NCV68061 acts as a reverse (voltage) polarity protection (RPP). To protect the whole circuit from high voltage transients a clamping circuitry is added, as shown in Figure 24.

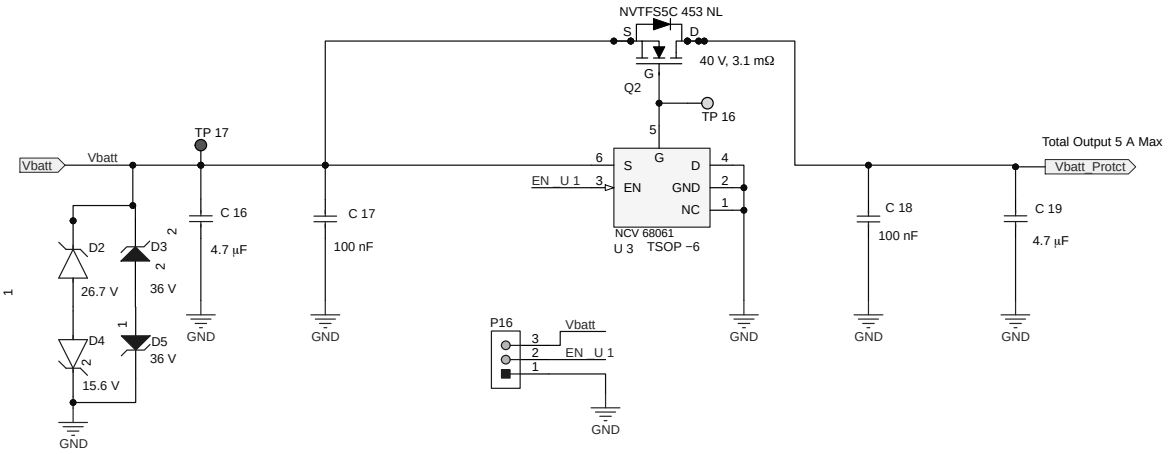

Figure 24. NCV68061 Reference Schematic

PCB Design and Comments

1. Maximal current stress is defined by the components used for the SEPIC. Refer to the schematic for additional comments on the peak and rms ratings.
2. Output voltage is user-configurable via jumpers. Refer to the section below and schematic.
3. In the proposed design load 1 & 2 outputs are supplied directly by the Vbatt input. In order to use the boosted voltage of up to 25 V on all 4 loads, the P5 jumper configuration and reverse battery protection (RBP) should be modified accordingly.
4. NCV760040 requires a specific R3 resistor value at its ADD pin to set its address− this value shall be selected in "I^{2}C Address" field in the GUI to establish the communication.

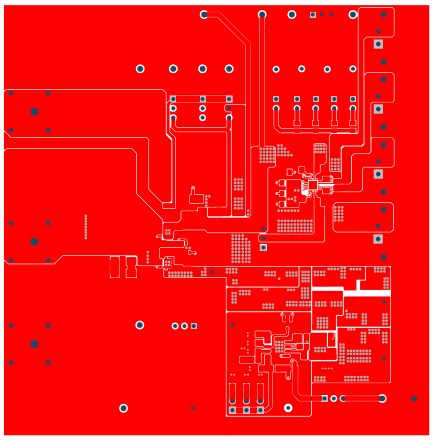

Figure 25. Top Layer

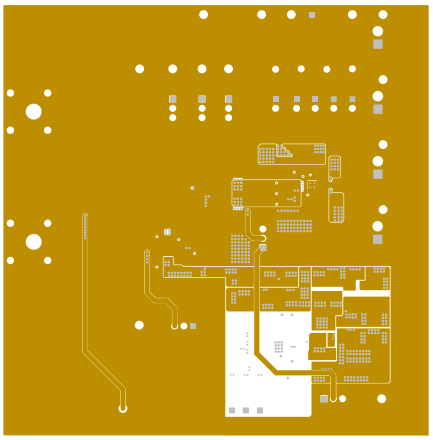

Figure 26. Inner Top Layer

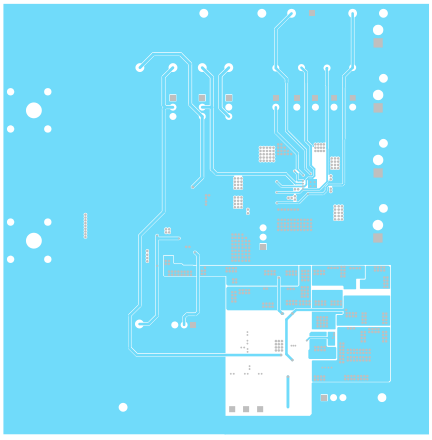

Figure 27. Inner Bottom Layer

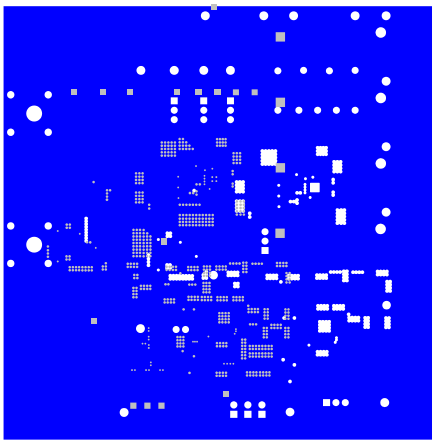

Figure 28. Bottom Layer

Jumper Configuration on the Evaluation Board (EVB)

NCV760040 (Quad HSS)
P1 − power up the controller (V_{dd}) via: • external supply via the J1 connector (EXT_5V) • LDO (NCV4295). Both 3.3 and 5 V variants can be used.
P2 − NCV760040 Enable Signal− EN_U2 comes from: • LDO Power Good Output • External Supply.
P5 – interconnect between controller inputs: • Vin1 (OUT1, OUT2) • Vin2 (OUT3 and OUT4), −and supplies: • SEPIC Output (V_{out_SP}) • External (V_{batt})
P11, P12, P13, P14, P15 − sets the limit of load current limit per channel: • 0.1, 0.2, 0.5, 1.0, 1.2 A (max $I_{outChannel}$).
NCV8711 (SEPIC)
P3 − SEPIC Enable Signal • EN_U4 comes from LDO output (High: 2.4 – 5 V, Low 0 − 0.7 V)
J8, J9, J10 − $V_{Feedback}$ SEPIC V_{out} feedback input • Sets the SEPIC output voltage (V_{out_SP}) via: R20, R21, R22. See Output Voltage Options in the schematic.
P10 – enables external buck−boost controller. • to be connected via TP5 and TP6 pin
NCV68061 (RBP)
P16 – RBP EN pin, deactivates the device.

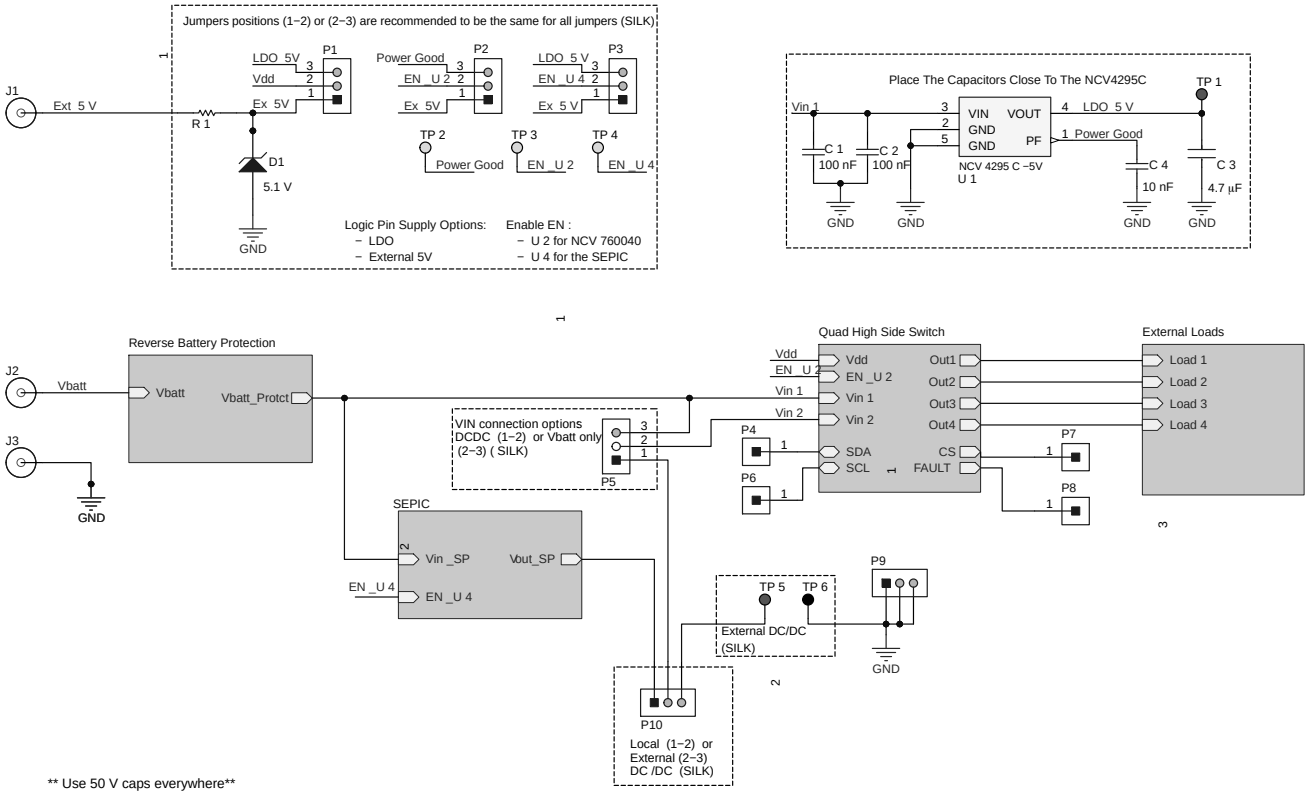

Figure 29. Appendix− Full System Schematic

Table 11. APPENDIX− BILL OF MATERIALS

Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
C1, C2, C6, C8, C9, C10, C11, C12, C13, C22, C25, C28	12	100 nF	GCM21BR71 H104KA37K	Murata	Chip Multilayer Ceramic Capacitors 100 nF, 10%, X7R, 50 Vdc, 0805, 125 °C	0805
C3	1	4.7 μF	GRM31CR71 H475KA12L	Murata	Chip Multilayer Ceramic Capacitors for General Purpose, 1206, 4.7 μF, X7R, 15%, 10%, 50 V	1206
C4	1	10 nF	GCM2195C1H 103JA16D	Murata	Chip Multilayer Ceramic Capacitors, 10 nF, 5%, C0G, 50 Vdc, 0805, 125 °C	0805
C5, C7	2	10 μF	GRM32ER71 H106KA12L	Murata	CAP CER 10UF 50 V, 10% X7R 1210	1210
C16, C19	2	4.7 μF	GRM31CR71 H475KA12L	Murata	Chip Multilayer Ceramic Capacitors for General Purpose, 1206, 4.7 μF, X7R, 15%, 10%, 50 V	1206
C17, C18	2	100 nF	GCM21BR71 H104KA37K	Murata	0.1 μF ±10% 50 V Ceramic Capacitor X7R 0805 (2012 Metric)	0805
C20, C24	2	150 μF	GYA1V151M CQ1GS	Nichicon	CAP, Hybrid Polymer, 150 μF, 35 V, ±20%, 0.027 Ω, SMD	D8xL10 mm
C21, C23, C26	3	4.7 μF	GCM32ER71 H475KA55	Murata	CAP, CERM, 4.7 μF, 50 V, ±10%, X7R, 1210	1210
C27, C31, Cp	3	100 pF	GRM2165C2A 101JA01D	Murata	CAP, CERM, 100 pF, 100 V, ±5%, C0G/NP0, 0805	0805
C30	1	1 μF	GCM21BR71 H105KA03L	Murata	Ceramic Capacitor for Automotive 1 μF ±10% 50VDC X7R 0805 Embossed T/R	0805
Cz	1	220 nF	08055C224JA T2A	AVX Interconnect / Elco	AVX − 08055C224JAT2A − SMD Multilayer Ceramic Capacitor, 0.22 μF, 50 V, 0805 [2012 Metric], ±5%, X7R	0805
D1	1	5.1 V	SZMM5Z5V1 T1G	**onsemi**	Zener Voltage Regulator, 500 mW, 2− Pin SOD−523, Pb−Free, Tape and Reel	SOD− 523−2− 502−01
D2	1	38.9 V	SBJ24A−13− F	Diodes Inc	TVS DIODE 24 V 38.9 V SMB	SMB
D3, D5	2	36 V	SZ1SMB5938 BT3G	**onsemi**	3 W Zener Voltage Regulator, 2−Pin SMB, Pb−Free, Tape and Reel	SMB−2− 403A− 03_H
D4	1	23.2 V	SBJ14A−13− F	Diodes INC	TVS DIODE 14 V 23.2 V SMB	SMB
D6	1	60 V	NRVBS360BN T3G	**onsemi**	Diode, Schottky, 60 V, 3 A, SMB	SMB
D7	1	70 V	SBAV70LT1G	**onsemi**	Diode, Switching, 70 V, 0.25 A, AEC− Q101, SOT−23	SOT−23
J1, J2	2	1000 V	66.9040−22	Stäubli	4 mm Angled Sockets XELW−4 Banana Jack Connector	XELW− 4
J3	1	1000 V	66.9040−21	Stäubli	4 mm Angled Sockets XELW−4 Banana Jack Connector	XELW− 4
J4, J5, J6, J7	4	150 V	ED555/2DS	On− Shore Technology	Terminal Block, 3.5 mm Pitch, 2x1, TH	7.0x8.2x6.5 mm
J8, J9, J10	3	250 V	61300211121	Wurth Elektronik	Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH
L1	1	18 μH	MSD1278− 183ML	Coilcraft	Coupled inductor, 18 μH, 8 A, 0.08 Ω, AEC−Q200 Grade 3, TH	12.3x12, 3 mm

Table 11. APPENDIX− BILL OF MATERIALS (continued)

Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
P1, P2, P3, P5, P9, P10, P16	7	250 V AC, 250 V	61300311121	Wurth Elektronik	THT Vertical Pin Header WR−PHD, Pitch 2.54 mm, Single Row, 3 pins	2.54 mm, 3 pins
P4, P6, P7, P8	4	250 V	61300111121	Wurth Elektronik	THT Vertical Pin Header WR−PHD, Pitch 2.54 mm, Single Row, 1 pins	2.54 mm, 1 pin
P11, P12, P13, P14, P15	5	250 V	61300211121	Wurth Elektronik	THT Vertical Pin Header WR−PHD, Pitch 2.54 mm, Single Row, 2 pins	2.54 mm, 2 pins
Q2	1	40 V, 3.1 mΩ	NVTFS5C453 NL	**onsemi**	N MOSFET NVTFS5C453NL 3.1 mΩ	WDFN− 8 3x3mm
Q3	1	60 V, 27.5 mΩ	NVMFS5C680 NLWF	**onsemi**	MOSFET, N−CH, 60 V, 21 A, SO−8FL	DFN5 5x6 mm
R1	1	100 Ω	CRCW080510 0RFKEAHP	Vishay Dale	Thick Film Resistor, 100 Ω, 1%, 150 V, 0805, 155 °C	0805
R2, R4, R5	3	4.7 kΩ	CRCW08054K 70FKEAHP	Vishay Dale	Thick Film Resistor, 4.7 kΩ, 1%, 150 V, 0805, 155 °C	0805
R3	1	1.24 kΩ	CRCW08051K 00FKEA	Vishay Dale	RES SMD 1.24 kΩ 1% 1/8W 0805	0805
R6	1	3 kΩ	CRCW08053K 00FKEA	Vishay Dale	Thick Film Resistor, 3 kΩ, 1%, 150 V, 0805, 155 °C	0805
R7	1	6.04 kΩ	CR0805−FX− 6041ELF	Bourns	Thick Film Resistor, 6.04 kΩ, 1%, 150 V, 0805, 155 °C	0805
R8	1	15 kΩ	CRCW080515 K0FKEA	Vishay Dale	Thick Film Resistor, 15 kΩ, 1%, 150 V, 0805, 155 °C	0805
R9	1	30 kΩ	CRCW080530 K0FKEA	Vishay Dale	Thick Film Resistor, 30 kΩ, 1%, 150 V, 0805, 155 °C	0805
R10	1	330 Ω	CRCW080533 0RFKEA	Vishay Dale	Thick Film Resistor, 330 Ω, 1%, 150 V, 0805, 155 °C	0805
R11	1	10 Ω	CRCW201010 R0FKEF	Vishay Dale	RES, 10.0 Ω, 1%, 0.75 W, AEC−Q200 Grade 0, 2010	2010
R12	1	15.4 kΩ	CRCW080515 K4FKEA	Vishay Dale	Thick Film Resistor, 15.4 kΩ, 1%, 150 V, 0805, 155 °C	0805
R14, Rz/p	2	100 Ω, 2.2 kΩ	CRCW080547 5RFKTA, RCS08052K2 0 FKEA	Vishay Dale	Thick Film Resistor, 100 Ω, 1%, 150 V, 0805, 155°C, Thick Film Resistor, 2.2 kΩ, 1%, 150 V, 0805, 155 °C	0805
R15	1	100 kΩ	CRCW080510 0KFKEA	Vishay Dale	Thick Film Resistor, 100 kΩ, 1%, 150 V, 0805, 155 °C	0805
R16	1	10 Ω	CRCW080510 R0FKTA	Vishay Dale	Thick Film Resistor, 10 Ω, 1%, 150 V, 0805, 155 °C	0805
R19	1	11 kΩ	CRCW080511 K0FKEA	Vishay Dale	Thick Film Resistor, 11 kΩ, 1%, 150 V, 0805, 155 °C	0805
R20, R21	2	40.2 kΩ	CRCW080540 K2FKTA	Vishay Dale	Thick Film Resistor, 40.2 kΩ, 1%, 150 V, 0805, 155 °C	0805
R22	1	16.9 kΩ	CRCW080516 K9FKEA	Vishay Dale	Thick Film Resistor, 16.9 kΩ, 1%, 150 V, 0805, 155 °C	0805
Rsns	1	30 mΩ	ERJ− B1CFR03U	Panasonic	RES, 0.03, 1%, 2 W, 1020 (wide 2010)	1020 (wide 2010)
TP1, TP5, TP7, TP9, TP11, TP12, TP13, TP14, TP17	9	94 V	5010	Keystone	Test Point, Red, Through Hole, RoHS, Bulk	5010

Table 11. APPENDIX− BILL OF MATERIALS (continued)

Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
TP2, TP3, TP4, TP8, TP10, TP16	6	94 V	5014	Keystone	Test Point, Yellow, Through Hole, RoHS, Bulk	5014
TP6, TP15	2	94 V	5014	Keystone	Test Point, Black, Through Hole, RoHS, Bulk	5011
TP18, TP19	2	94 V	5000	Keystone	Test Point, Miniature, Red, TH	Red Miniature Testpoint
TP20, TP21, TP23	3	94 V	5001	Keystone	Test Point, Miniature, Black, TH	Black Miniature Testpoint
TP22	1	94 V	5002	Keystone	Test Point, Miniature, White, TH	White Miniature Testpoint
U1	1	5 V	NCV4295CSN50T1G	**onsemi**	Off−Battery LDO 5 V 30 mA	TSOP−5
U2	1	40 V	NCV760040	**onsemi**	Quad High−Side Driver 40 V 1.2 A per channel	QFN20 3.5x3.5 mm
U3	1	32 V	NCV68061	**onsemi**	Ideal Diode NMOS Driver	TSOP−6
U4	1	40 V	NCV887103D1R2G	**onsemi**	Automotive Grade Non−Synchronous Boost Controller	SOIC−8

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

◊