FAN53730 Evaluation Board User's Manual

3 A Constant-On-Time Buck Regulator

EVBUM2927/D

This user's manual supports the evaluation kit for the FAN53730. It should be used in conjunction with the FAN53730 datasheet.

Description

The FAN53730 evaluation board is a compact circuit including **onsemi**'s FAN53730, 3 A Constant On Time (COT) buck regulator in a 12−bump Wafer−Level Chip−Scale Package (WLCSP). The device's constant on time topology provides the fastest transient recovery and optimal efficiency vs load due to its variable frequency operation.

The evaluation board provides probe access points to all key circuit nodes so that electrical characteristics can be measured.

FEATURES

Part Number	Output Voltage	VSEL	PG	FCCM	I²C Address	Temperature Range
FAN53730UCX	I²C Controlled	VSET1, VSET2	Yes	Yes	7h'20	−40 °C to 85 °C

Features

- Input Voltage Range: 2.3 V to 5.5 V
- Output Voltage: Programmable from 0.3 V to 2 V
- Pin Selectable Defaults
- Low Quiescent Current: 12 μA
- Internal Soft−Start Limits Input Current During Turn−On
- 2.5 MHz Switching Frequency in Continuous Conduction Operation
- Fault Protection (Input Under Voltage, Short Circuit, Over Current, and Thermal)
- Power Good Output (PG)
- Forced Continuous Conduction Mode (FCCM)
- Audio Reduction Mode Eliminates Audible Tones Due to Switching
- −40 °C to +85 °C Ambient Temperature Range
- This is a Pb−Free Device

Quick Start Connection Guide

1. Connect input power supply (2.30 V – 5.50 V) between banana jacks VIN and GND as shown in Figure 1.
2. Connect the USB Interface POD as shown in Figure 1.
3. Start up the GUI application. If not installed, refer to GUI Installation.
4. Connect external load between banana jacks VOUT and GND as shown in Figure 1.
5. Kelvin connected input and output voltage sense points (VIN_S, VOUT_S) are provided.

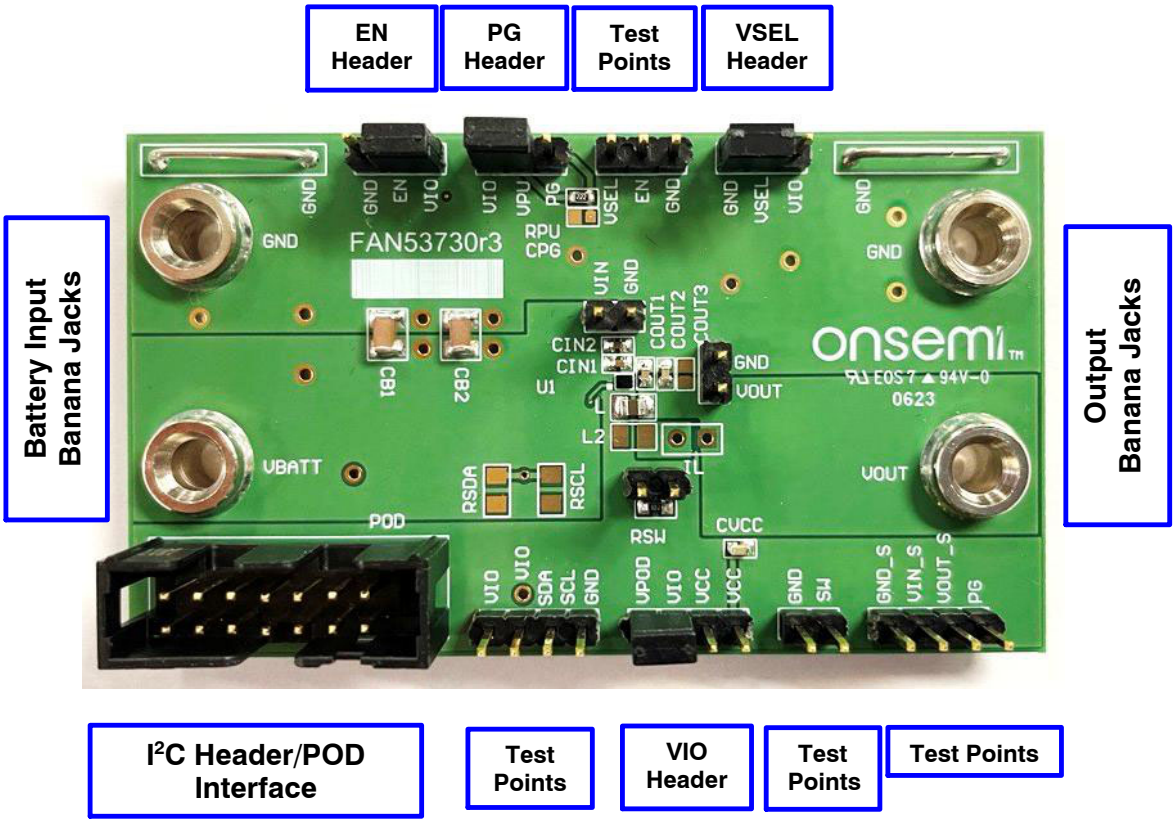

Figure 1. Evaluation Board Connection Diagram

GUI Installation

Installation

a. Run the installer_FAN53730.exe.

b. Follow the steps as shown in the dialog box for setup.

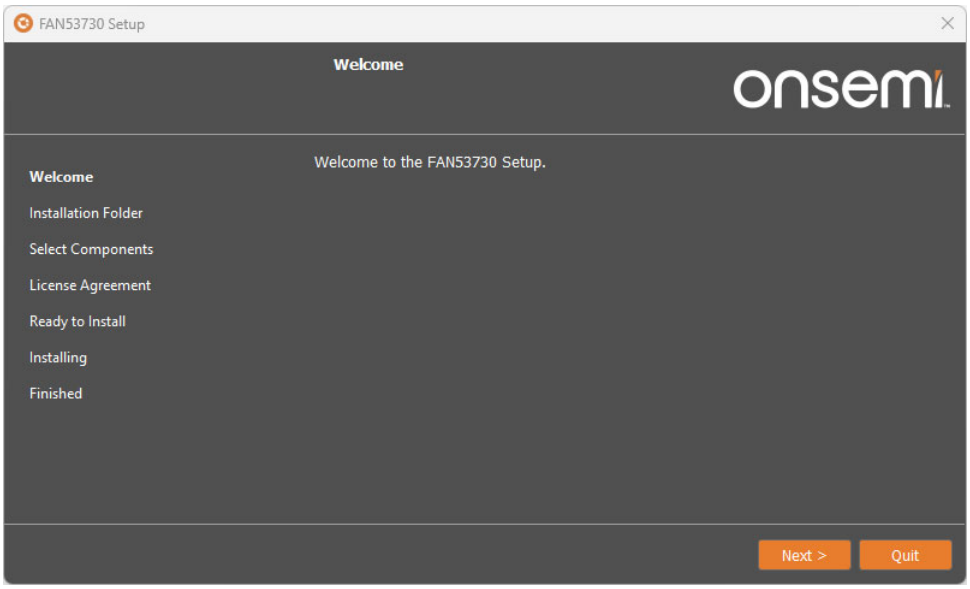

Figure 2. FAN53730 GUI Installation

c. When prompted for Selecting Components, please check the box for PIC POD Driver to install appropriate drivers needed for USB Interface POD.

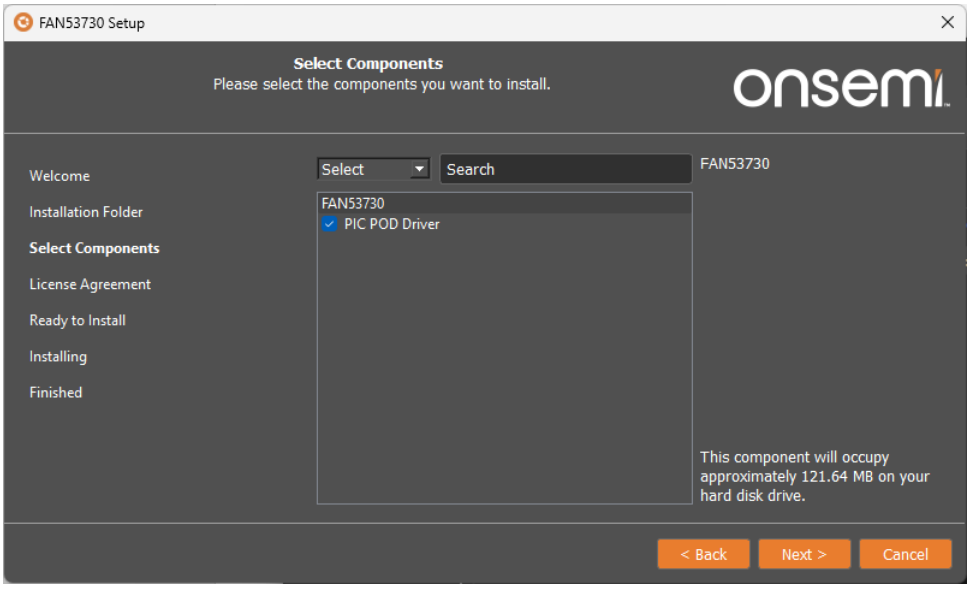

Figure 3. FAN53730 GUI Component Selection

d. Once all steps have been completed, it will start installing the GUI.

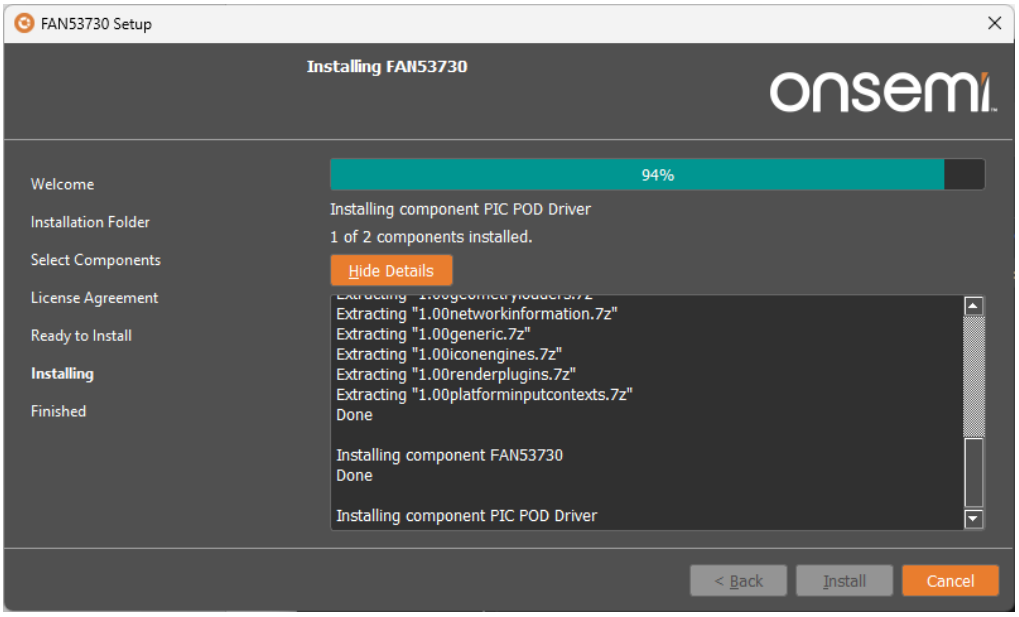

Figure 4. FAN53730 GUI Installation Update

e. Once the installation is complete, FAN53730 GUI will open automatically.
f. You can find the installed GUI at this path: C:\Users*******\onsemi\FAN53730.

g. Below is a screen shot of the FAN53730 GUI that is used to communicate via I^2C.

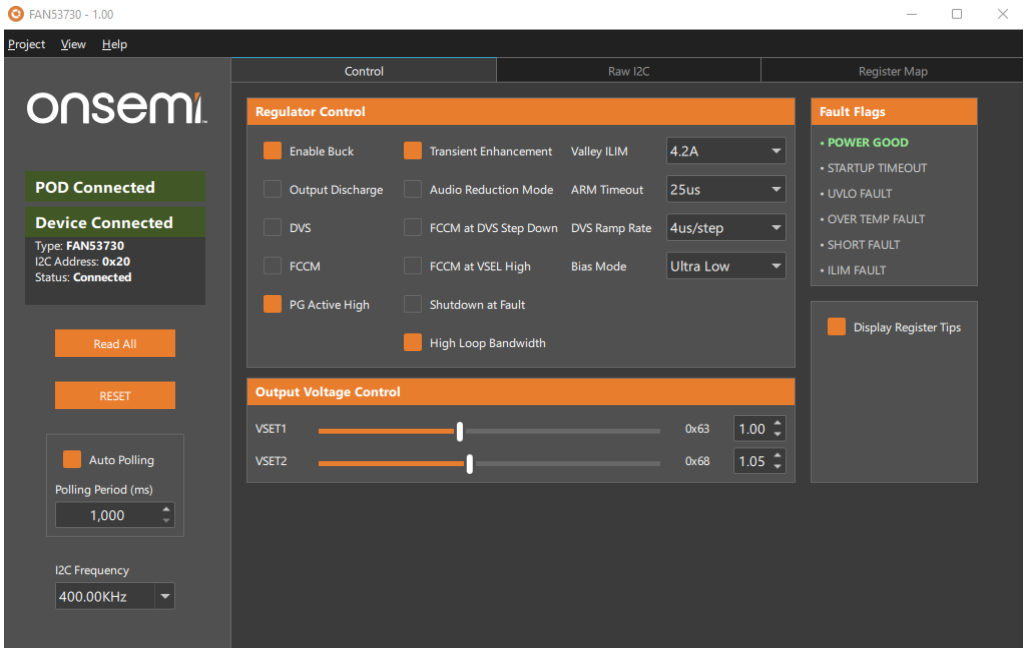

Figure 5. FAN53730 GUI Interface

GUI Overview

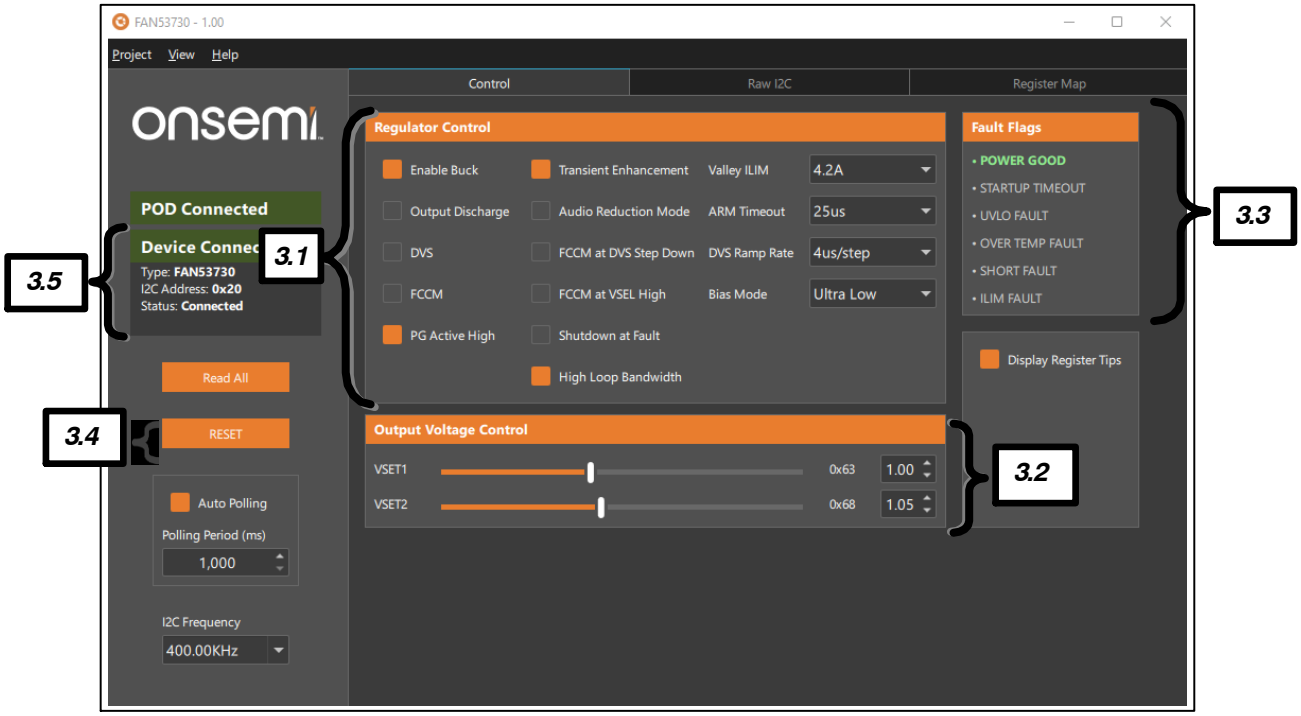

Figure 6. GUI Control Panel

3.1 Regulator Control

a. **Enable** or disable the part.
b. **Output Discharge** enables/disables 100 Ω output discharge resistance in shutdown.
c. **DVS** functionality enables/disables at specified rate in RR_DVS [4:2] in register 0x02.
d. **FCCM** forces the part to operate in CCM regardless of the load current.
e. **PG Active High** changes the polarity of Power−Good Output to active high/low.
f. **Transient Enhancement** enables/disables the extended on−time during V_{OUT} dip.
g. **Audio Reduction Mode** keeps the switching frequency above a programmed target frequency to eliminate audible noise.
h. **FCCM at DVS Step Down** controls whether the FCCM functionality is active when DVS is enabled and the voltage is programmed from high to low.
i. **FCCM at VSEL High** controls whether FCCM will be enabled when VSEL is logic HIGH
j. **Shutdown at Fault** enables the converter to be placed into shutdown if a fault occurs.
k. **High Loop Bandwidth** a bit for control loop high bandwidth adjustment. Set to “0” when VOUT < 0.8 V.
l. **Valley ILIM** sets the limit for the valley of the inductor current.
m. **Arm Timeout** sets the timeout period for Audio Reduction Mode forced switching event.
n. **DVS Ramp Rate** (Dynamic Voltage Scaling) controls the time per step (μs) during the slewing of the output voltage when a new target voltage is set. The converter will increment through each voltage set−point (10 mV/step) until the new target voltage is reached.
o. **Bias Mode** sets the converters ability to shutdown various blocks to achieve low quiescent current vs. output accuracy and response time. The I2C controlled device has three programmable bias mode options (High Bias, Low Bias, Ultra Low Bias Mode).

3.2 Output Voltage Control

a. Output voltage settings for different VSEL levels. User can control values of output voltage either by sliders or by pressing left & right arrow keys from keyboard.
b. Limits output voltage range through values defined by registers 0x04 and 0x05 for VSET1 and VSET2, respectively.
c. If the user enters VOUT values that don’t meet MIN ≤ VOUT ≤ MAX criteria, a warning message or error message (red outline on VOUT) will be displayed.

3.3 Status and Fault−Flags

a. Interrupts or Faults are shown with Red when the bit is HIGH
b. The interrupt flags on the GUI remain asserted (red) until the fault has been cleared.

3.4 Soft Reset

Soft Reset resets the device to its default register values.

3.5 Device Communication

Displays the connection status and I2C address of the device.

Register Map Panel

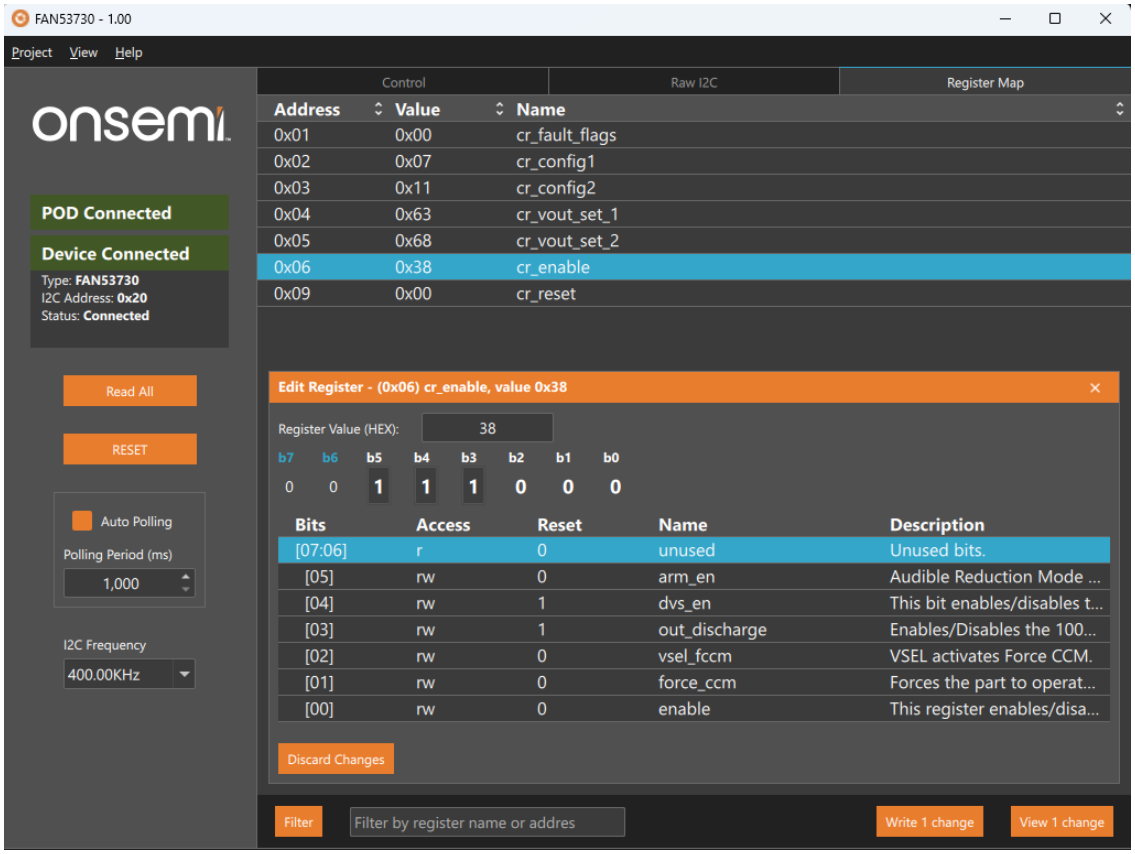

Figure 7. GUI Register Map Panel

Register Map allows control of individual bits of each Register

Edit Register Window: By double clicking on each Register, the “Edit Register” window will pop−up. Register value can be changed from this window

Discard Changes: This option will revert the changes made by the user to the current register.

Write # changes: This option will write all registers changed from the previous settings.

View # changes: This option will allow user to see what changes have been made from the last set of register settings and then write all the changes together.

Raw I2C Panel

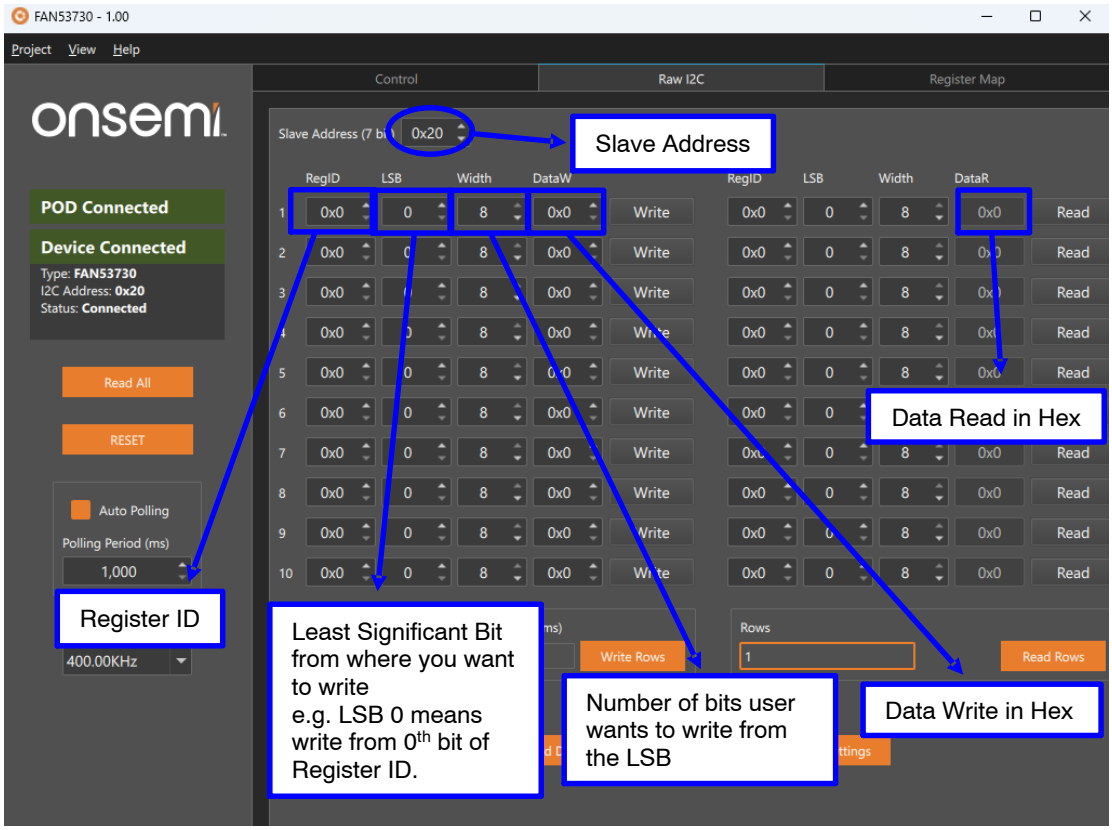

Figure 8. GUI Raw I2C Panel

Raw I2C Panel allows the user to write to or read from the known Slave Address with Hex values of data & Register info.

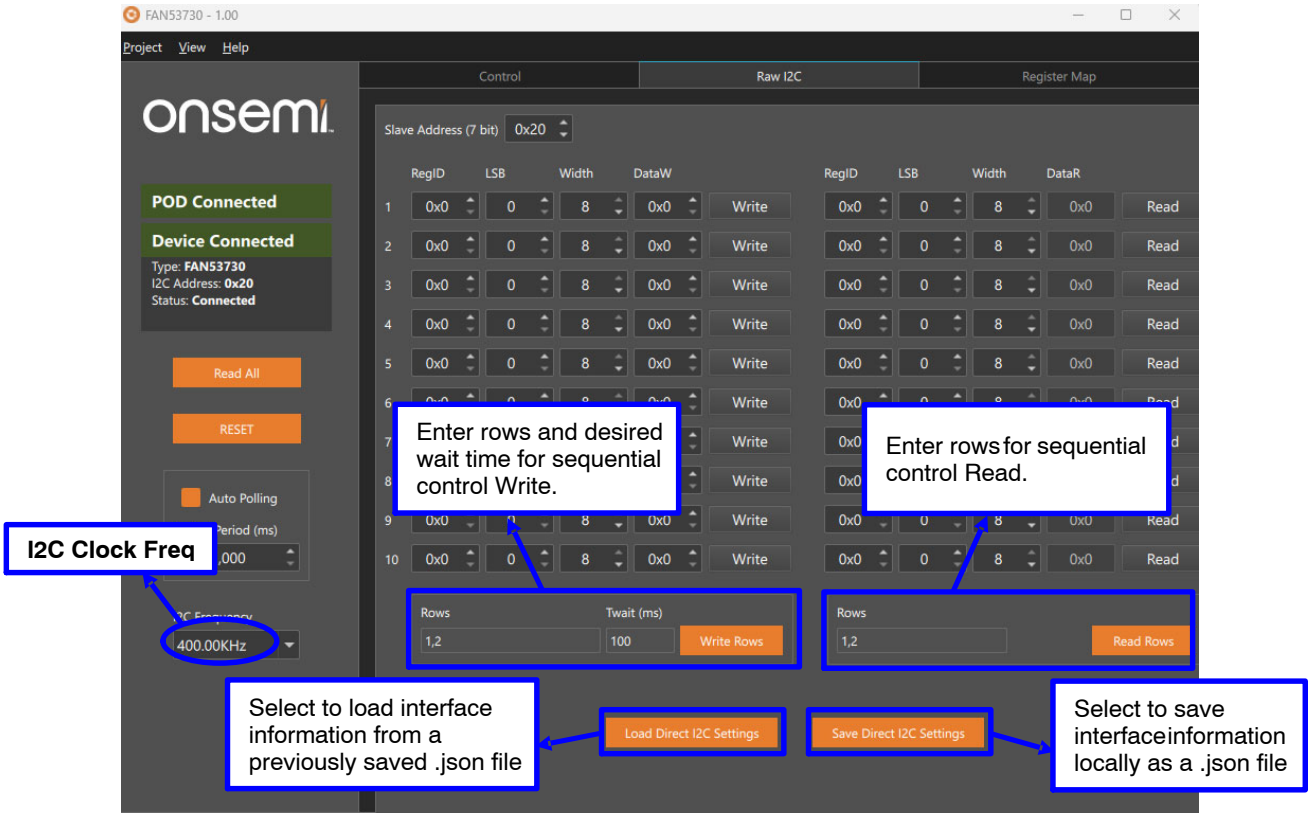

Figure 9. GUI Raw I2C Panel

GUI has features to select I2C Clock Frequency, write/read registers sequentially, and save/load complete settings to/from .json file.

Communication Error: If Slave−Address is not correct or communication with respective Slave Address fails it will give error on Write or Read as shown. Please ensure correct Slave Address is provided and try again.

Schematic

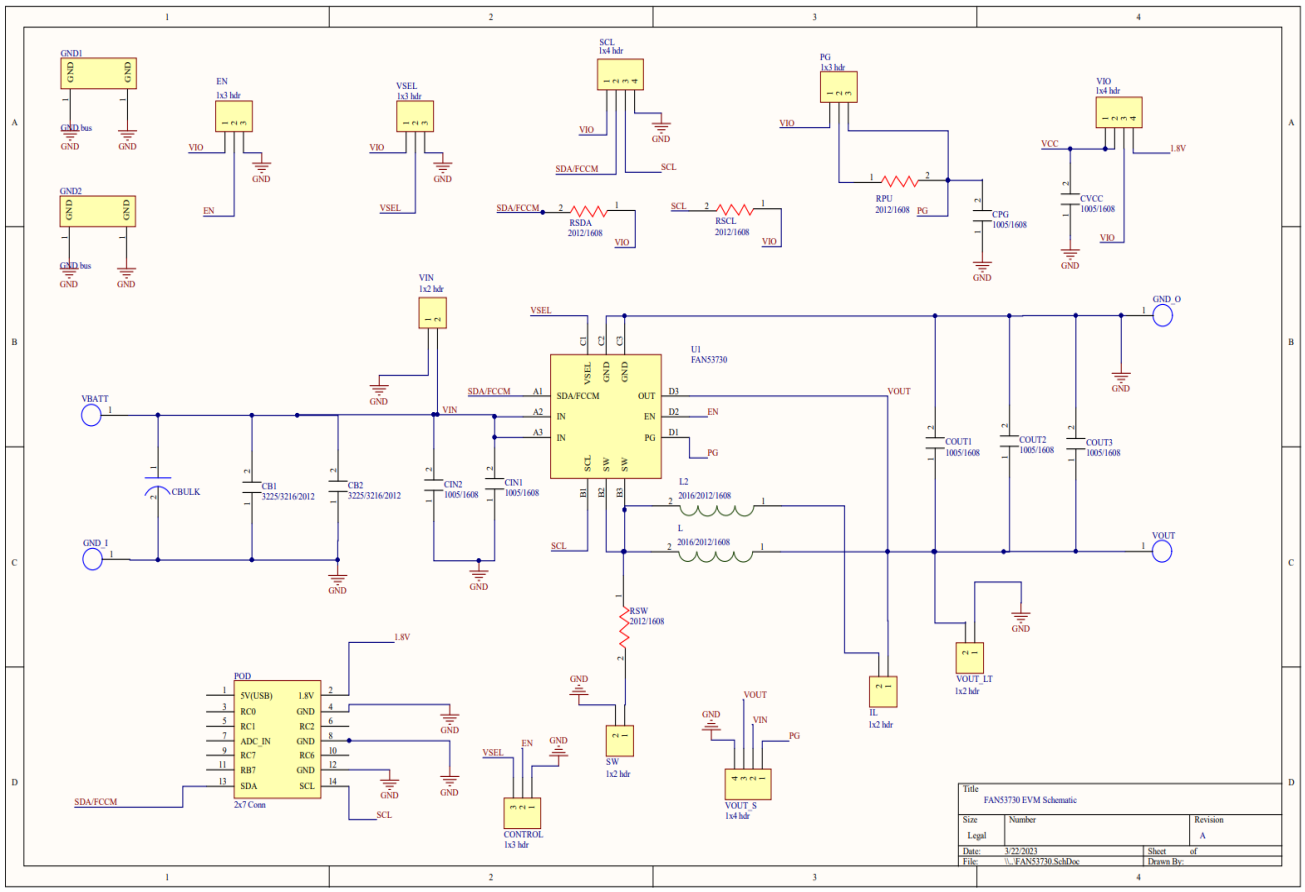

Figure 10. Evaluation Board Schematic

BILL OF MATERIALS

Component	Description	Part Number	Manufacturer	Value	Rating	Size(EIA)
CIN1/CIN2	Input capacitor	GRM155R61A475MEAA#	Murata	4.7 μF	10 V	0402
CB1/CB2	Input capacitor	GRM31CR61A476KE15#	Murata	47 μF	10 V	1206
COUT1/COUT2	Output capacitor	GRM158R60J226ME01#	Murata	22 μF	6.3 V	0402
L	Power inductor	MCHK2012TR24MKG OR LSCNE2012HKTR24MD		Taiyo Yuden	0.24 μH, 4.8A DC	0805
RSW	1 kΩ	RC0603JR−071KL	YAGEO	1 kΩ	1/10 W	0603
COUT3	Output capacitor	GRM158R61A226ME15#	Murata	22 μF	6.3 V	0402
POD	14 pin plug for I2C	MHC14K−ND	3M			14 pin, 100 mil, dual row
CVCC	Bypass for ext. VCC	GRM155R61A475MEAA#	Murata	4.7 μF	10 V	0402
CPG	Bypass capacitor for PG Output	Various	Various	1 nF	10 V	1005/1608 (hybrid)
VBATT, VOUT, GND	Banana jack plugs	575−4	Keystone			7.92 mm
GND, GND	Ground straps	Various	Various	18AWG		18AWG,Solid bare wire
3 x 4−pin 4x 3−pin 3 x 2−pin 2 x 2−pin GND	Various headers			100 mil L.S.		
RSCL, RSDA	Pull−up resistors for SCL & SDA	CRCW06032k20JNEA	Vishay	2.2 kΩ	1/10 W	0603 (Not Populated)
RPU	PGOOD and I2C pull−ups	CRCW06032k20JNEA	Vishay	2.2 kΩ	1/10 W	0603

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales