Isolated Single Channel Gate Driver Evaluation Board User's Manual

NCP51152 EVBUM

Introduction

This user guide supports the evaluation board for the NCP51152. It should be used in conjunction with the NCP51152 datasheets as well as **onsemi**'s application notes and technical support team. Please visit **onsemi**'s website at www.onsemi.com.

This document describes the proposed solution for an isolated single channel gate driver using the NCP51152 family. This user's guide also includes information regarding operating procedures, input/output connections, an electrical schematic, printed circuit board (PCB) layout, and a bill of material (BOM) for the evaluation board.

These evaluation boards can be used to evaluate:

- NCP51152xyDR2G
- NCV51152xyDR2G

Description

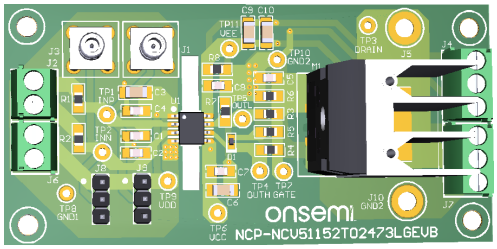
The NCP51152 is a family of isolated single−channel gate driver with 4.5 A / 9 A source and sink peak current respectively. They are designed for fast switching to drive power MOSFETs, and SiC MOSFET power switches. The NCP51152 offers short and matched propagation delays. The NCP51152xA provides a split output that controls the rise and fall times individually. The NCP51152xB has its V_{CC} UVLO referenced to GND2 to get a true UVLO.

The NCP51152 is available in a 4 mm SOIC−8 package and can support isolation voltage up to 3.75 kV_{RMS}.

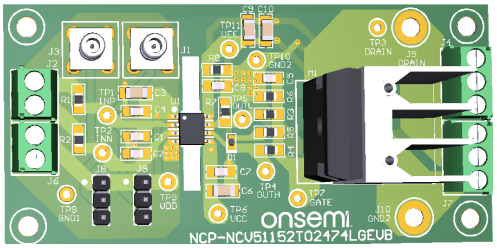
The NCP51152 offers other important protection function such as independent under−voltage lockout for both−side driver.

Key Features

- Feature Options
  - Separated Outputs (OUTH, and OUTL) for only Variant A
  - Wide Bias Voltage Range including Negative V_{EE} and V_{CC} UVLO Referenced to GND2 for only Variant B
- 3 V to 20 V Input Supply Voltage
- Output Supply Voltage from 6.5 V to 30 V with 6 V and 8 V for MOSFET, 12 V and 17 V for SiC, Threshold.
- 4.5 A Peak Source, 9 A Peak Sink Output Current Capability
- Minimum CMTI of 200 V/ns dV/dt
- Propagation Delay Typical 36 ns with
  - 5 ns Max Delay Matching
- Gate Clamping during Short Circuit
- Available Package Footprint
  - Type−A : TO−3P, TO−247, D−PAK, and D2PAK
  - Type−B : TO−247−4L
  - Type−C : D2PAK−7L



Type−A



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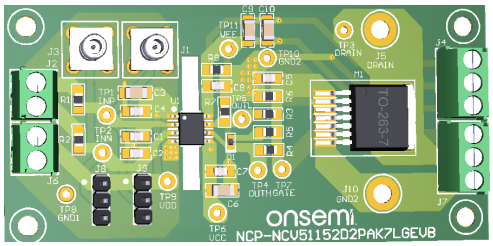
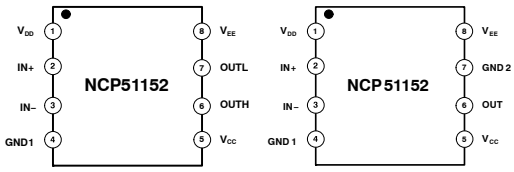


Type−C

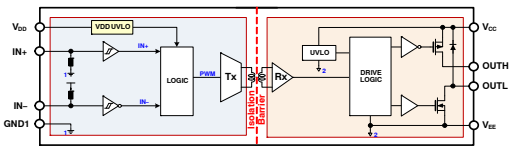
Figure 1. Evaluation Board Picture

PIN CONNECTIONS

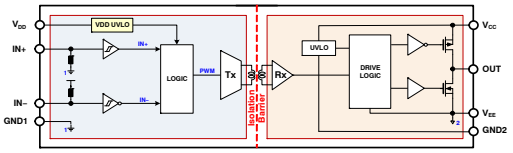


Variant A Variant B

FUNCTIONAL BLOCK DIAGRAM



(a) Separated Output (Variant A)



(b) V_{CC} UVLO Referenced to GND2 and external negative bias (Variant B)

EVALUATION BOARD OPERATION

This section describes how to operate the NCP51152 family evaluation board (EVB). Make external connections to the NCP51152 EVB using either the installed test−points or by installing wires into the connectors. The main connections that must be made to the EVB are the analog supply voltage, input signal, and output load and monitoring equipment.

Features

- Evaluation board for the NCP51152 product family in the narrow body (4 mm) SOIC−8 package.
- 3 V to 20 V Input Supply Voltage
- Output Supply Voltage from 6.5 V to 30 V with 6 V and 8 V for MOSFET, 12 V and 17 V for SiC, Threshold.
- 4.5 A and 9 A source/sink current driving capability
- TTL−compatible inputs and allowable input voltage up to V_{DD} with for IN+, and IN− pins
- 3−position header with for IN+, and IN− pins
- Support to test with MOSFETs, and SiC MOSFETs with connection to external power stage

Power and Ground

NOTE: Connecting the all power supplies in reverse polarity (backwards) will instantly device when power is turned on and device damage can result.

The primary side of the EVB (V_{DD}) operates from a single 3 V to 20 V power supply and connected via J6. Test point (TP9) is available for monitoring the primary power supply. The EVB provides connections for evaluating the output side (V_{CC}, V_{EE}) with bipolar power supply from a minimum 6.5 V to maximum 30 V with respect to V_{EE} pin.

V_{CC} and V_{EE} can be monitored with respect to GND2 (TP10) via TP6 and TP11, respectively.

The V_{CC} pin should be bypassed with a capacitor with a value of at least ten times the gate capacitance of the power device, and over 100 nF and located as close to the device as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is necessary. We had recommends using at least 2 capacitors; an over 100 nF ceramic surface−mount capacitor, and another a tantalum or electrolytic capacitor of few microfarads added in parallel (e.g. C6, C7, C9 and C10).

Input and Output

1. Connection of primary−side power supply to the V_{DD} and GND1 pins connector **[J6−1, and J6−2]**.
2. Connection of secondary−side power supply to the V_{CC} and GND2 pins connector **[J4−1, and J4−2]**.
3. Connection of secondary−side power supply to the V_{EE} and GND2 pins connector **[J4−3, and J4−2]**.
4. Connection of non−inverting input signal (IN+) to the SIGNAL connector **[J2−1, or J1]**.
5. Connection of inverting input signal (IN−) to the SIGNAL connector **[J2−2, or J3]**.

Configuration of Evaluation Board

The NCP51152 have different output stages of the variant A and B. Therefore, EVBs configuration setting is required to select variant A or B as shown in Table 1.

- Separated Outputs (OUTH, and OUTL) for Variant A
- Wide Bias Voltage Range including Negative V_{EE} and V_{CC} for Variant B

Table 1. EVB CONFIGURATION SETTING FOR VARIANT A AND B

Type	PIN7	R3	R5	R7	R8	C8
NCP51152xA	OUTL	3.3 Ω	DNP	DNP	0 Ω	DNP
NCP51152xB	GND2	DNP	3.3 Ω	0 Ω	DNP	470 nF

Evaluation Board Jumper Setting

Table 2. EVB JUMPER SETTING

Jumper	Jumper Setting Options for Input Signals (IN+ & IN−)		Default Setting
J9−IN+ (INP)	Option1	Jumper not installed, IN+ signal provided by external signal and this pin is default LOW if left open	Option1
	Option2	Jumper on J9−INP−2 and J9−INP−3 set IN+ for LOW state	
	Option3	Jumper on J9−INP−2 and J9−INP−1 set IN+ for HIGH state	
J8−IN− (INN)	Option1	Jumper not installed, IN− signal provided by external signal and this pin is default HIGH if left open	Option2
	Option2	Jumper on J8−INN−2 and J8−INN−3 set IN− low for LOW state	
	Option3	Jumper on J8−INN−2 and J8−INN−1 set IN− high for HIGH state	

Evaluation Board Setting before Power Up

1. If the ENABLE mode is used , IN− pin (PIN3) should be connected to GND1(PIN4) through a wire−bridge between pin 2 and pin 3 of J8.
2. If using the DISABLE mode, should be connect IN− pin (PIN3) to V_{DD} pin (PIN1) through a wire−bridge between pin 1 and pin 2 of J8 or this pin is default HIGH if left open.

Bench Setup

The bench setup diagram includes the function generator, power supplies and oscilloscope connections.

Follow the connection procedure below and use Figure 2 as a reference.

- Make sure all the output of the function generator, power supplies are disabled before connection.
- Function generator channel−B channel (CH2) applied on IN+ (J1 or J2 pin−1) ↔ TP1 as seen in Figure 2.
- Function generator channel−A channel (CH1) applied on IN− (J3 or J2 pin−2) ↔ TP2 as seen in Figure 2.
- Power supply #1: positive node applied on J6 pin−1 (TP9), and negative node applied on J6 pin−2 (TP8).
- Power supply #2: positive node applied on J4 pin−1 (TP6), and negative node connected directly to J4 pin−3 (TP11) with respect to GND2 pin (J4−2 & TP10).
- Oscilloscope channel−A probes TP1 (IN+) ↔ TP8 (GND1), smaller measurement loop is preferred
- Oscilloscope channel−B probes TP2 (IN−) ↔ TP8 (GND1), smaller measurement loop is preferred.
- Oscilloscope channel−C probes TP7 (GATE) ↔ TP10 (GND2), smaller measurement loop is preferred.

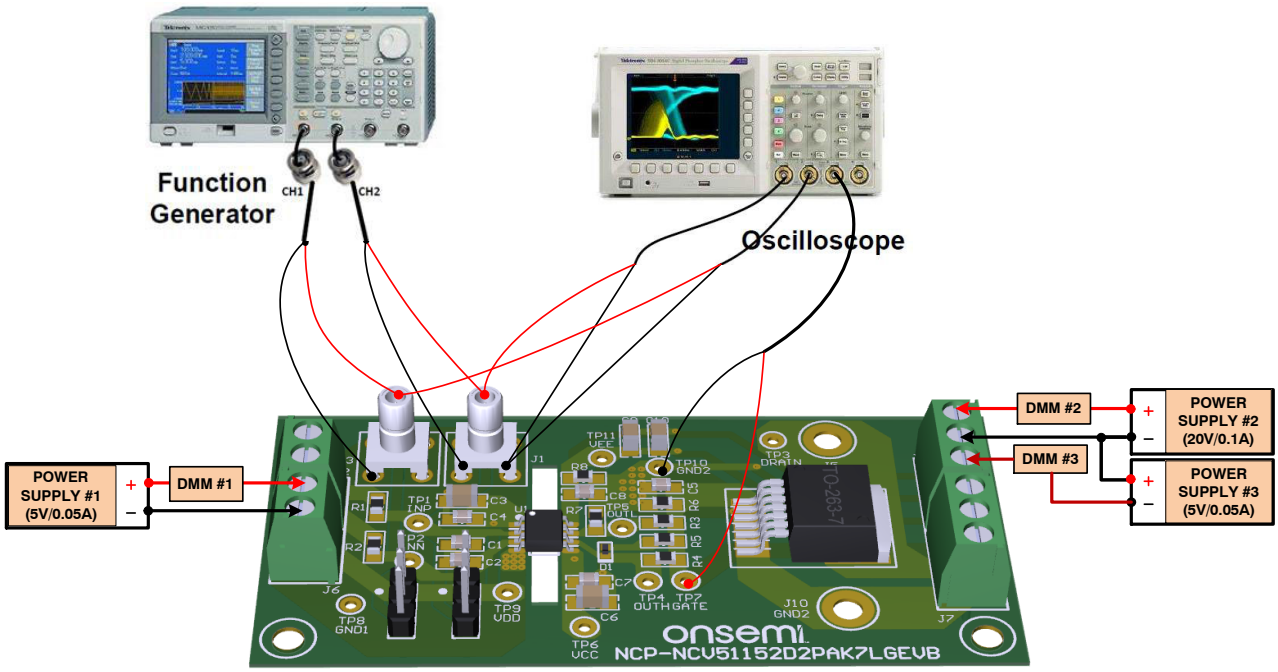
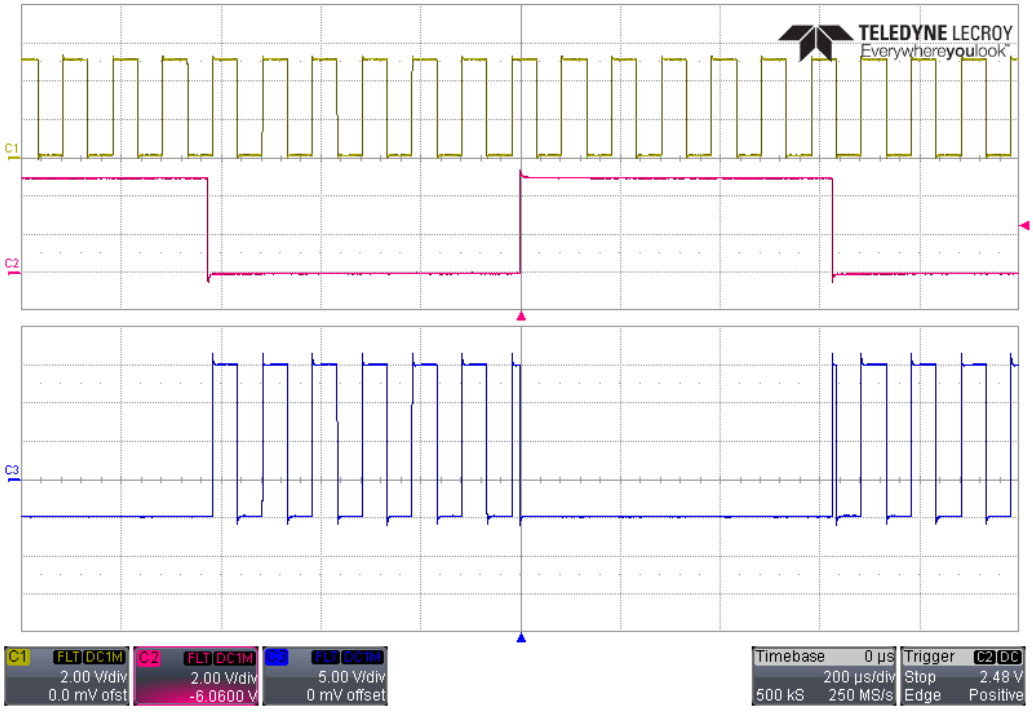


Figure 2. Bench Setup Diagram and Configuration

Power−Up and Power Down Procedure

Power (V_{DD}, V_{CC} & V_{EE}) Up Procedure

1. Enable power supply through pin1 of J6 V_{DD} connector in primary−side
2. Enable power supply through pin1 of J4 V_{CC} connector in secondary−side
   Measure the quiescent current of V_{CC} on DMM2 ranges from 0.5 mA to approximately 1.0 mA if everything is set correctly;
3. Measure the current of V_{EE} with respect to GND2 pin on DMM3 if everything is set correctly;
4. Enable the function generator, two−channel outputs: channel−A for IN− and channel−B for IN+ ;
5. There will be:
   a. Stable pulse output on the channel−A, channel−B, and channel−C in the oscilloscope
   b. Scope frequency measurement is the same with function generator output;
   c. DMM #2 read measurement results should be around 3 mA ± 1 mA under no load conditions.



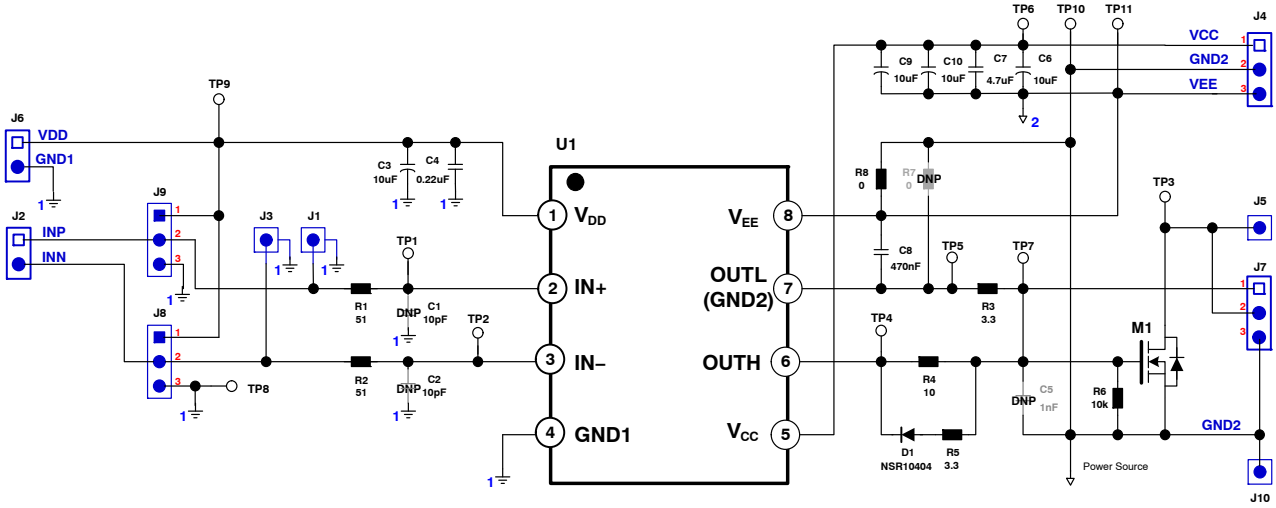
CH1: IN+, CH2: IN-, and CH3: OUT_GND2

Figure 3. Experimental Waveforms of Input to Output

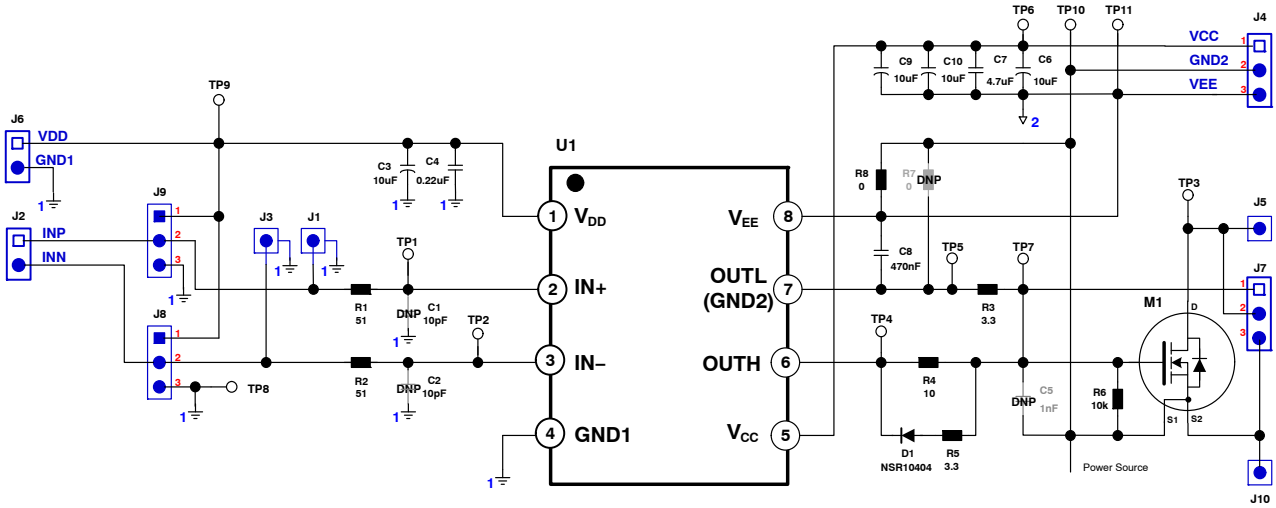
Power (V_{DD}, V_{CC} & V_{EE}) Down Procedure

1. Disable function generator
2. Disable power supply of V_{CC} and V_{EE} in secondary−side
3. Disable power supply of V_{DD} in primary−side
4. Disconnect cables and probes

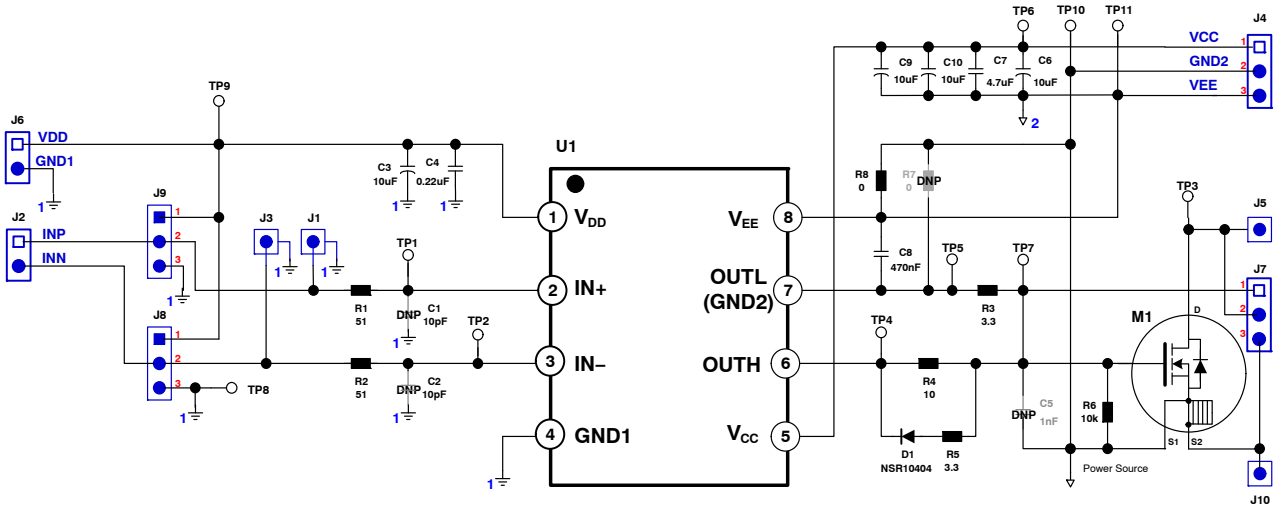
Figure 4 shows the NCP51152 application schematic of each evaluation board to cope with various package types.



(A) Schematic of Type−A for TO−3P, TO−247, and TO−252 (D−PAK), and TO−263 (D2PAK) Package



(B) Schematic of Type−B for TO−247−4L Package



(C) Schematic of Type−C for D2PAK−7L Package

Figure 4. Typical Application Schematic of NCP51152

List of Test Point

Table 3 shows the test point list of NCP51152 for an evaluation board (EVB).

Table 3. LIST OF TEST POINT

TP	Reference	Description
TP1	INP	Non−inverting Logic Input with internal pull−down resistor to GND1
TP2	INN	Inverting Logic Input with internal pull−up resistor to V_{DD}
TP3	DRAIN	Drain of switch
TP4	OUTH	Gate Drive Pull−up Output (Source Output)
TP5	OUTL	Gate Drive Pull−down Output (Sink Output)
TP6	VCC	Positive Output Supply Rail
TP7	GATE	Gate of switch
TP8	GND1	Ground Input−side. (all signals on input−side are referenced to this pin)
TP9	VDD	Input−side Supply Voltage. It is recommended to place a bypass capacitor from V_{DD} to GND1.
TP10	GND2	Gate−drive common pin. Connect this pin to the MOSFET source. V_{CC} UVLO threshold referenced to GND2.
TP11	VEE	Negative output supply rail

Electrical Specifications

Table 4 shows the recommended operating conditions of NCP51152 for an evaluation board.

Table 4. ELECTRICAL SPECIFICATIONS

Rating		Symbol	Min.	Max.	Unit
Power Supply Voltage – Input side		V_{DD}	3.0	20	V
Power Supply Voltage – Driver side	6−V UVLO Version	V_{CC}	6.5	30	V
	8−V UVLO Version		9.5	30	V
	12−V UVLO Version		13.5	30	V
	17−V UVLO Version		18.5	30	V
Negative Supply Voltage for only Variant B (NCP51152xB)		VEE – GND2	−15	0	V
Logic Input Voltage at pins IN+, and IN−		V_{IN}	0	V_{DD}	V
Ambient Temperature		T_A	−40	+125	°C
Junction Temperature		T_J	−40	+125	°C
Common Mode Transient Immunity		CMTI	200		kV/μs

Bill of Material (BOM)

Table 5 shows the bill of material (BOM) of NCP51152 for an evaluation board.

Table 5. BILL OF MATERIAL

Reference	Qty	Description	Value	Footprint	Manufacturer
U1	1	Gate driver	NCP51152	8−SOIC−NB	**onsemi**
D1	1	Diode	US1MFA	SMB/DO214AA	**onsemi**
R1,R2	2	Resistor	51 Ω	SMD 0805W	Rohm
R3 ,R5	2	Resistor	3.3 Ω	SMD 0805W	Rohm
R4	1	Resistor	10 Ω	SMD 0805W	Rohm
R6	1	Resistor	10 kΩ	SMD 0805W	Rohm
C1, C2	2	Capacitor, Ceramic	10 pF, 50 V	SMD 0805W	Yageo
C3 , C6, C9, C10	4	Capacitor, Ceramic	10 uF, 50 V	SMD 3216	Yageo
C4	1	Capacitor, Ceramic	0.22 uF, 50 V	SMD 3216	Yageo
C7	1	Capacitor, Ceramic	4.7 uF, 50 V	SMD 0805W	Yageo
C8	1	Capacitor, Ceramic	For only NCP51152xB	SMD 0805W	Yageo
C5	1	Capacitor, Ceramic	1 nF (DNP), 50 V	SMD 0805W	Yageo
M1	0	Switch	For Only Type−A	TO−247−3L	**onsemi**
			For Only Type−B	TO−247−4L	**onsemi**
			For Only Type−C	D2PAK−7L	**onsemi**
J1, J3	2	BNC Connector		SMB	Johnson / Cinch
J2,J6	2	Connector	2 Pin		CAMDEN
J4,J7	2	Connector	3 Pin		CAMDEN
J8, J9	2	Header	3 Pin	PItch 2.54mm	JINLING
J5, J10	0	Connector	DNP		

EVBs Configuration Setting for Variant A or B

R7	**DNP** for NCP51152xA, and **0 Ω** for NCP51152xB
R8	**0 Ω** for NCP51152xA, and **DNP** for NCP51152xB

Input Stage

The input pins of NCP51152 is based on a TTL−compatible input−threshold logic that is independent of the V_{DD} supply voltage for IN+, and IN− pins. The logic level compatible input provides a typically HIGH and LOW threshold of 1.63 V and 1.08 V respectively. The input signal pins impedance is 125 kΩ typically and the IN+ pin is pulled to GND1 pin and IN− pin is pulled to V_{DD} pin as shown in Figure 5. For non−inverting input logic signal is applied to IN+ while the IN− input can be used as an enable function. If IN− is pulled HIGH, the driver output remains LOW state, regardless of the state of IN+. To enable the driver output, IN− should be tied to GND1 pin through a few ten kΩ resistor (e.g.10 kΩ) or can be used as an active LOW enable pull down.

- Non−inverting input IN+ controls the driver output while inverting input IN− is set to LOW
- Inverting input IN− controls the driver output while non−inverting input IN+ is set to HIGH.

And we recommend an RC network is to be added on the PWM input pins, IN+ and IN−, for reducing the impact of system noise and ground bounce, for example, 51 Ω (R1, and R2) with 10 pF (C1, and C2) is an acceptable choice as shown in Figure 5. IN+, and IN− signal can be monitored via TP1, and TP2, respectively.

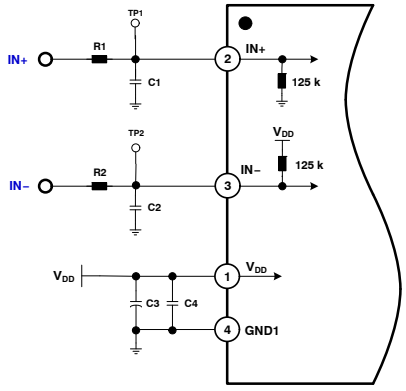


Figure 5. Recommended Input Circuit

Output Stage

The output stage is able to sink/source typically around +4.5 A/−9.0 A at 25°C for the NCP51152.

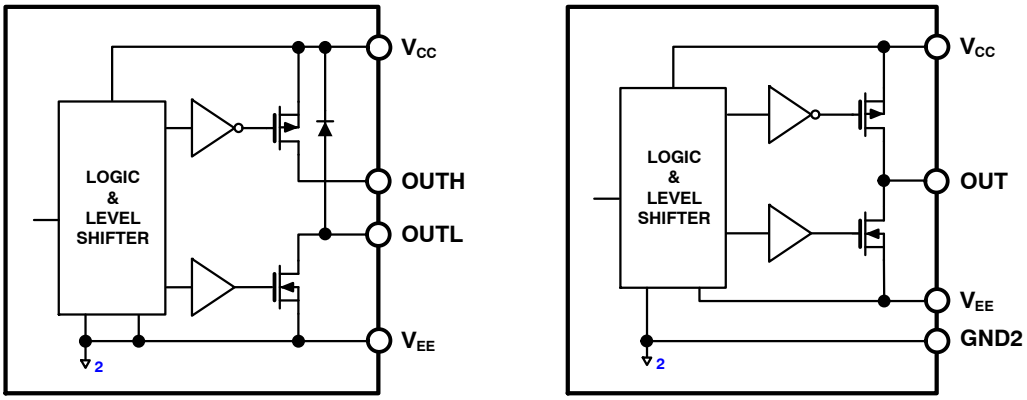
The NCP51152 have different output stages of the variant A and B as shown in Figure 6.

For the variant A is designed to support separate source (OUTH) and sink (OUTL) outputs. This scheme allows a single resistor between each pin and the MOSFET gate to independently control gate ringing as well as fine tuning dV_{DS}/dT turn−on and turn−off transitions present on the MOSFET drain−source voltage.

The EVB comes populated with a 1 nF load (C5) on the output side. The OUTH, OUTL and GATE can be monitored directly via TP4, TP5 and TP7, respectively.

The Type−A EVB allows for evaluation of the device with an MOSFET load in either of the standard TO−3P, TO−247−3L, and TO−252 (D−PAK), and TO−263 (D2PAK) footprints. The Type−B EVB allows for evaluation of the device with an MOSFET load in the standard TO−247−4L The Type−C EVB allows for evaluation of the device with an MOSFET load in the standard D2PAK−7L.

During evaluation with an SiC MOSFET load, the pre−installed capacitive load (C5) can be disconnected from the output. The EVB provides an additional connection (J5) for applying an external power supply to the MOSFET Drain. The EVB is not intended for high voltage testing and the voltage applied to J5 should be limited to 50 V_{DC}.



(A) For variant A

(B) For variant B

Figure 6. Schematic of Output Stage

Functional Mode Table

Table 6 and Table 7 show the functional modes for the NCP51152 variant A and B assuming V_{DD} and V_{CC} are in the recommended ranges for an evaluation board.

Table 6. FUNCTIONAL MODES FOR VARIANT A

INPUT		GATE DRIVE OUTPUT	
IN+	IN−	OUTH	OUTL
LOW	X	Hi−Z	LOW
X	HIGH	Hi−Z	LOW
HIGH	LOW	HIGH	Hi−Z

Table 7. FUNCTIONAL MODES FOR VARIANT B

INPUT		GATE DRIVE OUTPUT
IN+	IN−	OUT
LOW	X	Low
X	HIGH	Low
HIGH	LOW	High

PERFORMANCE OF EVALUATION BOARD

This section describes application guidance and operation of the NCP51152 for an evaluation board (EVB) include key functions.

Protection Function

The NCP51152 provides important protection functions such as independent under−voltage lockout for gate driver. Figure 7 shows an overall input to output timing diagram. Under−Voltage Lockout protection on the primary− and secondary−sides power supplies events in the **CASE−A, B and C** and the gate driver output (OUT) is immediately turn−off when an inverting input signal (IN−) is HIGH regardless non−inverting input (IN+) signal state in the **CASE−D**. The negative bias control circuit is enabled after the V_{CC} power−up delay time, $t_{VPOR\ to\ OUT}$, during initial V_{CC} start−up or after POR event.

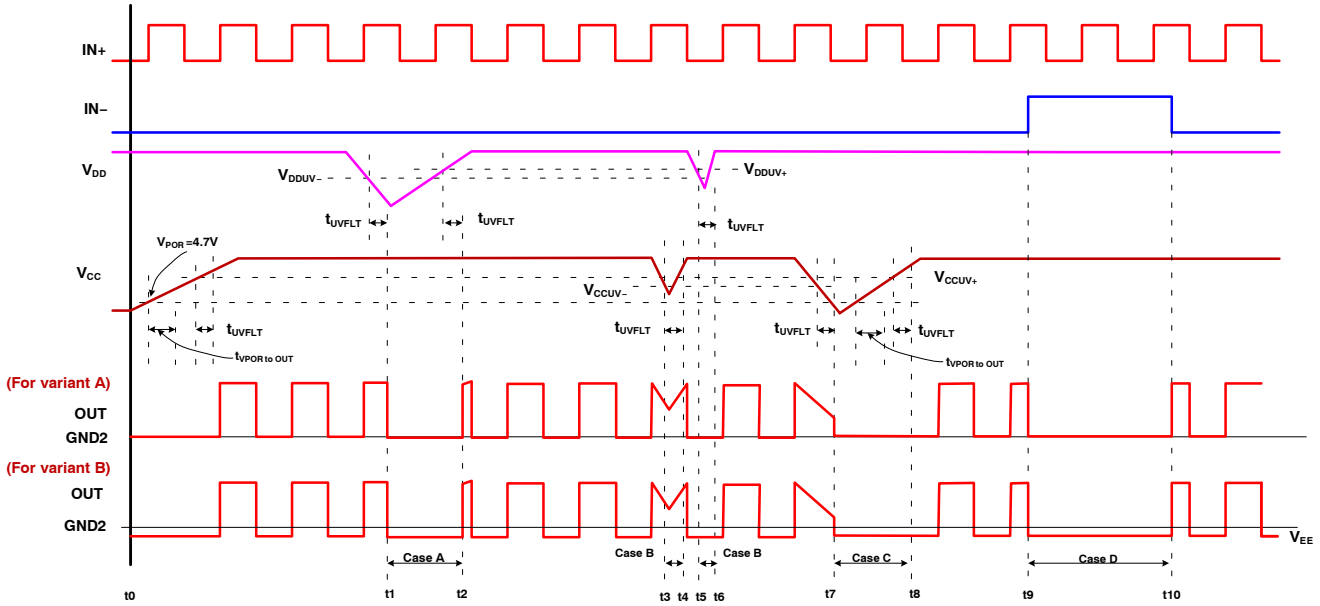
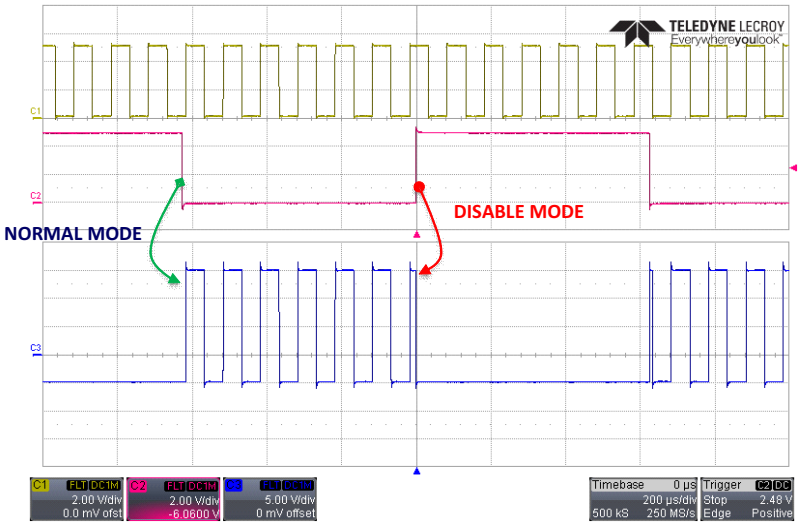


Figure 7. Overall Operating Waveforms Definitions

Figure 8 shows an experimental result of enable function that the inverting input pin (IN−) voltage goes to HIGH state in normal operation, the gate driver output is turned−off immediately regardless non−inverting input (IN+) pin signal state.



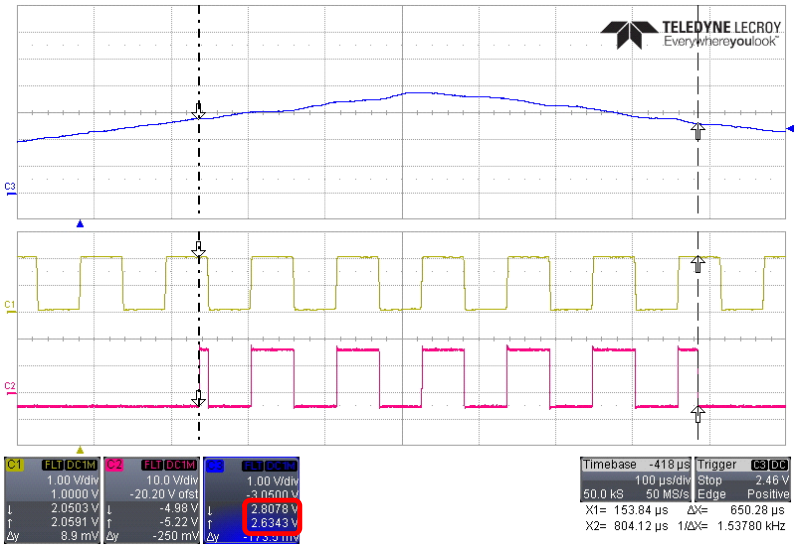
CH1: IN+, CH2: IN−, CH3: OUT_GND2

Figure 8. Experimental Waveforms of Enable Function

Under−Voltage Lockout Protection V_{DD}

The NCP51152 provides the Under−Voltage Lockout (UVLO) protection function for V_{DD} in primary−side.

As test result, the V_{DD} UVLO turn−on and off threshold voltages are around 2.8 V and 2.63 V respectively as shown in Figure 9.

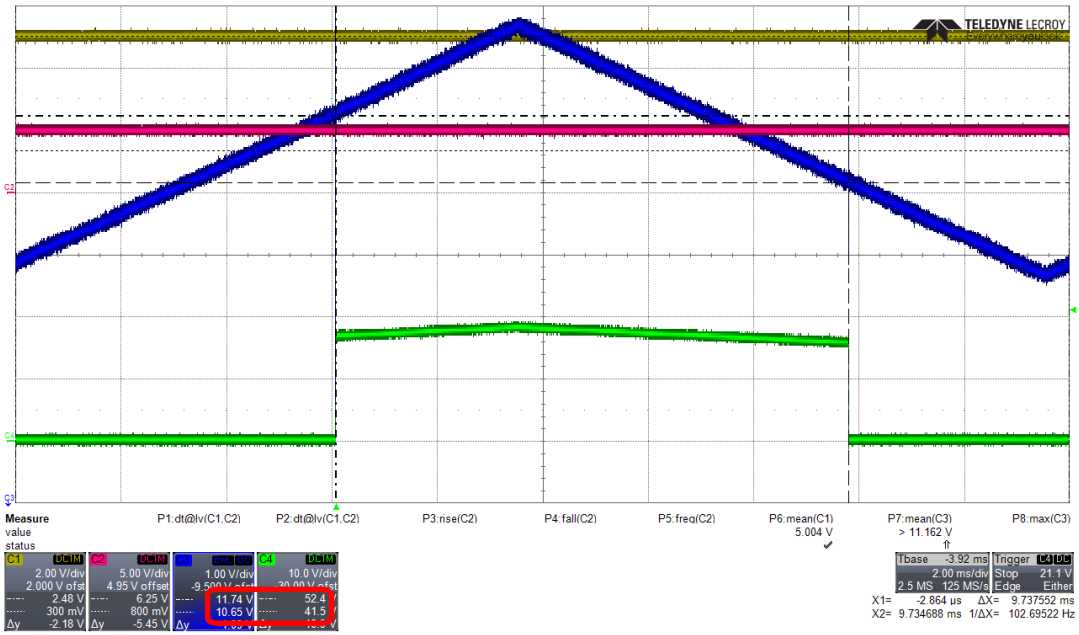


CH1: IN+, CH2: OUT_VEE, CH3: VDD

Figure 9. Experimental Waveforms of V_{DD} Under−Voltage Lockout Protection

Under−Voltage Lockout Protection V_{CC}

The NCP51152 provides the Under−Voltage Lockout (UVLO) protection function of gate drive output in secondary−side. As test result of NCP51152CB variant (For example, VCC UVLO Threshold = 12 V), the V_{CC} UVLO turn−on and off threshold voltages are around 11.74 V and 10.65 V with respect to GND2 respectively due to GND2_VEE external bias voltage is 5−V as shown in Figure 10.

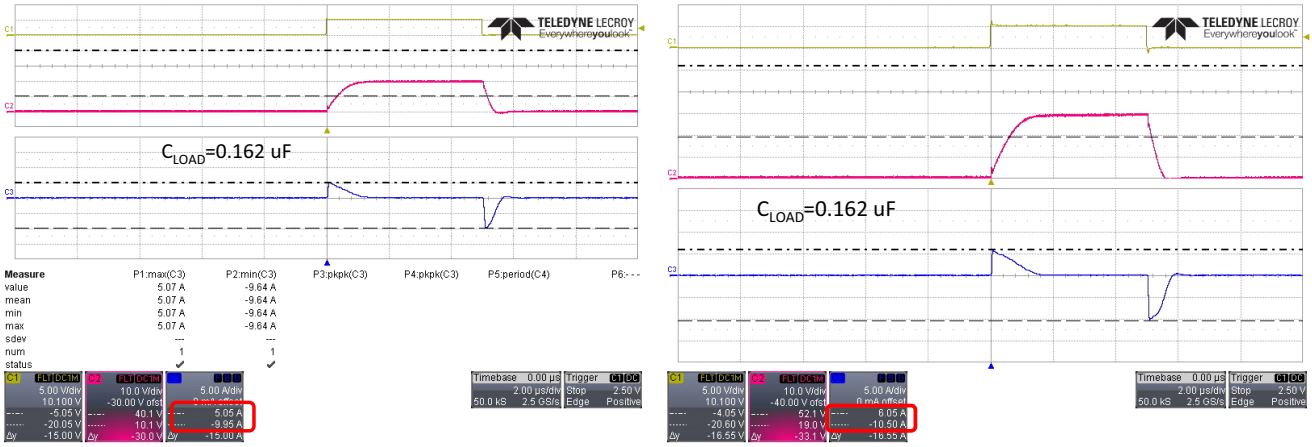


CH1: IN+, CH2: VDD, CH3: VCC_VEE and CH4: OUT_VEE

Figure 10. Experimental Waveforms of V_{CC} Under−Voltage Lockout Protection

Output Driving Current Capability

The experimental result of source and sink peak currents driving capability around 5.0 A and 9.95 A respectively at V_{CC} = 20 V and room temperature as shown in Figure 11 (a). And source and sink peak currents driving capability around 6.0 A and 10.5 A respectively at V_{CC} = 30 V and room temperature as shown in Figure 11 (b).



(a) At V_{DD} = 5 V, and V_{CC} = 20 V

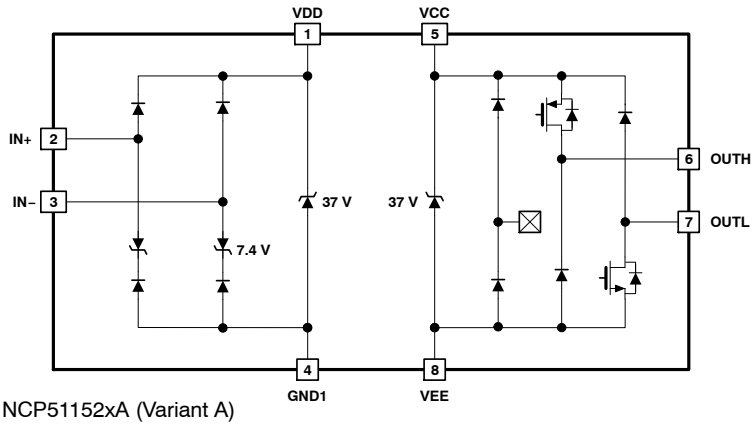
(b) At V_{DD} = 5 V, and V_{CC} = 30 V

CH1: IN+, CH2: OUT_VEE, CH3: OUT Current

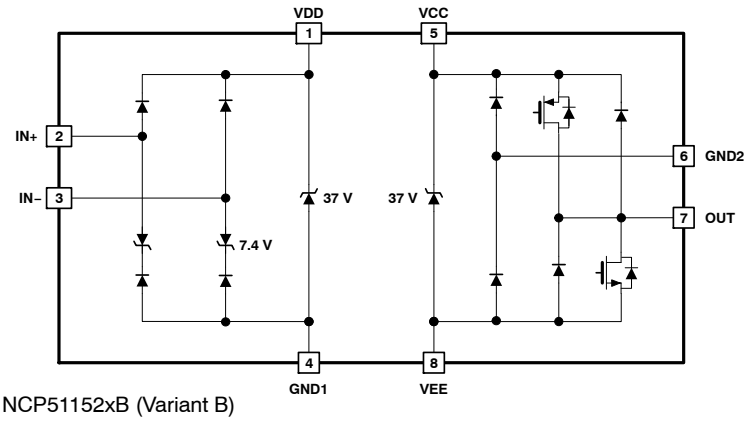
Figure 11. Experimental Waveforms of Current Driving Capability

ESD Structure

Figure 12 shows the multiple diodes related to an ESD protection components of NCP51152 for variants A and B. This illustrates the absolute maximum rating for the device.



(A) For NCP51152xA (Variant A)

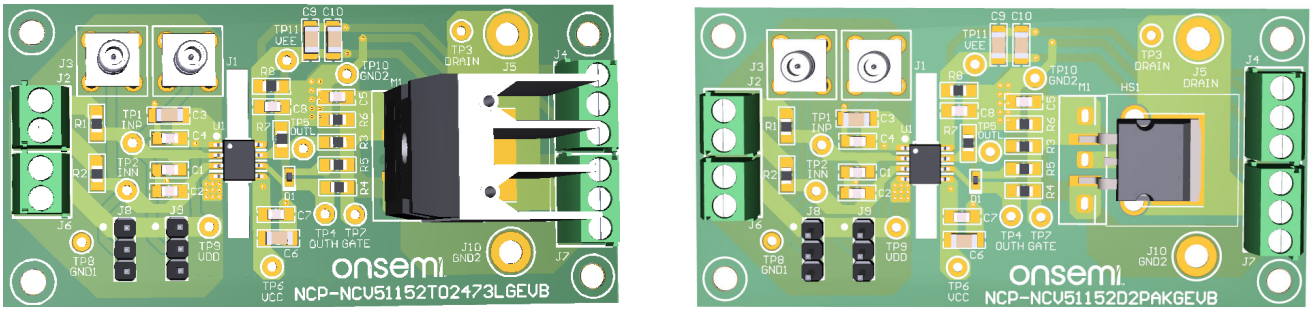


(B) For NCP51152xB (Variant B)

Figure 12. ESD Structure

Printed Circuit Board

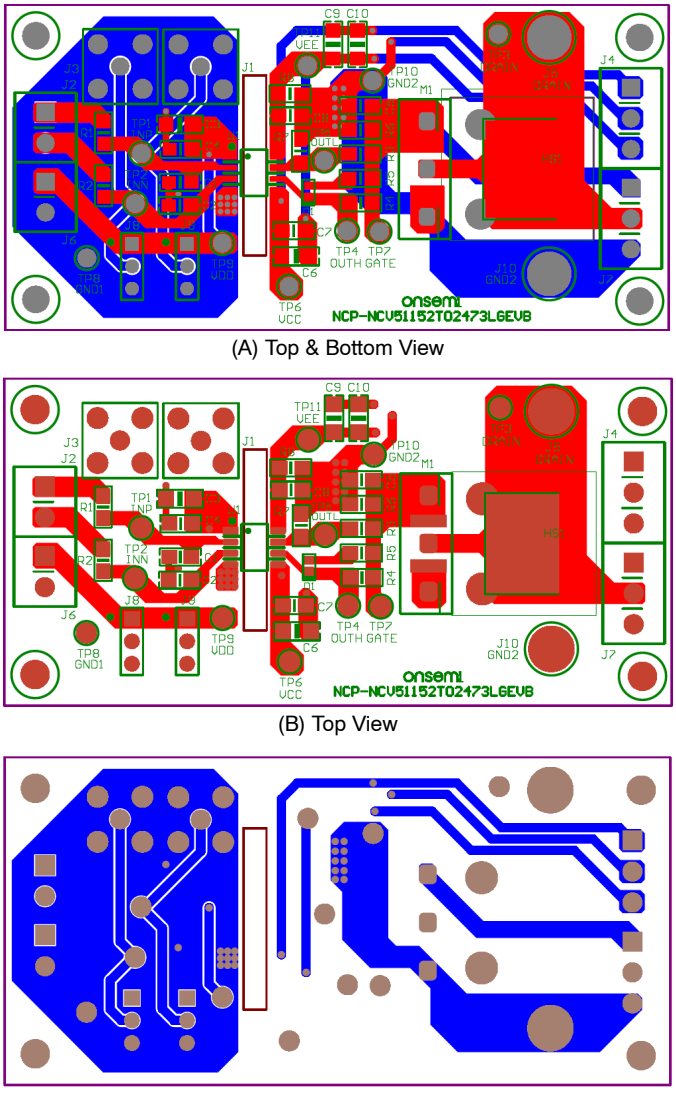
Figure 13 shows the photograph of the NCP51152 evaluation board for the Type−A. This EVB allows for evaluation of the device with an MOSFET load in either of the standard TO−3P, TO−247, TO−252 (D−PAK), and TO−263 (D2PAK) footprints.



(A) For TO−247−3L Package (B) For D2PAK Package

Figure 13. Evaluation Board Picture of Type−A (Top View)

Figure 14 shows the printed circuit board layout of NCP51152 evaluation board for the Type−A.



(A) Top & Bottom View

(B) Top View

(C) Bottom View

Figure 14. Printed Circuit Board of Type−A

Figure 15 shows the photograph of the NCP51152 evaluation board for the Type−B. This EVB allows for evaluation of the device with an MOSFET load in the standard TO−247−4L footprint.

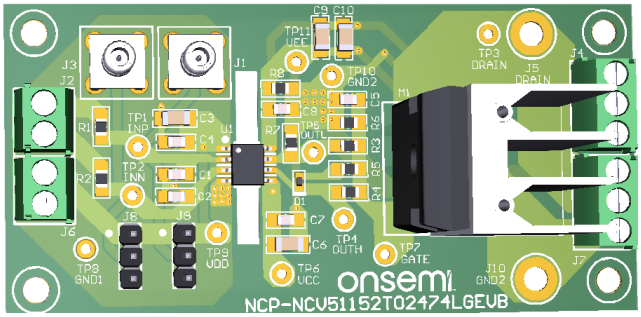
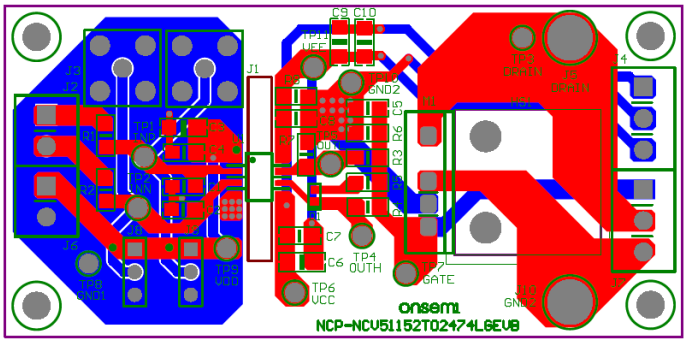
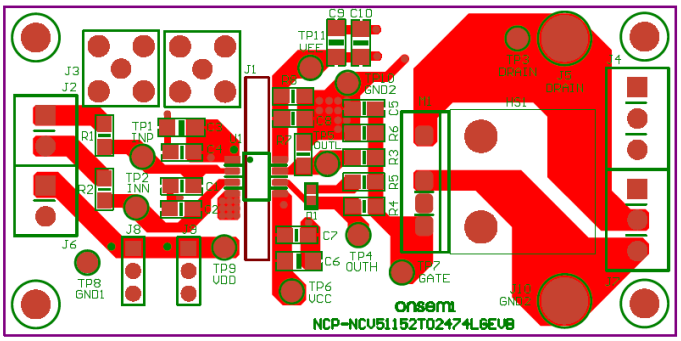


Figure 15. Evaluation Board Picture of Type−B (Top View)

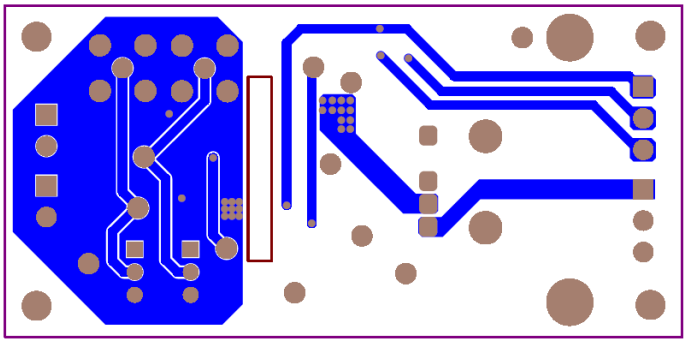
Figure 16 shows the printed circuit board layout of NCP51152 evaluation board for the Type−B.



(A) Top & Bottom View



(B) Top View



(C) Bottom View

Figure 16. Printed Circuit Board of Type−B

Figure 17 shows the photograph of the NCP51152 evaluation board board for the Type−C. This EVB allows for evaluation of the device with an MOSFET load in the standard D2PAK−7L footprint.

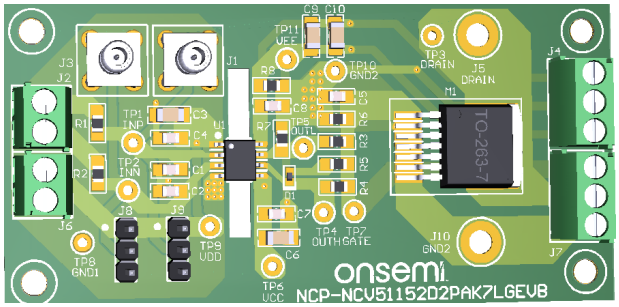
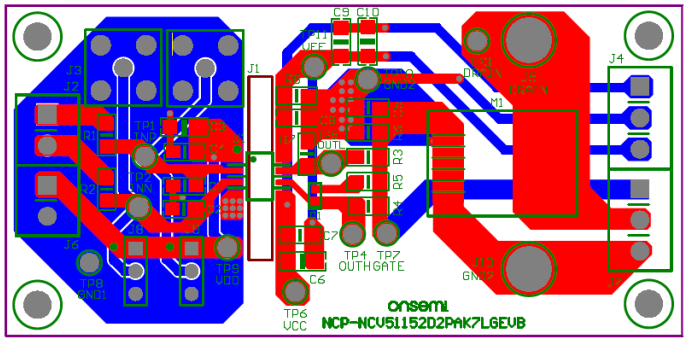
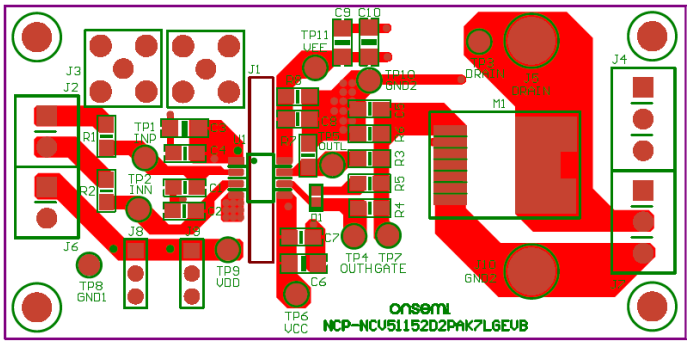


Figure 17. Evaluation Board Picture of Type−C (Top View)

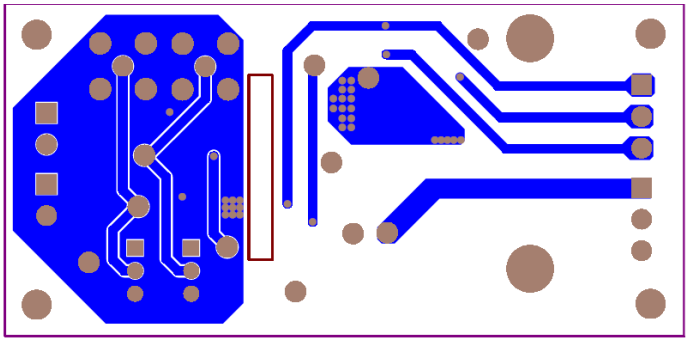
Figure 16 shows the printed circuit board layout of NCP51152 evaluation board for the Type−B.



(A) Top & Bottom View



(B) Top View



(C) Bottom View

Figure 18. Printed Circuit Board of Type−C

Related Product Information

[1] Datasheet of NCP51152 available on **onsemi** website

[2] Datasheet of NCV51152 available on **onsemi** website

[3] **onsemi** AND90180/D, “Practical Design Guidelines on the Usage of an Isolated Gate Driver”

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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