

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for OBC_PFC_control_board.PrjPcb

Design Rules Verification Report

Filename : C:\Users\fg4ngv\AppData\Local\Temp\Snapshot\1\design_files\OBC_PFC_cont
 rol_board.PcbDoc

Warnings 0
 Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=7.874mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=100mil) (Preferred=24mil) (All)	0
Routing Layers(All)	0
Routing Via (Templates Used To Check Via: v102h51_lib, v142h71_lib, v203h102_lib) (All)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=10mil) (Max = 10mil) (Prefered= 10mil) and Width	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Fabrication Testpoint Style (Under Component=Yes) (All)	0
Fabrication Testpoint Usage (Valid =Don't care, Allow multiple per net=No) (All)	0
Assembly Testpoint Style (Under Component=Yes) (All)	0
Assembly Testpoint Usage (Valid =Don't care, Allow multiple per net=No) (All)	0
Hole Size Constraint (Min=11.811mil) (Max =165.354mil) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=4mil) (All),(All)	0
Silk To Solder Mask (Clearance=4mil) (IsPad),(All)	0
Silk to Silk (Clearance=8mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Component Clearance Constraint (Horizontal Gap = 4mil, Vertical Gap = 4mil) (IsComponent and	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil) (IsComponent and (Name =	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil) (IsComponent and (Name Like	0
Component Clearance Constraint (Horizontal Gap = 10mil, Vertical Gap = 10mil) (All),(All)	0
Silk primitive without silk layer	0
Total	0