


- 1 Material: Isola DE104 or similar
- 2 Finish: ENIG (Electroless Nickel Immersion Gold), nickel layer $1 \div 4 \mu\text{m}$, gold layer $0.076 \div 0.2 \mu\text{m}$
- 3 All gerber files generated as a top view
- 4. Fabricate according IPC-A-600
- 5. Non-conductive epoxy ink recommended for silkscreen
- 6. Silkscreen should not cover any exposed copper, silkscreen gerber data have to be trimmed eventually
- 7. All holes diameter refer to final diameter after eventual plating

Gerber and drill file extensions table

Gerber files	
.GTO	Top side silkscreen
.GTP	Top side solder paste mask
.GTS	Top side solder mask
.GTL	Top Layer
.GBL	Bottom Layer
.GBS	Bottom side solder mask
.GBP	Bottom side solder paste mask
.GBO	Bottom side silkscreen
.GM1	Board dimension
Drill files	
.TXT	Layer pair Top Layer to Bottom Layer - round holes
.TXS	Layer pair Top Layer to Bottom Layer - slot holes

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Layer Stack

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Paste			Paste Mask	GTP
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.0120mm(0.472mil)	Solder Resist	Solder Mask	GTS
Copper	Top Layer	0.1000mm(3.937mil)		Signal	GTL
Core		1.4760mm(58.110mil)	Isola DE104 (4x7628M)	Dielectric	
Copper	Bottom Layer	0.1000mm(3.937mil)		Signal	GBL
Surface Material	Bottom Solder	0.0120mm(0.472mil)	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
	Bottom Paste			Paste Mask	GBP

Total thickness: 1.7000mm(66.929mil)

Notes:

- ⑧ Top and Bottom layer thickness consists of 70µm copper foil, ~25µm plating and ~5µm ENIG finish

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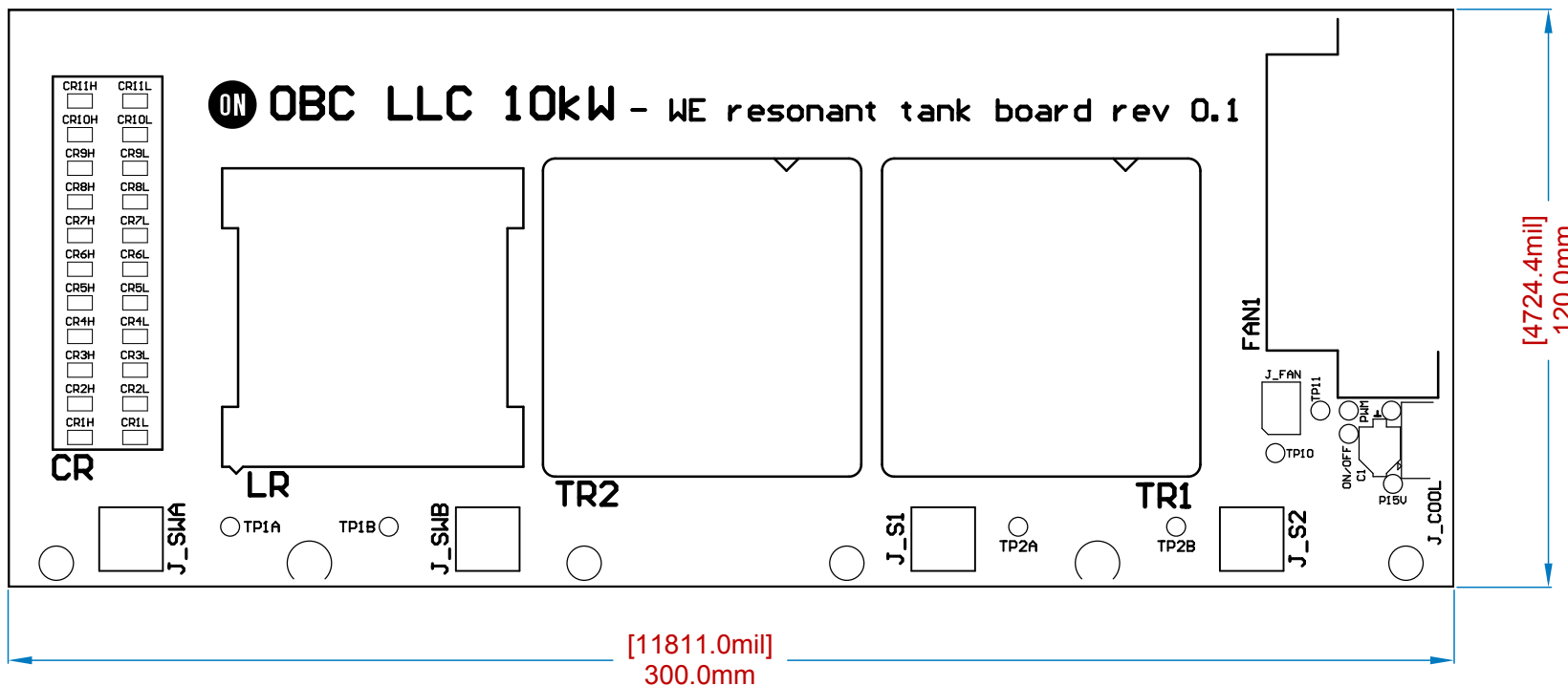
B

C

C

D

D



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<i>Board outline definition - top view 2:3</i>		Fabrication document	Sheet 3 / 12
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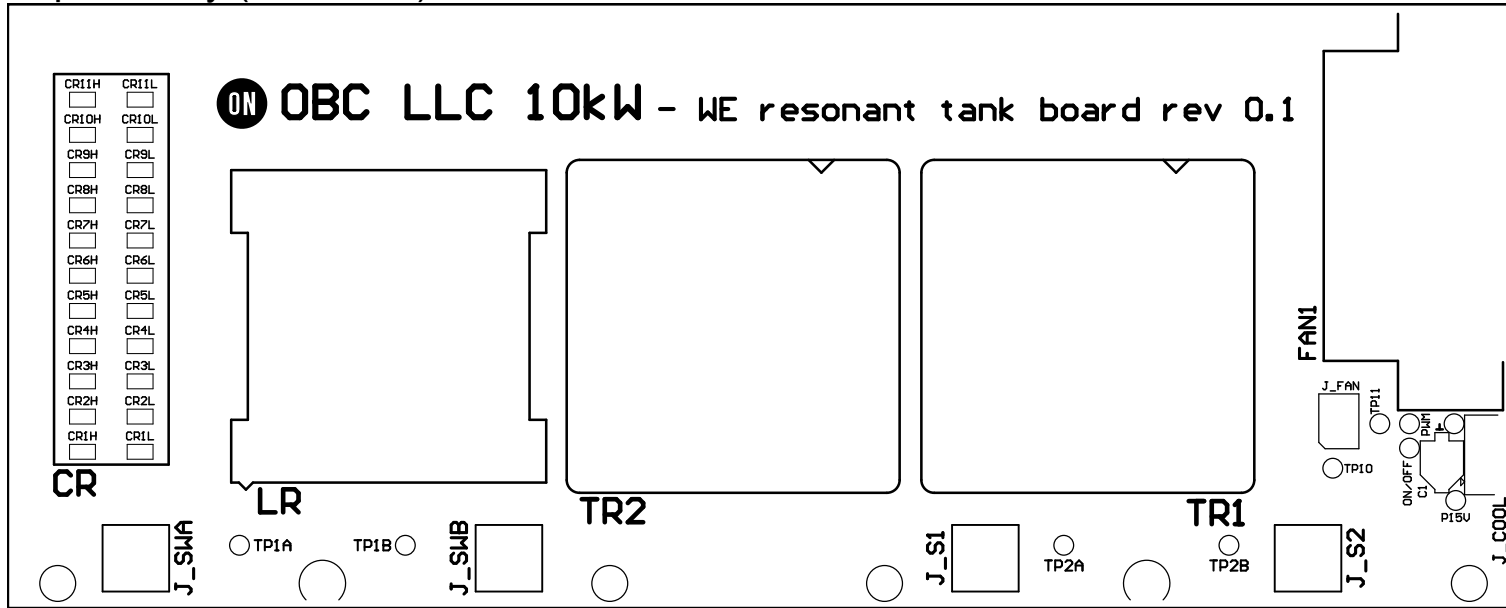
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Top Overlay (Scale 2:3)



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<i>Top side silkscreen - top view</i>		Fabrication document	Sheet 4 / 12
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Top Paste (Scale 2:3)



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<i>Top side solder paste - top view</i>		Fabrication document	Sheet 5 / 12
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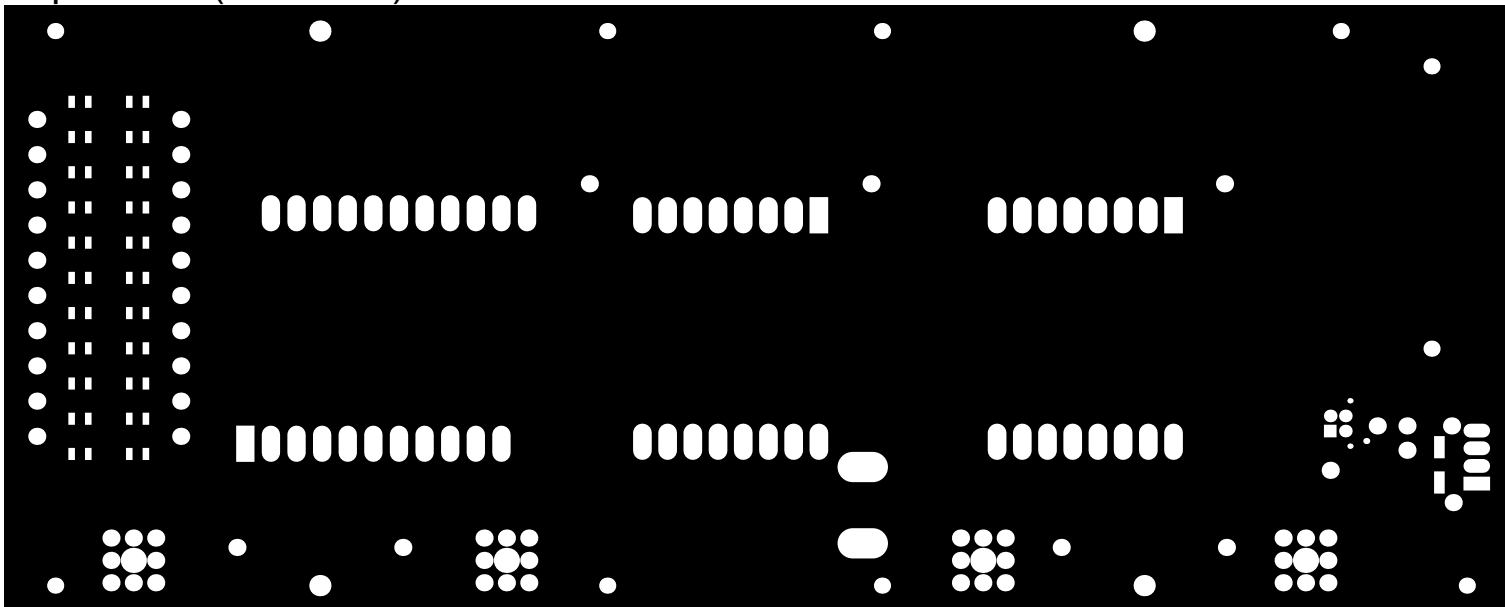
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Top Solder (Scale 2:3)



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<i>Top side solder mask - top view</i>		Fabrication document	Sheet 6 / 12
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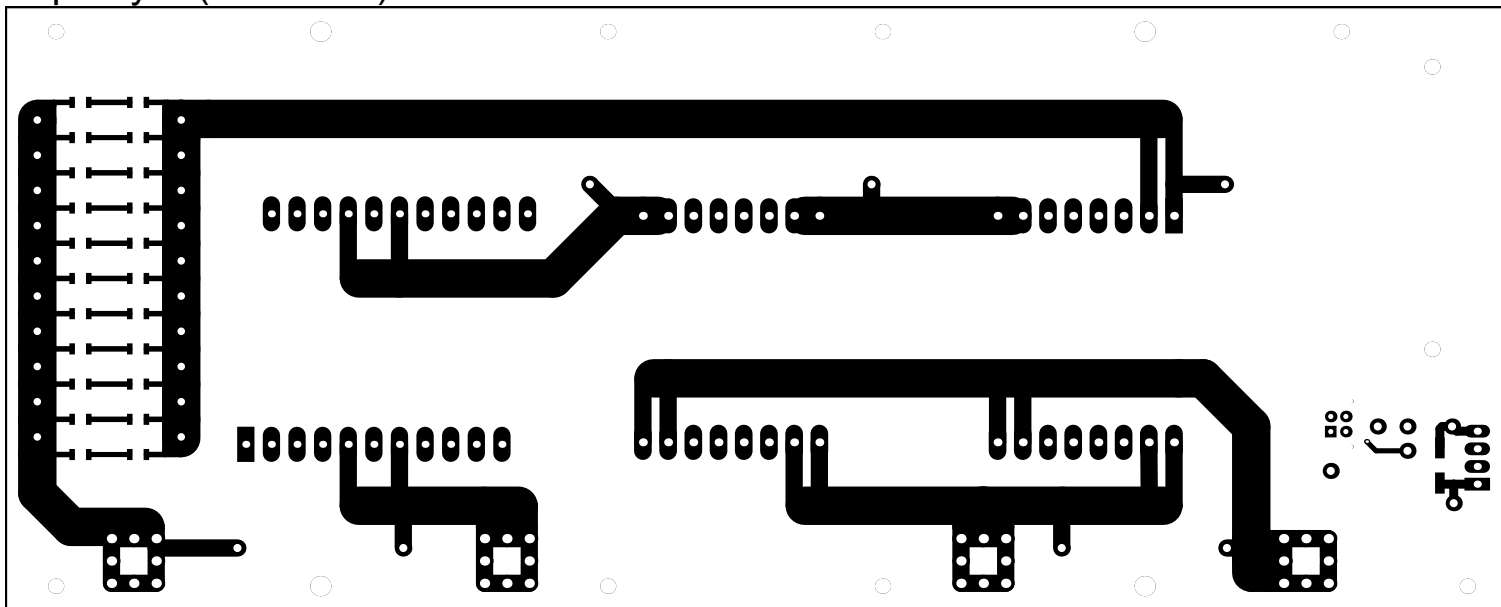
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Top Layer (Scale 2:3)



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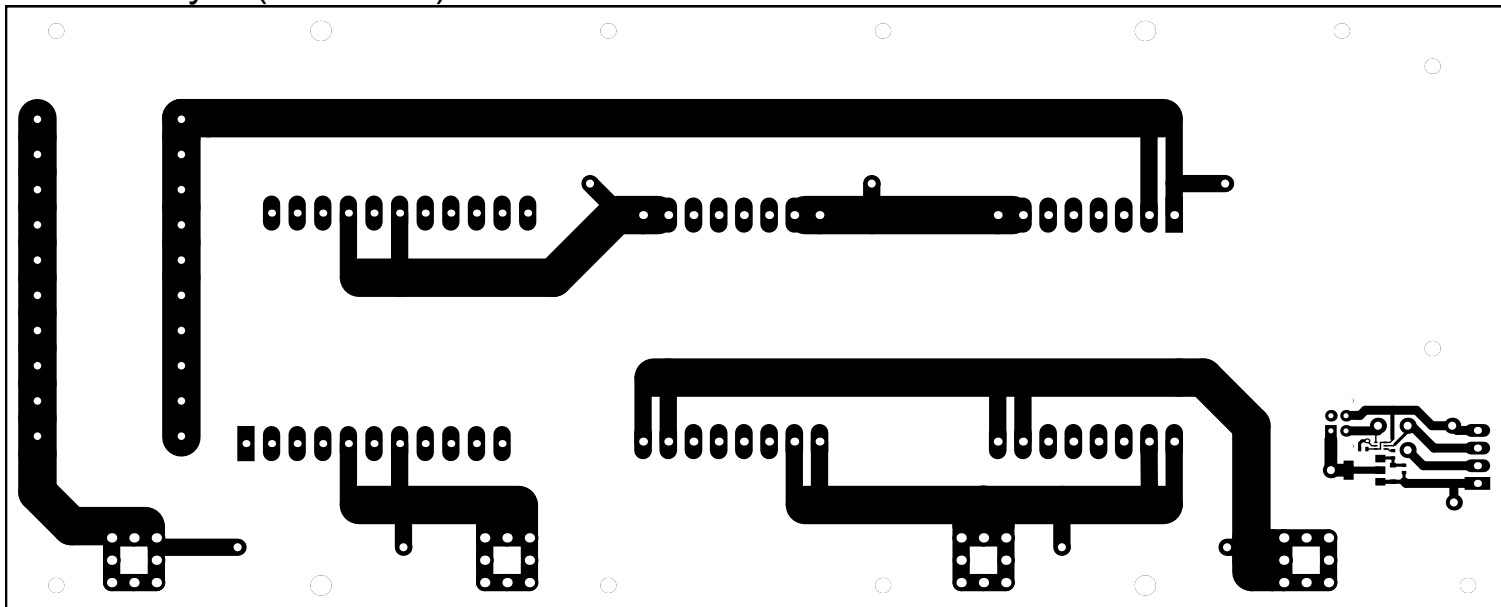
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Bottom Layer (Scale 2:3)



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<i>Bottom Layer - top view</i>		Fabrication document	Sheet 8 / 12
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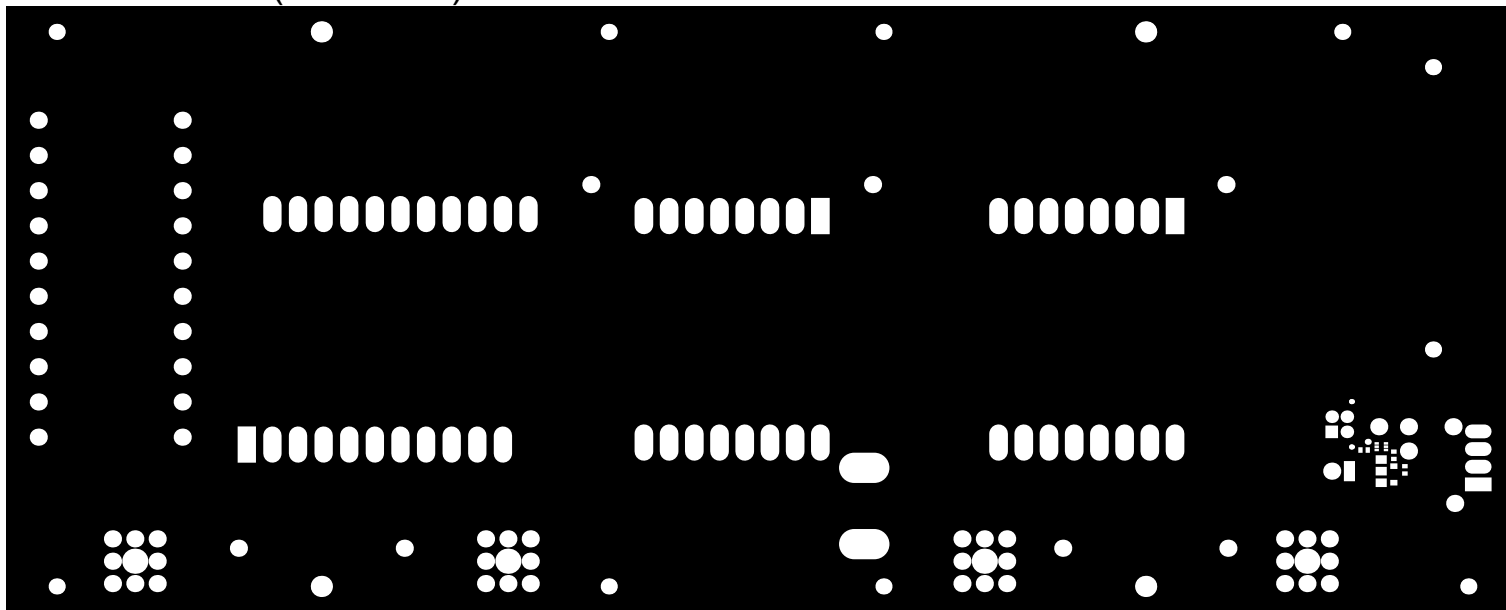
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Bottom Solder (Scale 2:3)



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<i>Bottom side solder mask - top view</i>		Fabrication document	Sheet 9 / 12
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Bottom Paste (Scale 2:3)



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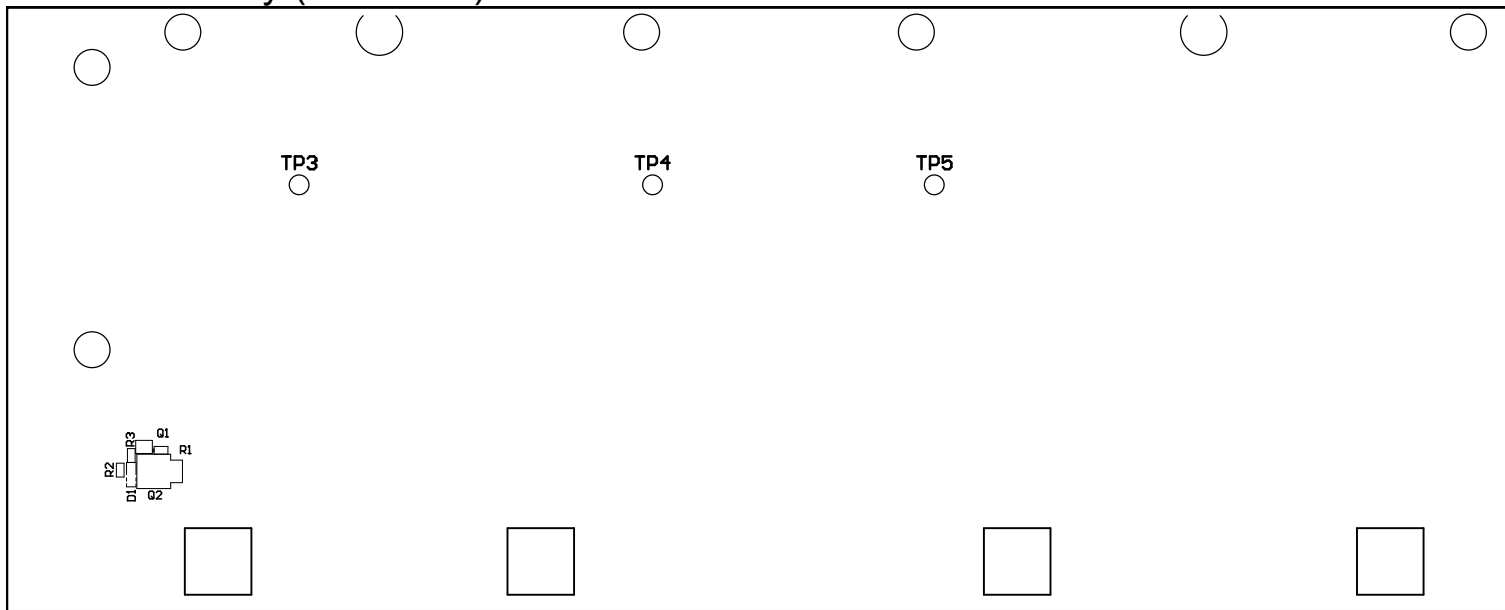
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A

Bottom Overlay (Scale 2:3)



B

B

C

C

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D

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<i>Bottom side silkscreen - bottom view</i>		Fabrication document	Sheet 11 / 12
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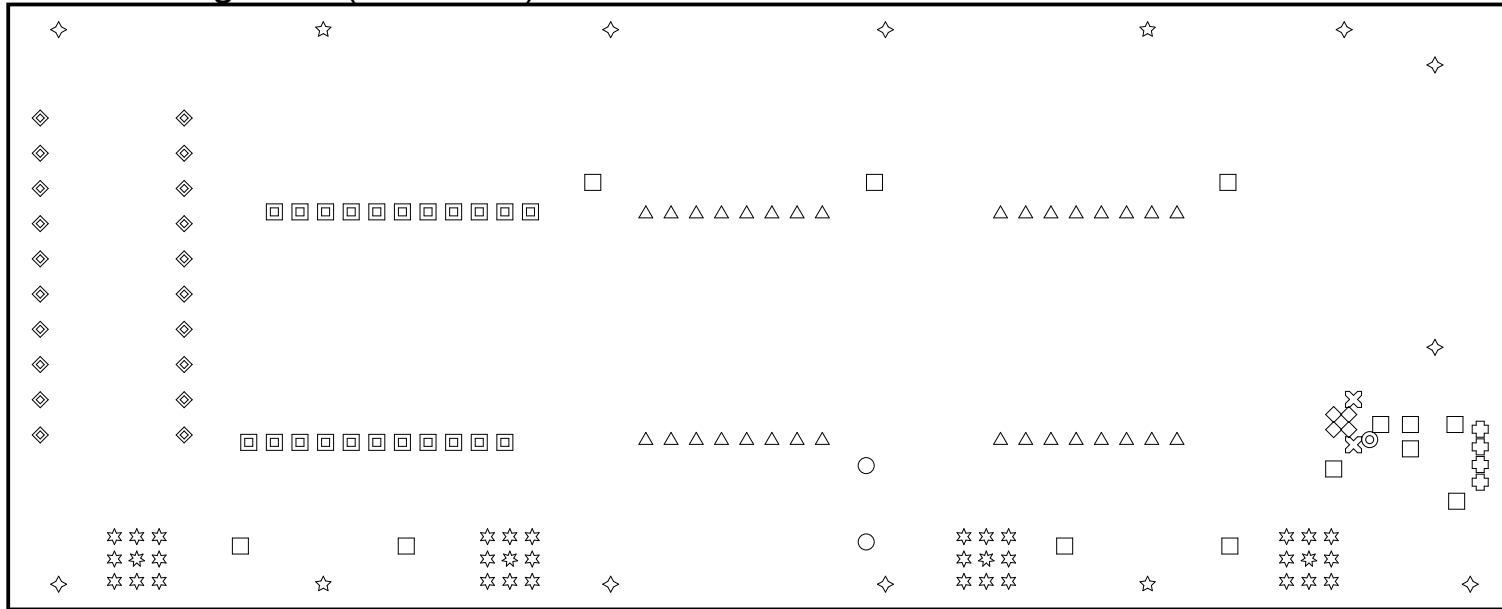
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Drill Drawing View (Scale 2:3)



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad	Template
⊙	1	0.500mm(20mil)	Plated	Top Layer - Bottom Layer	Via	v100h50
◇	4	1.020mm(40mil)	Plated	Top Layer - Bottom Layer	Pad	(Mixed)
⊗	2	1.020mm(40mil)	Non-Plated	Top Layer - Bottom Layer	Pad	c80hn102
▣	22	1.397mm(55mil)	Plated	Top Layer - Bottom Layer	Pad	(Mixed)
⊕	4	1.422mm(56mil)	Plated	Top Layer - Bottom Layer	Pad	(Mixed)
◆	20	1.500mm(59mil)	Plated	Top Layer - Bottom Layer	Via	v320h150
△	32	1.570mm(62mil)	Plated	Top Layer - Bottom Layer	Pad	(Mixed)
□	13	1.600mm(63mil)	Plated	Top Layer - Bottom Layer	Pad	c320h160
☆	32	1.850mm(73mil)	Plated	Top Layer - Bottom Layer	Pad	c320h185
◇	10	3.000mm(118mil)	Non-Plated	Top Layer - Bottom Layer	Pad	c300hn300
☆	4	4.000mm(157mil)	Non-Plated	Top Layer - Bottom Layer	Pad	c400hn400
☆	4	5.000mm(197mil)	Non-Plated	Top Layer - Bottom Layer	Pad	c254hn500
○	2	6.000mm(236mil)	Non-Plated	Top Layer - Bottom Layer	Pad	c500hn600_1000
150 Total						

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Drill drawing

Fabrication
document

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