100 W USB-PD Solution with NCP1945 and NCP4306

DN05138/D

SPECIFICATIONS

onsemi Devices	Application	Input Voltage	Output Power	Topology	I/O Isolation
NCP1945 NCP4306	USB-PD	90 to 264 Vac	100 W	BOOST PFC, Quasi-resonant Flyback	Isolated

Output Voltage/Nominal Current	5 V/5 A, 9 V/5 A, 12 V/5 A, 15 V/5 A, 20 V/5 A
Average Efficiency*	92.28% / 91.78% at 20 V, 5 A, 115 Vac / 230 Vac
Standby Power*	23.8 mW / 41.5 mW at 5 V, 115 Vac / 230 Vac
PCB Size	72 mm x 142 mm

NOTE: The data in this table is taken with the NCP1945BA version, with Gallium Nitride FETs.

Overview

This design note describes a 100 W constant voltage power supply intended for high-performance off-line USB-PD and USB Type-C® power converters. The evaluation board (EVB) uses the NCP1945, a combination IC which integrates power factor correction (PFC) and quasi-resonant flyback functionality. Key features of the NCP1945 demonstrated on this board include Boost follower, Dynamic Response Enhancer (DRE), Power Excursion Mode (PEM), adjustable PFC enable and disable thresholds, and several protections features while maintaining low cost, high efficiency, and low standby power consumption.

The EVB is available with either the NCP1945AA or NCP1945AB OPN. The AA version features silicon FET daughter cards for the most cost-effective solution. The BA OPN version comes with Gallium Nitride FETs that are directly driven by the NCP1945. The BA version has a clamped drive voltage making it capable of directly driving a GaN FET on both the PFC and QR drives.

The NCP1945 has optimized circuitry for a Boost PFC with features to ensure near-unity power factor while optimizing efficiency at all loads. The PFC operates in critical conduction mode (CrM) until the power drops below a threshold level at which time innovative Valley Synchronized Frequency Fold-back (VSFF) method is used. Using the VSFF the PFC stage enters discontinuous conduction mode (DCM) with a dead-time which increases as the load decreases (frequency foldback) reducing switching losses.

The NCP1945 also supports a quasi-resonant (QR) current-mode flyback stage featuring proprietary valley-lockout circuitry to ensure stable valley switching down to the 6th valley, then transitions to frequency foldback mode to reduce switching losses. When the load decreases further, the NCP1945 QR section enters skip mode to manage the power delivery with special minimum peak current modulation circuitry. The minimum peak current modulation circuitry reduces the switching frequency quickly improving light load performance with high frequency designs. The QR circuitry automatically senses reflected output voltage and adjusts features or optimal performance including minimum peak current in light loads, current limiting circuitry to ensure a constant output current limit regardless of programmed output voltage, or nameplate output power.

Synchronous rectification (SR) is implemented on the secondary side for increased efficiency with the NCP4306. The SR controller features adjustable minimum on and off times for SR drive pulses.

Key Features

- PFC: Follower Boost Capability
- PFC: Adjustable Enable and Disable Threshold
- Integrated High-voltage Startup Circuit with Brownout Detection
- Integrated X2 Capacitor Discharge Capability
- Dual Range Vcc, with 150 V VccH Pin for Connection to High Voltage Aux Winding
- Primary Side Based Constant Output Current Limiting
- Latching or Auto-recovery Timer-Based Overload Protection
- QR: Abnormal Overcurrent Fault Protection for Winding Short Circuit Detection
- QR: Valley Switching Operation with Valley-lockout for Noise-free Operation
- QR: Frequency Foldback with 25 kHz Minimum Frequency
- QR: Rapid Frequency Foldback for Fast Reduction of Switching Frequency
- QR: Frequency Jittering for Reduced EMI Signature
- QR: Adjustable Overpower Protection
- Power Excursion Mode (PEM) Enables use of Low Bulk Capacitance

MOTHERBOARD SCHEMATIC

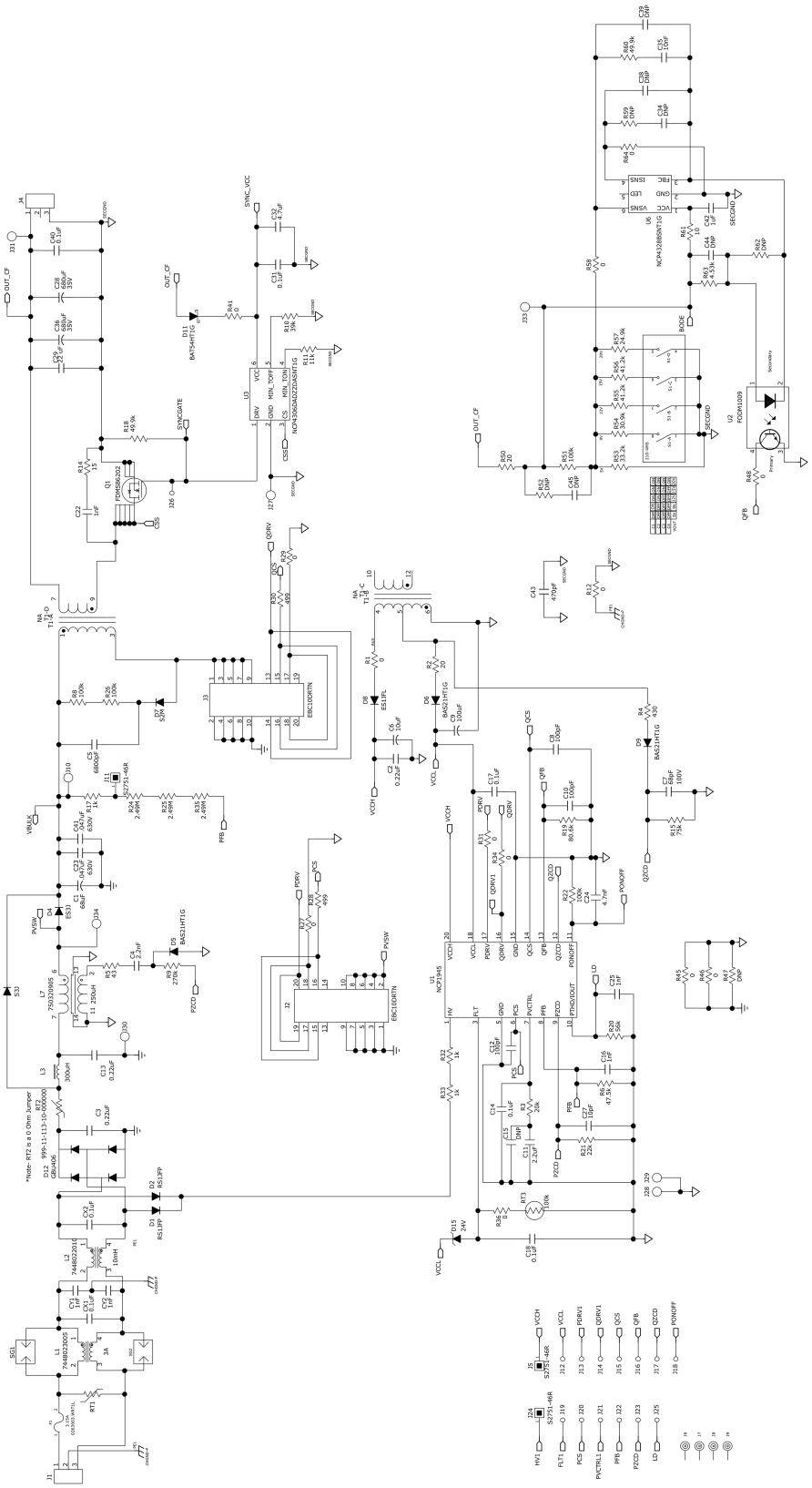


Figure 1. Motherboard Schematic

DAUGHTER CARD CIRCUIT SCHEMATIC

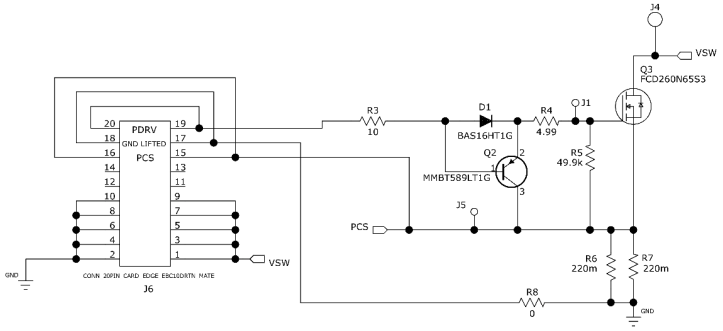


Figure 2. PFC Daughter Card with Si FET

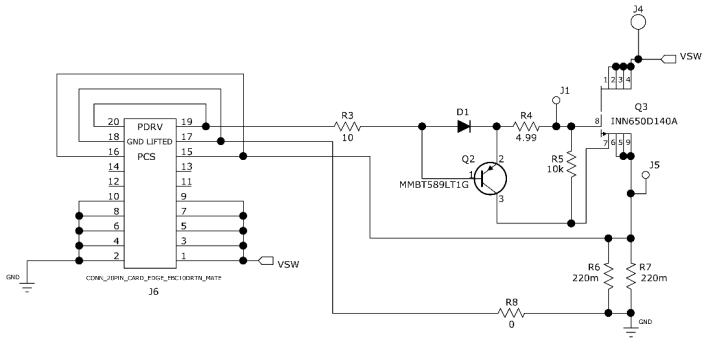


Figure 3. PFC Daughter Card with GaN

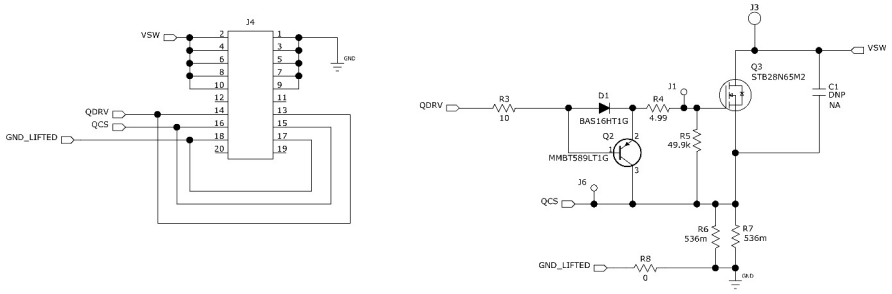


Figure 4. QR Daughter Card with Si

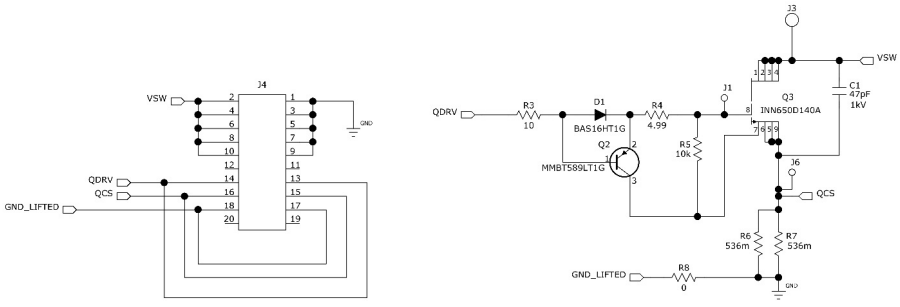


Figure 5. QR Daughter Card with GaN

Board Picture and Test Setup

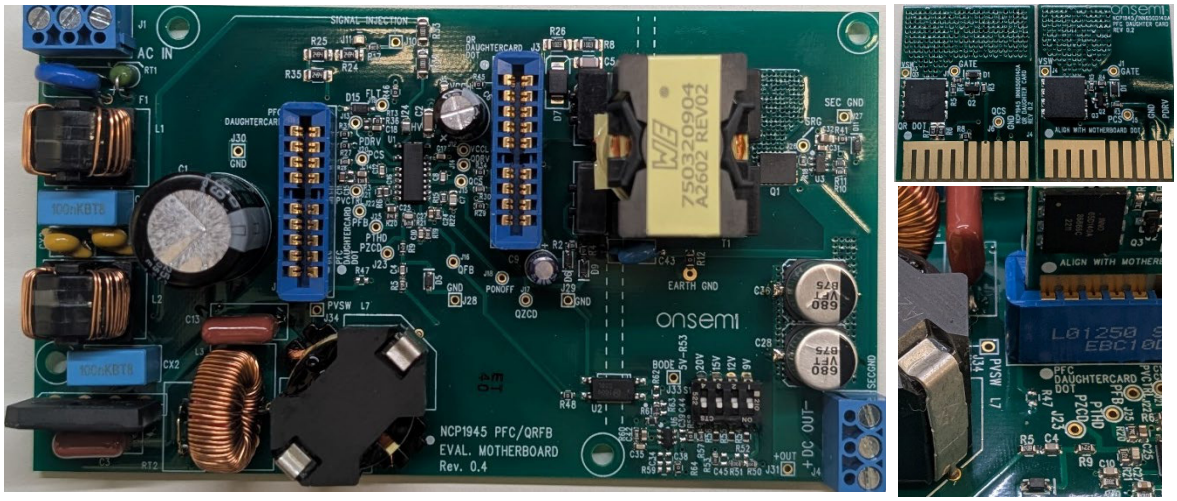


Figure 6. NCP1945 USB-PD Evaluation Board and Daughter Cards

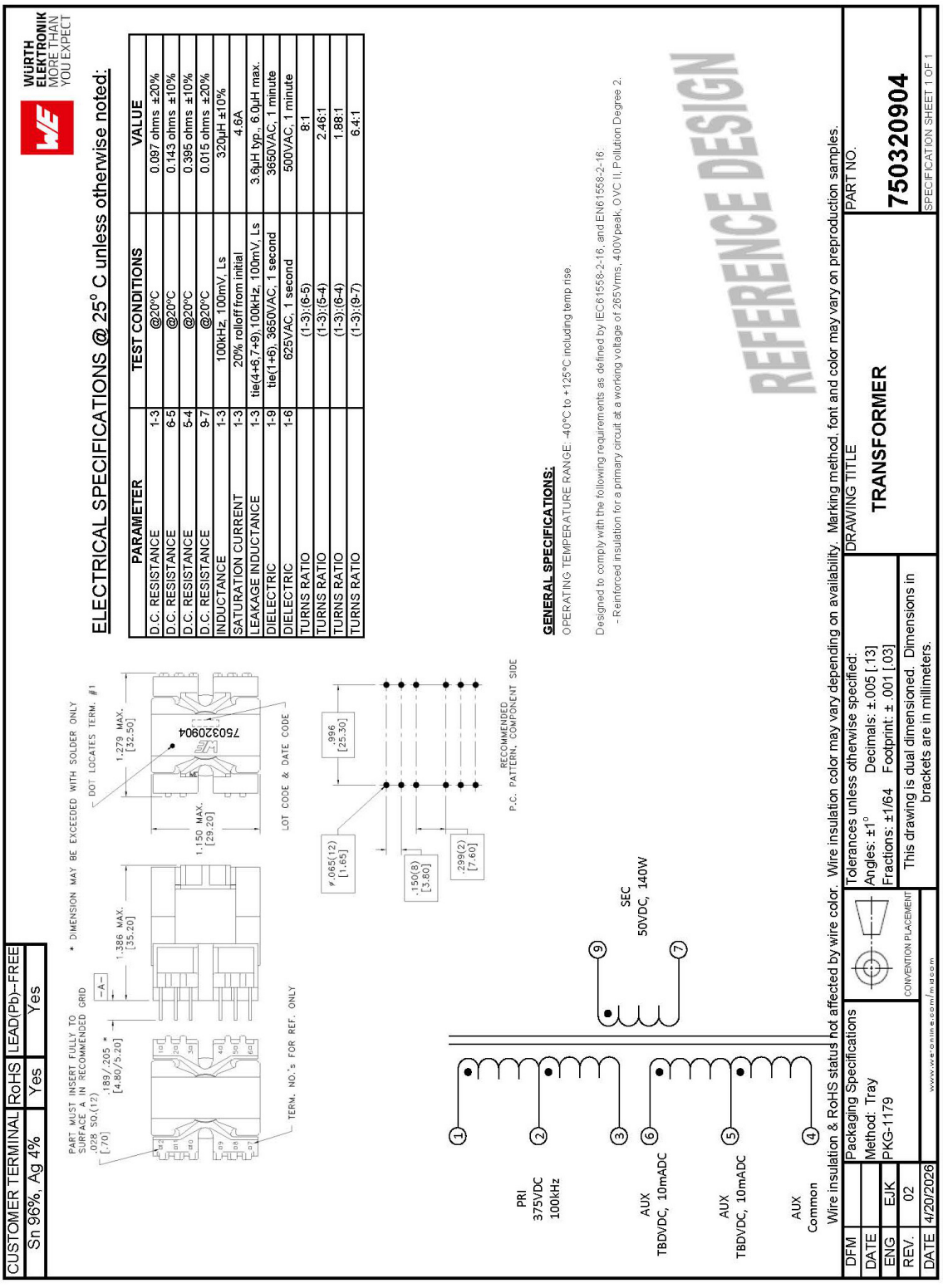
Here are some key points regarding the operation and the Test set up of the NCP1945 USB-PD EVB:

- The NCP1945 features a HV startup sequence that makes it such that this board does not require any external biasing. The only required connections are J1, the AC input, and J4, the DC output. J1, the AC Input connector is pinned out for a 3-wire AC input connection, however, the chassis GND connection is not required and can be left open. The user should determine the appropriate input connection based on their application requirements.
- J2 and J3 are the sockets for the daughter cards. When inserting the daughter cards, please ensure that the PFC daughter card is in J2, and the QR daughter card is in J3. Also ensure that the alignment dots on the daughter cards match up with the dots on the mother board. The bottom right image in Figure 6 shows a close-up image of the J2 socket to demonstrate proper daughter card alignment. Accidental swapping of the daughter cards, or misalignment in the socket will cause damage to the board and the IC.
- The output voltage is selected through the dip switch panel near the output capacitors. The output voltage can be 5 V, 9 V, 12 V, 15 V, or 20 V. Please note that the nominal max current is 5 A in all voltage settings. Table 2 below shows the arrangement of the switches for each of the potential output voltages.

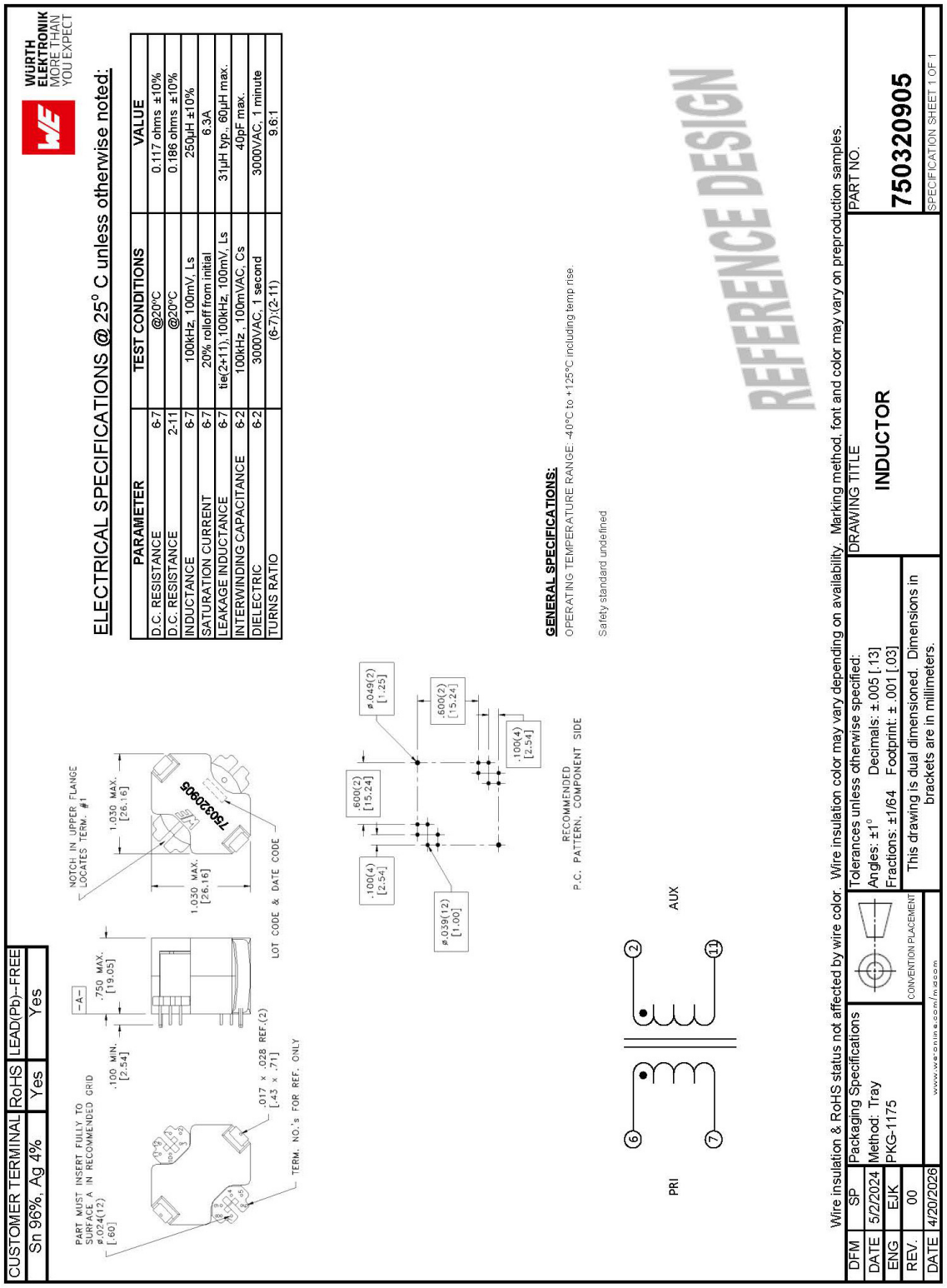
Table 1. OUTPUT VOLTAGE DIP SWITCH SETTINGS

Output Voltage	Switch 1	Switch 2	Switch 3	Switch 4
5 V	Up	Up	Up	Up
9 V	Up	Up	Up	Down
12 V	Up	Up	Down	Down
15 V	Up	Down	Down	Down
20 V	Down	Down	Down	Down

FLAYBACK TRANSFORMER SPECIFICATION



PFC INDUCTOR SPECIFICATION



DESCRIPTION OF KEY FEATURES

Boost Follower Operation

The PFC error amplifier can be programmed with a line-dependent reference voltage that increases when the application is operating at high line. This allows the PFC to operate as a two-level boost follower, enabling higher average efficiency across line voltage.

At low-line, a Follower Boost reduces the PFC bulk voltage to optimize the PFC stage efficiency and significantly shrink its size and cost. In particular, the boost inductance and the MOSFET losses can be dramatically reduced. Since the output voltage must remain higher than the line voltage, the output voltage is lowered only in low line while it remains regulated to the default nominal level generally set to 400 V in high-line conditions. Practically, the IC controls this 2-level follower boost operation through the reference voltage on the error amplifier.

On this board, the bulk voltage is regulated to 400 V at highline, and 256 V at lowline. Figures 15 and 16 show the transition between high line and low line where the bulk voltage changes between 256 V and 400 V.

Dynamic Response Enhancer (DRE)

Given the low bandwidth of the regulation loop, abrupt variations of the load, may result in excessive over or under-shoots. The NCP1945 embeds a “Dynamic Response Enhancer” circuitry (DRE) that contains under-shoots. An internal comparator monitors the FB pin and when this voltage is lower than 95.5% of its nominal value (92.5% when boost follower low line), a 200-μA current is sourced to speed-up the charge of the compensation network as shown in Figure 7. Effectively this appears as a 10x increase in the loop gain. DRE is disabled during the start-up sequence until the PFC stage has stabilized (that is when the “pfcOK” signal of the block diagram, is high). The resulting slow and gradual charge of the VCTRL voltage (VCTRL) softens the soft start-up sequence. DRE is also disabled in case the OVP2 (Second Over Voltage Protection) signal is high.

Power Excursion Mode (PEM)

The NCP1945 includes a power excursion mode, where the QR flyback can operate in off-time controlled continuous conduction mode (CCM) for short time durations, enabling the application to ride through transient peak power loads. PEM operation eliminates the need for a larger transformer to handle peak power requirements and also helps reduce the size of the PFC output bulk capacitance, allowing for higher power density. This board can deliver 2x the maximum load and can operate in PEM for 160 ms before the constant current overload is tripped. Figure 14 below shows a waveform of the device entering PEM. As the output load increases, the device transitions into PEM. The controller raises the cycle by cycle current limit threshold and increases the switching frequency, enabling the board to operate in CCM and deliver up to twice its nominal power.

Adjustable PFC ON/OFF Thresholds

The PONOFF function is utilized to enable the PFC circuit as a function of the QR flyback output power. The feature utilizes a proprietary control circuit that takes the sensed voltage from the QZCD pin and the measured load current from the constant current protection to estimate the output power from the QR flyback. The estimated power signal is output from the PONOFF pin, where a programming resistor can be used to select the power level when the PFC would be enabled. Table 3 shows the enable and disable thresholds of the USB-PD board across various line voltages and out voltages.

Table 2. PFC TURN ON/OFF THRESHOLDS

	90 V_{AC}		115 V_{AC}		230 V_{AC}		265 V_{AC}	
Vout	**Enable**	**Disable**	**Enable**	**Disable**	**Enable**	**Disable**	**Enable**	**Disable**
20 V	61 W	56 W	66 W	56 W	66 W	56 W	66 W	56 W
15 V	61 W	55 W	66 W	55 W	65 W	55 W	65 W	55 W

Dual V_{CC} Management

USB-PD applications are required to function across a wide range of output voltages, presenting a challenge for controllers that are self-biased from an auxiliary winding off of the flyback transformer. As the auxiliary winding voltage will typically scale proportionally with the output voltage, it is difficult to remain within the VCC operating range of the controller across the entire output voltage operating range. The NCP1945 addresses this issue by incorporating two VCC pins, VCCL and VCCH, capable of accepting up to 30 V and 150 V, respectively. The dual VCC pins, which include a linear regulator between VCCH and VCCL, enable the NCP1945 to be biased with stacked auxiliary windings to meet the wide output operating range of the design.

Rapid Freq Foldback (RFF)

As the operating load in the application decreases, it becomes less effective to continue valley switching due to damping of the resonance. Below a certain load, the NCP1945 begins adding dead time after the 6th valley, and new drive pulses are initiated after the dead time expires. The added dead time reduces the switching frequency which

is beneficial for meeting regulatory light load and no-load power dissipation standards. Figure 17 shows the transition from RFF to 6th valley operation. During RFF, the higher QCS setpoint allows the device to operate at significantly lower frequency.

The added dead-time and switching frequency reduction is accelerated by the RFF scheme which forces an increase in the minimum peak current required for drive pulse termination. The forced increase in peak current drives the application control loop to naturally reduce the error voltage delivered to the QFB pin, which then increases the amount of dead time added after the 6^{th} valley. During this mode, dead time continues to be added until skip mode is reached, or the switching frequency reaches its minimum level of 25 kHz.

GaN Direct Drive Voltage Clamp

With the proliferation of Gallium Nitride transistors, more USB-PD applications are using GaN to improve board performance. Using GaN transistors usually entails the use of a driver to accommodate the 6 V gate of GaN FETs, which increases the number of components and increases board costs. The NCP1945BA OPN is capable of directly driving a GaN transistor without the need for a driver. The drive voltage of both the PDRV and QDRV pins are clamped at 6.5 V. The diode on the turn path makes it such that the gate of the GaN transistors only see 6 V. Figure 19 shows the clamped drive voltage for GaN, as well as the voltage at the gate of the GaN device.

Programmable Constant Current Overload (CC Overload)

The NCP1945 incorporates a novel current limit technique that utilizes the demagnetization timing measured at QZCD to produce an internal voltage proportional to the application load current. The internal voltage representative of the load current is then compared against a threshold, programmed by the QCCLIM pin. The device enables the overload timer whenever the threshold is exceeded. This technique produces an overload current limit independent of the application's output voltage and overcoming the inaccuracy of using primary-side cycle-by-cycle peak current limit for enabling overload protection. Figure 20 shows a plot of the CC overload threshold for all output voltage conditions.

BOARD PERFORMANCE

Efficiency

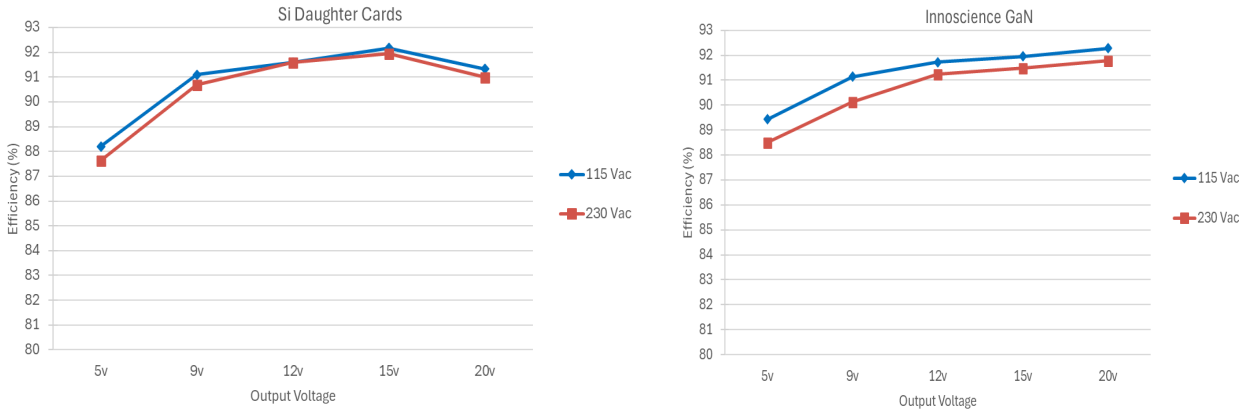


Figure 7. 4-point Average Efficiency

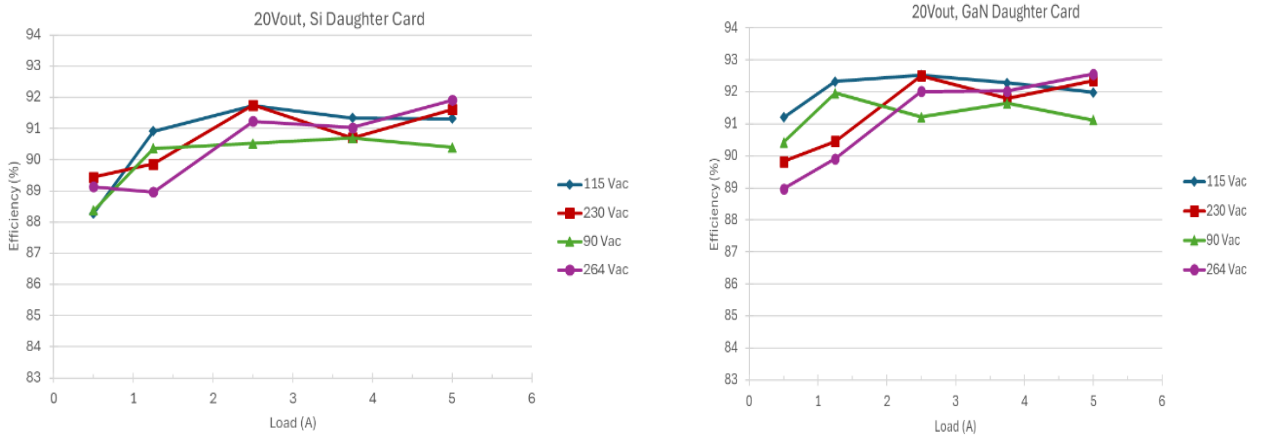


Figure 8. 20 V Output Efficiency Across Line and Load

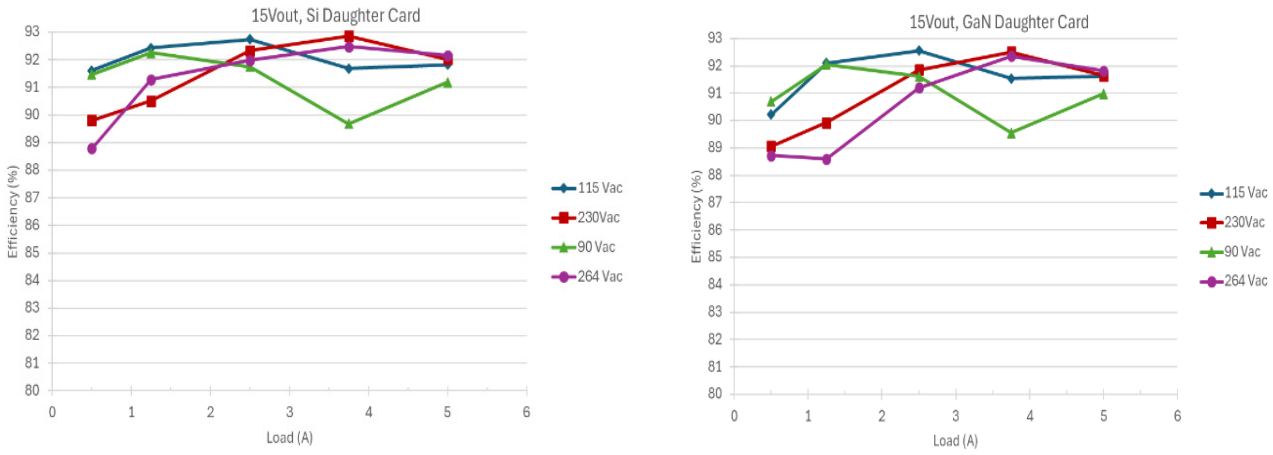


Figure 9. 15 V Output Efficiency Across Line and Load

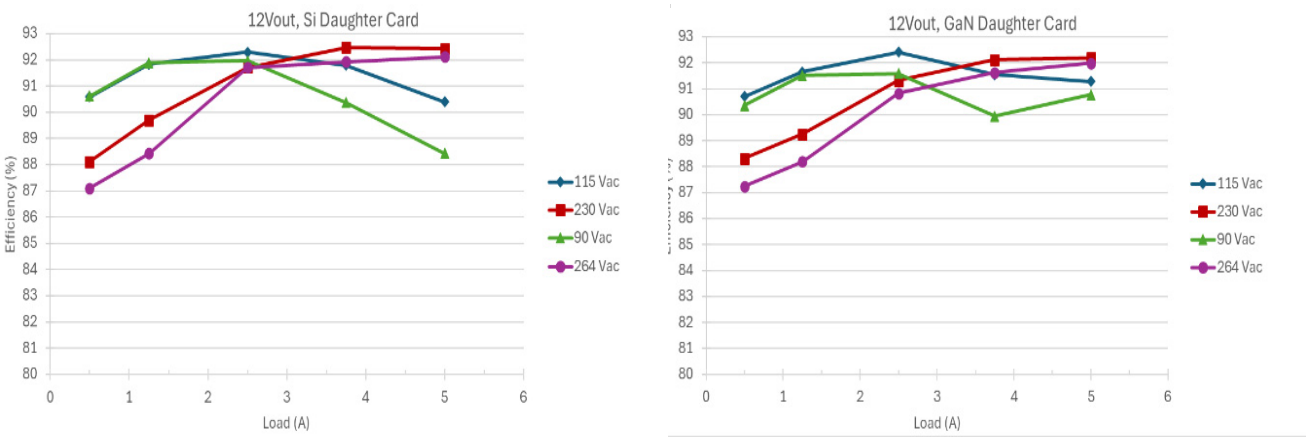


Figure 10. 12 V Output Efficiency Across Line and Load

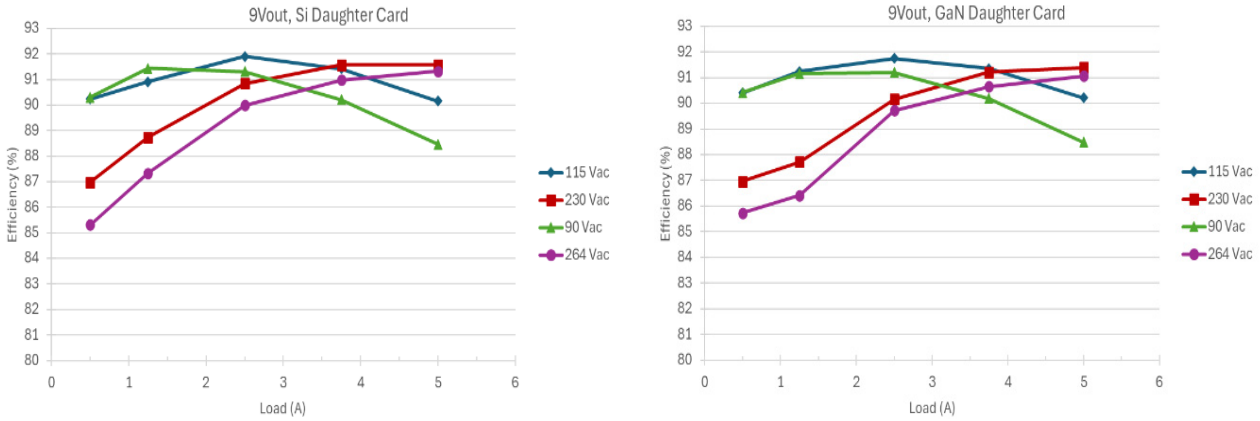


Figure 11. 9 V Output Efficiency Across Line and Load

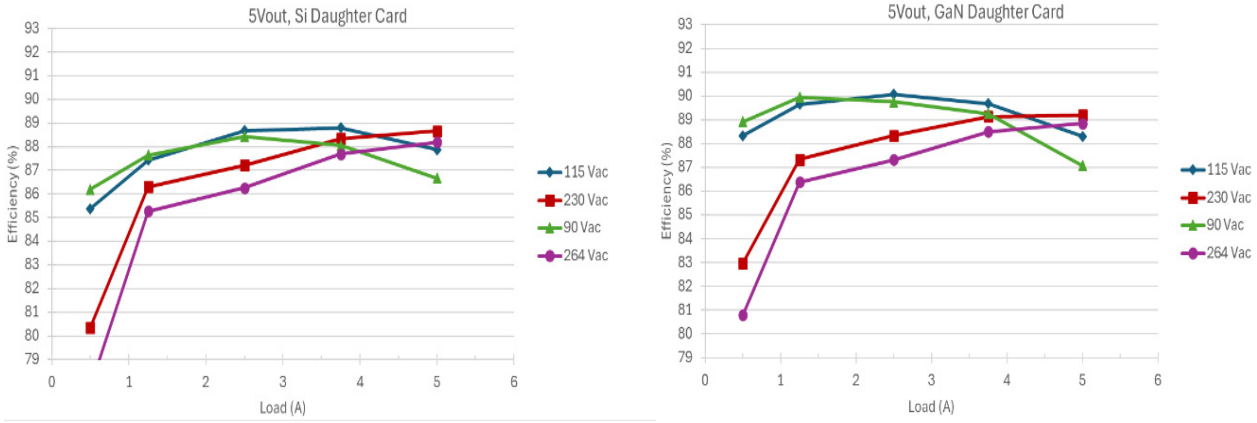


Figure 12. 5 V Output Efficiency Across Line and Load

Low Load and No-Load Performance

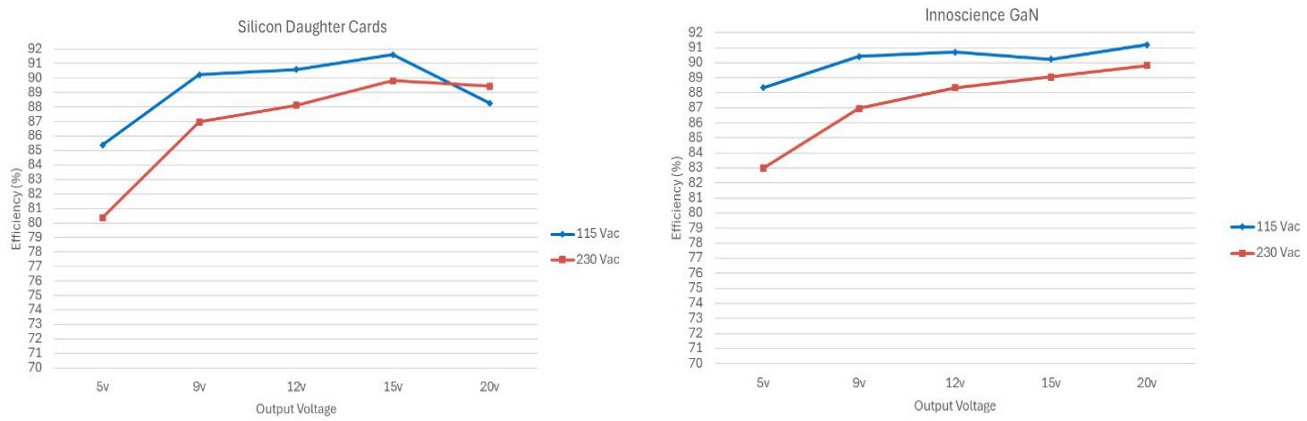


Figure 13. 10% Load Efficiency Across Various Output Voltages

Si MOSFET

No Load Power Consumption (mW)		
Output Voltage	**115Vac**	**230Vac**
5V	64.26	87.34
9V	62.19	83.85
15V	39.37	59.56
20V	24.64	42.58

Innoscience GaN

No Load Power Consumption (mW)		
Output Voltage	**115Vac**	**230Vac**
20V	63.00	85.63
15V	60.97	82.21
9V	38.60	58.39
5V	23.79	41.48

Si MOSFET

150mW Load Power Consumption			Spec (mW)
Output Voltage	115Vac	230Vac	
20V	250.70	264.67	270 mW

Innoscience GaN

150mW Load Power Consumption			Spec (mW)
Output Voltage	115Vac	230Vac	
20V	237.467	263.95	270 mW

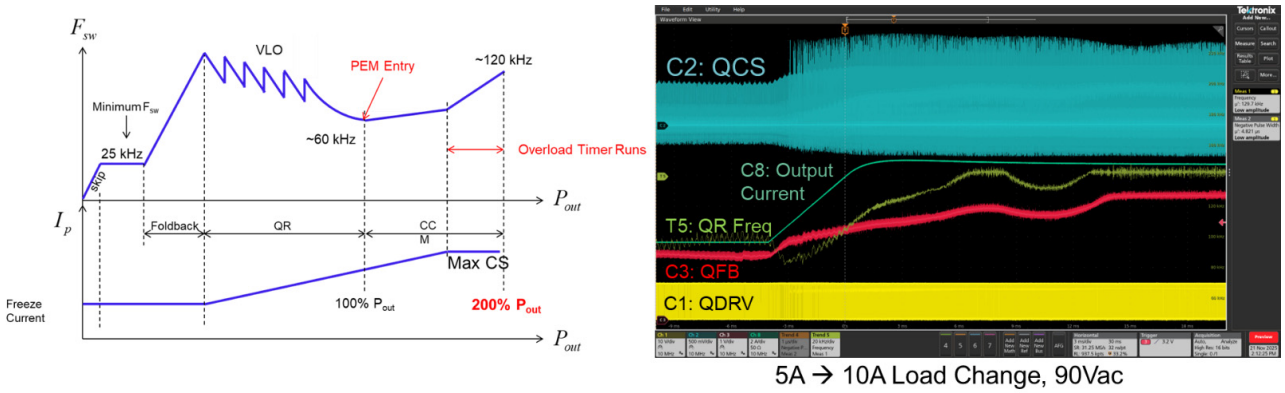


Figure 14. Waveform Demonstrating High Level Behavior of the NCP1945 Entering PEM

Figure 15. 90 Vac to 264 Vac Line Transition

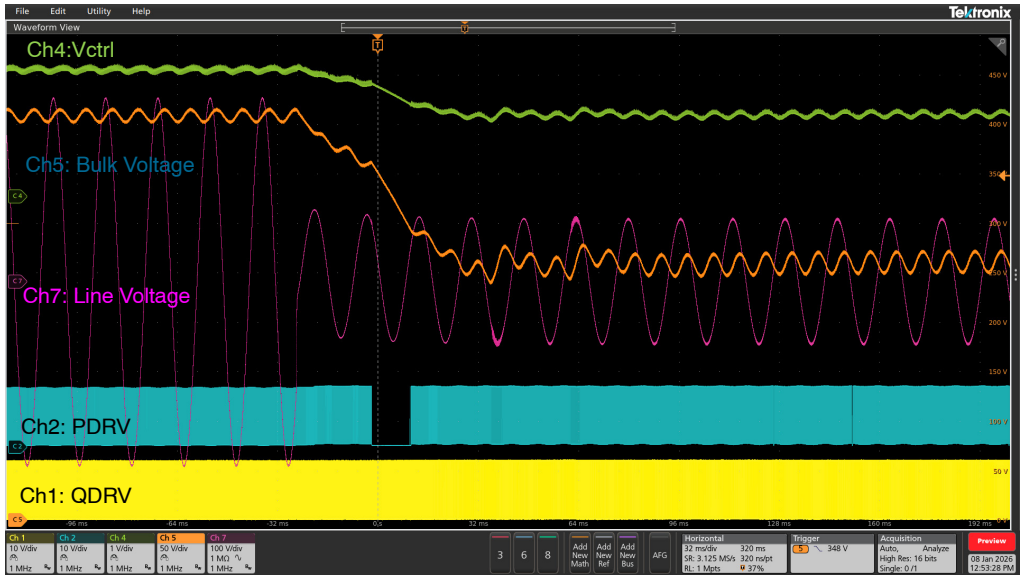


Figure 16. 264 Vac to 90 Vac Line Transition

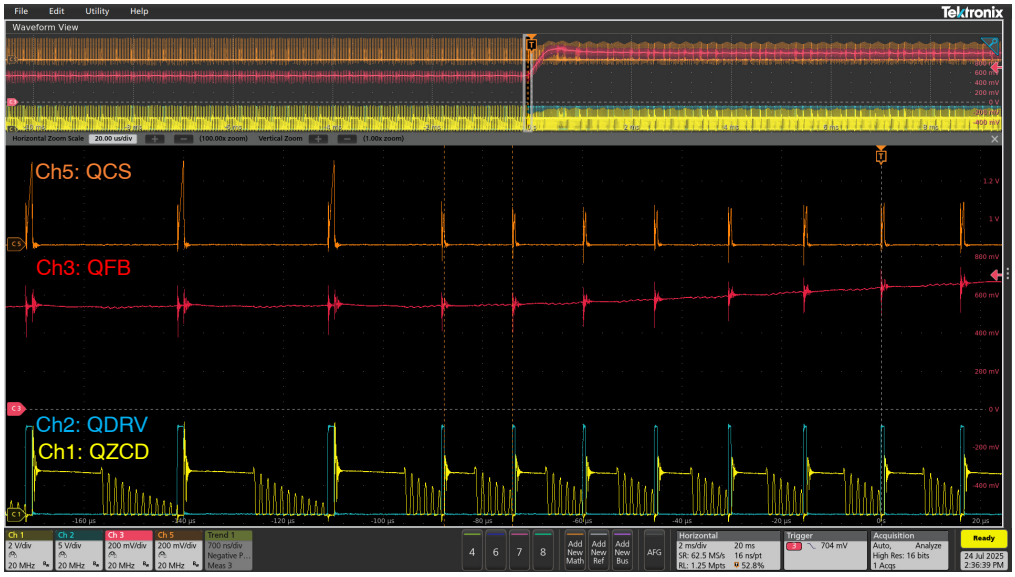


Figure 17. NCP1945 Transitioning from RFF to Normal Valley Operation

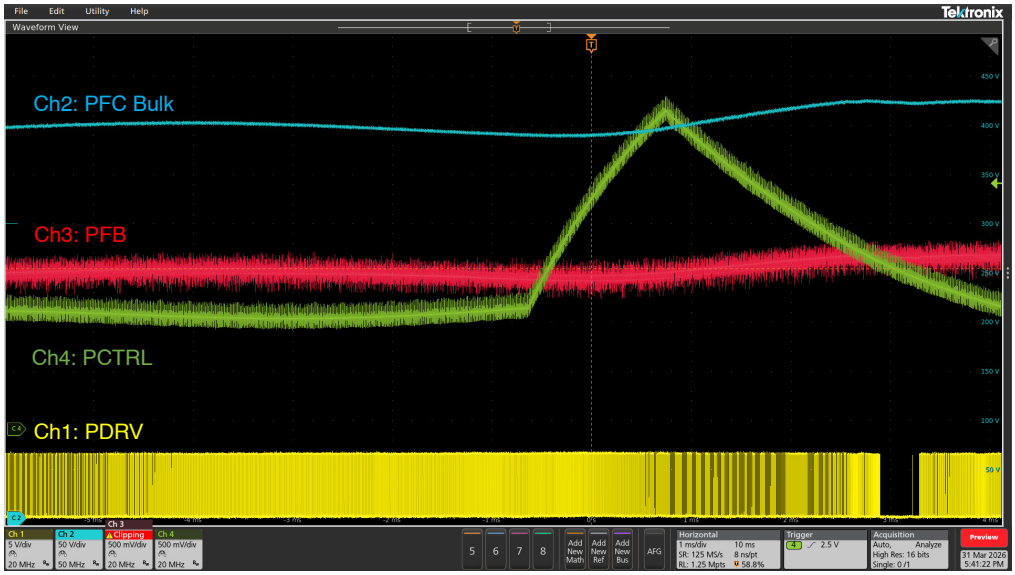


Figure 18. DRE Starting Due to Sharp Load Transient

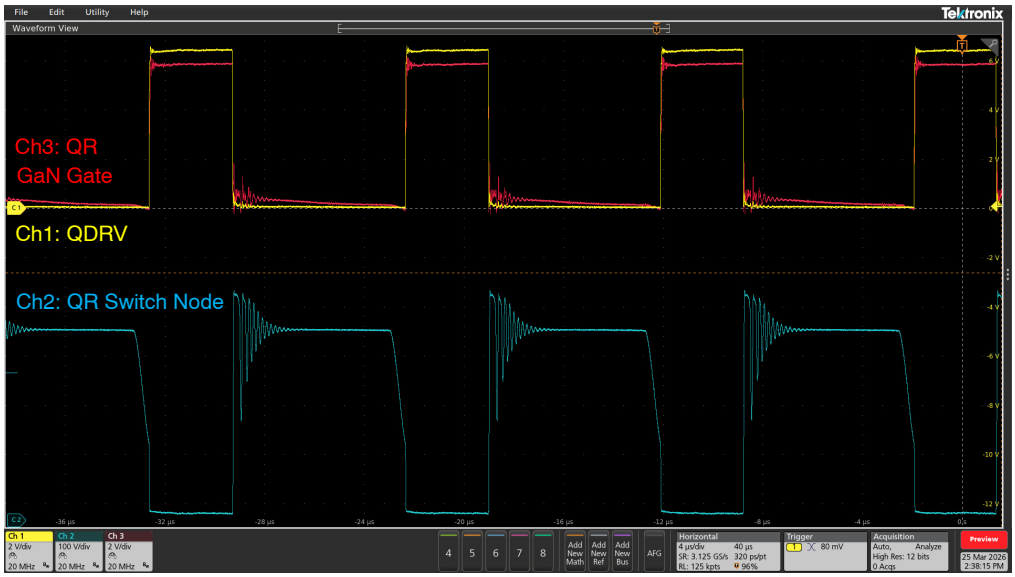


Figure 19. Drive and Switch Node Voltage of GaN FET

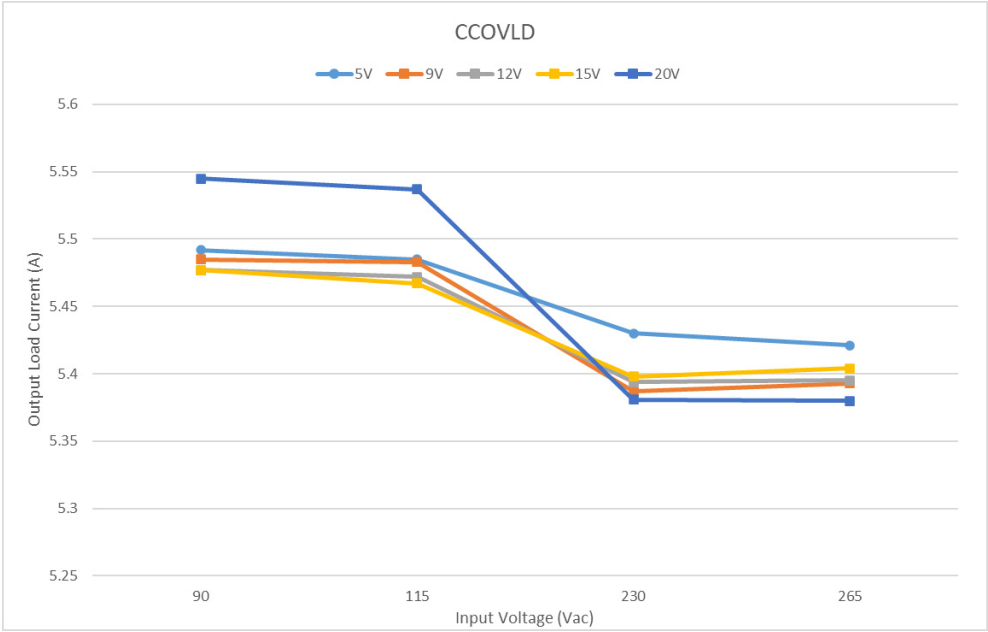


Figure 20. CC Overload Threshold Across Line Voltage for Different Output Voltages

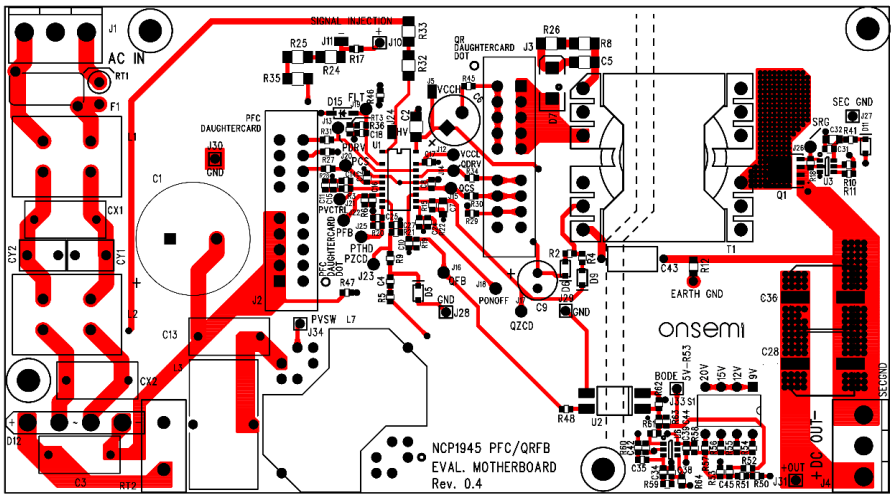


Figure 21. Motherboard Layout Topside

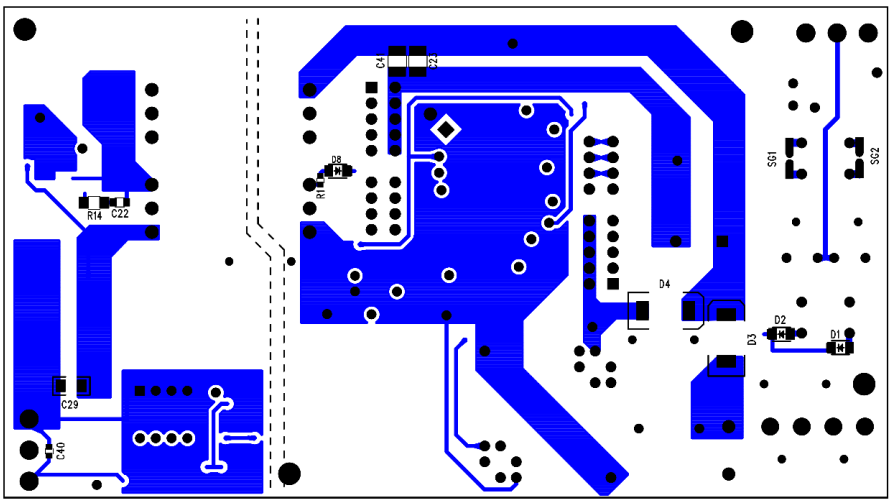


Figure 22. Motherboard Layout Bottomside

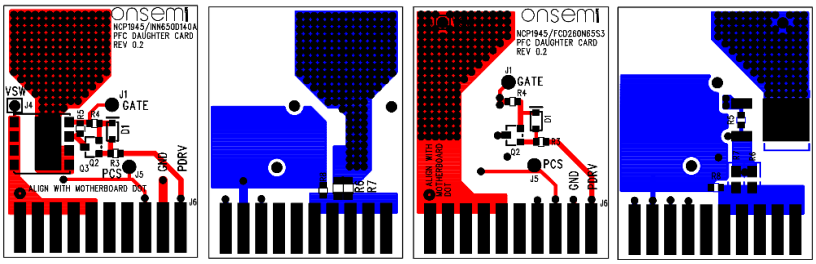


Figure 23. PFC Daughter Card Layout for Si and GaN FETs

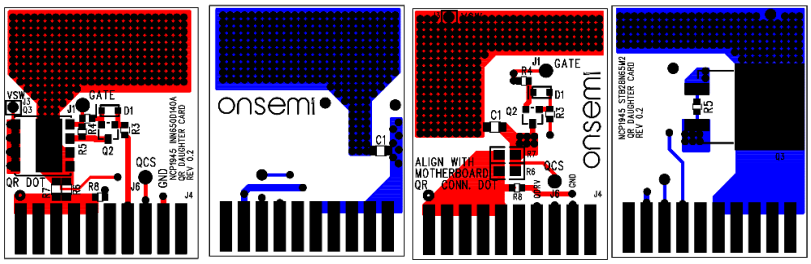


Figure 24. QR Daughter Card Layout for Si and GaN FETs

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	4/13/2026
1	Replaced Figure 1; updated Flyback Transformer and PFC inductor specification figures; added waveform labels in Figures 15–19.	5/22/2026

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales