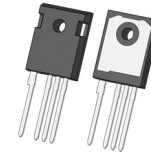


Silicon Carbide (SiC) JFET – EliteSiC, Power N-Channel, TO247-4, 750 V, 4.8 mohm

UJ4N075005K4S


 TO247-4
 CASE 340AN

Description

onsemi's UJ4N075005K4S is a 750 V, 4.8 mΩ High-Performance Gen 4 Normally-On SiC JFET Transistor. This device exhibits Ultra-low On resistance ($R_{DS(ON)}$) in a TO247-4L Package, making it an ideal fit to address the Challenging Thermal Constraints of Solid-state Circuit Breakers and Relay Applications. Additionally, the JFET is a Robust Device Technology Capable of the High-Energy Switching Required in Circuit Protection Applications.

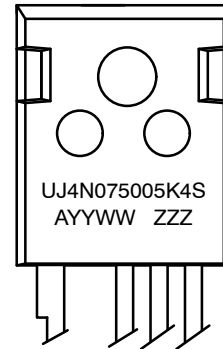
Features

- Single Digit On-Resistance
- Operating Temperature: 175 °C (Max)
- High Pulse Current Capability
- Excellent Device Robustness
- Silver-Sintered Die Attach for Excellent Thermal Resistance
- Low Intrinsic Capacitance
- Short Circuit Rated
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Typical Applications

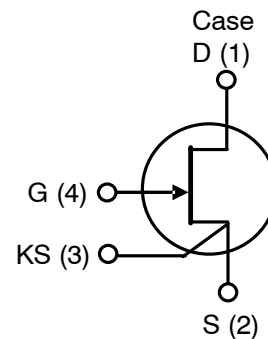
- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control
- Induction Heating

MARKING DIAGRAM



UJ4N075005K4S	= Specific Device Code
A	= Assembly Location
YY	= Year
WW	= Work Week
ZZZ	= Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

UJ4N075005K4S

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		750	V
Gate-Source Voltage	V_{GS}	DC	-30 to +3	V
		AC (Note 1)	-30 to +30	
Continuous Drain Current (Note 2)	I_D	$T_C < 127\text{ }^\circ\text{C}$	120	A
Pulsed Drain Current (Note 3)	I_{DM}	$T_C = 25\text{ }^\circ\text{C}$	588	A
Short Circuit Withstand Time	t_{SC}	$V_{DS} = 400\text{ V}$, $T_{J(\text{START})} = 175\text{ }^\circ\text{C}$	5	μS
Power Dissipation	P_{TOT}	$T_C = 25\text{ }^\circ\text{C}$	714	W
Maximum Junction Temperature	$T_{J,\text{max}}$		175	$^\circ\text{C}$
Operating and Storage Temperature	T_J , T_{STG}		-55 to 175	$^\circ\text{C}$
Max. Lead Temperature for Soldering, 1/8" from Case for 5 seconds	T_L		250	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- +30 V AC Rating Applies for Turn-on Pulses <200 ns applied with external $R_G > 1\Omega$.
- Limited by Bondwires
- Pulse width t_p limited by $T_{J,\text{max}}$

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Value			
			Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		-	0.16	0.21	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_J = +25\text{ }^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC						
Drain-Source Breakdown Voltage	BV_{DS}	$V_{GS} = -20\text{ V}, I_D = 2\text{ mA}$	750	–	–	V
Total Drain Leakage Current	I_{DSS}	$V_{DS} = 750\text{ V}, V_{GS} = -20\text{ V}, T_J = 25\text{ }^\circ\text{C}$	–	13	120	μA
		$V_{DS} = 750\text{ V}, V_{GS} = -20\text{ V}, T_J = 175\text{ }^\circ\text{C}$	–	65	–	
Total Gate Leakage Current	I_{GSS}	$V_{GS} = -20\text{ V}, T_J = 25\text{ }^\circ\text{C}$	–	0.1	100	μA
		$V_{GS} = -20\text{ V}, T_J = 175\text{ }^\circ\text{C}$	–	0.3	–	μA
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 2\text{ V}, I_D = 80\text{ A}, T_J = 25\text{ }^\circ\text{C}$	–	4.8	–	$\text{m}\Omega$
		$V_{GS} = 0\text{ V}, I_D = 80\text{ A}, T_J = 25\text{ }^\circ\text{C}$	–	5.4	6.6	
		$V_{GS} = 2\text{ V}, I_D = 80\text{ A}, T_J = 175\text{ }^\circ\text{C}$	–	10.4	–	
		$V_{GS} = 0\text{ V}, I_D = 80\text{ A}, T_J = 175\text{ }^\circ\text{C}$	–	11.9	–	
Gate Threshold Voltage	$V_{G(th)}$	$V_{DS} = 5\text{ V}, I_D = 180\text{ mA}$	–8.3	–6.0	–3.7	V
Gate Resistance	R_G	$f = 1\text{ MHz}, \text{Open Drain}$	–	0.8	–	Ω

TYPICAL PERFORMANCE – DYNAMIC

Input Capacitance	C_{iss}	$V_{DS} = 400\text{ V}, V_{GS} = -20\text{ V}, f = 100\text{ kHz}$	–	3028	–	pF
Output Capacitance	C_{oss}		–	364	–	
Reverse Transfer Capacitance	C_{rss}		–	360	–	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = -20\text{ V}$	–	448	–	pF
C_{OSS} Stored Energy	E_{OSS}	$V_{DS} = 400\text{ V}, V_{GS} = -20\text{ V}$	–	36	–	μJ
Total Gate Charge	Q_G	$V_{DS} = 400\text{ V}, I_D = 80\text{ A}, V_{GS} = -18\text{ V to } 0\text{ V}$	–	400	–	nC
Gate-Drain Charge	Q_{GD}		–	270	–	
Gate-Source Charge	Q_{GS}		–	60	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE DIAGRAM

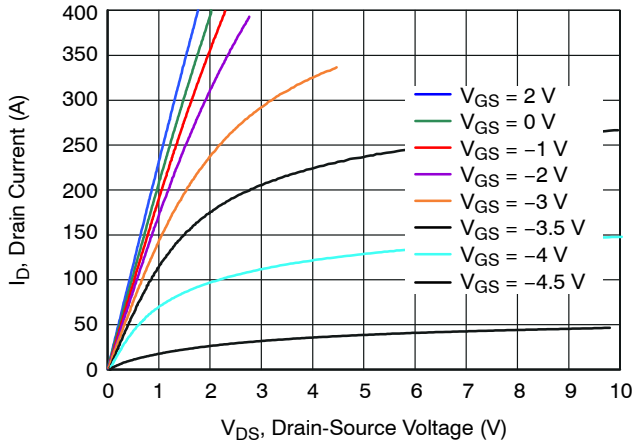


Figure 1. Typical Output Characteristics at $T_J = -55\text{ }^\circ\text{C}$, $t_p < 250\text{ }\mu\text{s}$

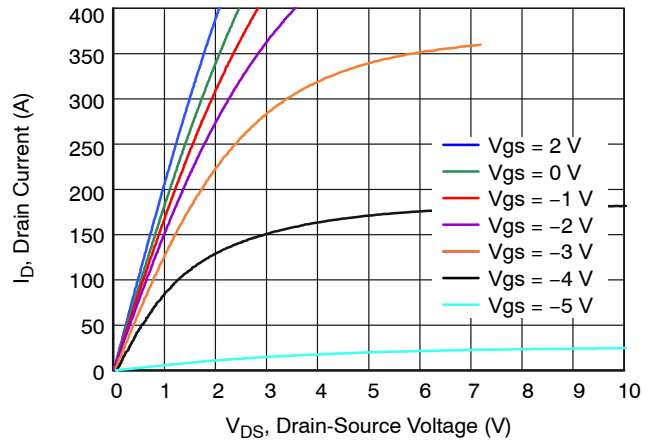


Figure 2. Typical Output Characteristics at $T_J = 25\text{ }^\circ\text{C}$, $t_p < 250\text{ }\mu\text{s}$

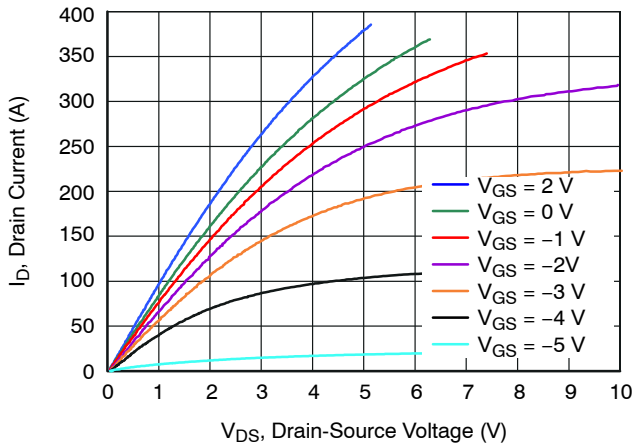


Figure 3. Typical Output Characteristics at $T_J = 175\text{ }^\circ\text{C}$, $t_p < 250\text{ }\mu\text{s}$

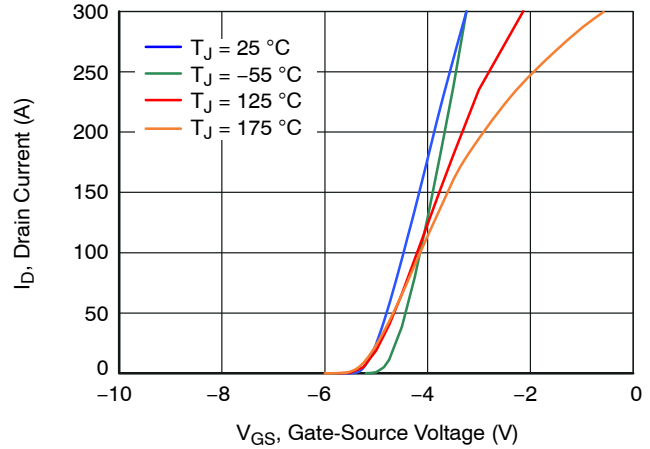


Figure 4. Typical Transfer Characteristics at $V_{DS} = 5\text{ V}$

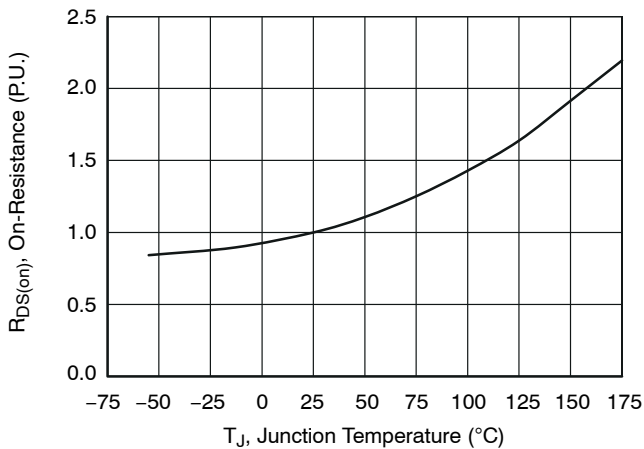


Figure 5. Normalized On-Resistance Vs. Temperature at $V_{GS} = 0\text{ V}$ and $I_D = 80\text{ A}$

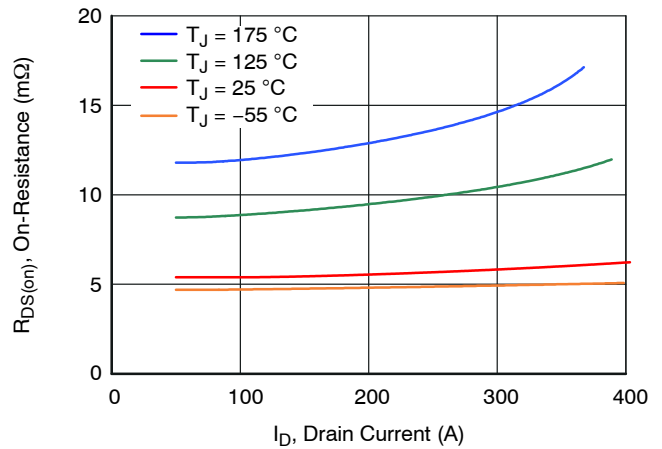


Figure 6. Typical Drain-Source On-Resistance $V_{GS} = 0\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

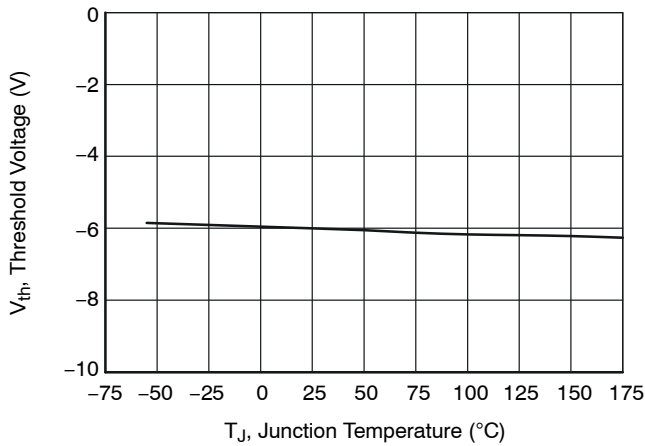


Figure 7. Threshold Voltage vs. Junction Temperature at $V_{DS} = 5\text{ V}$ and $I_D = 180\text{ mA}$

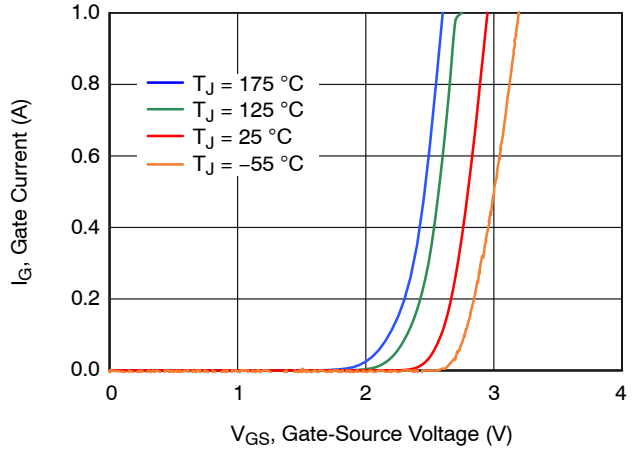


Figure 8. Typical Gate Forward Current at $V_{DS} = 0\text{ V}$

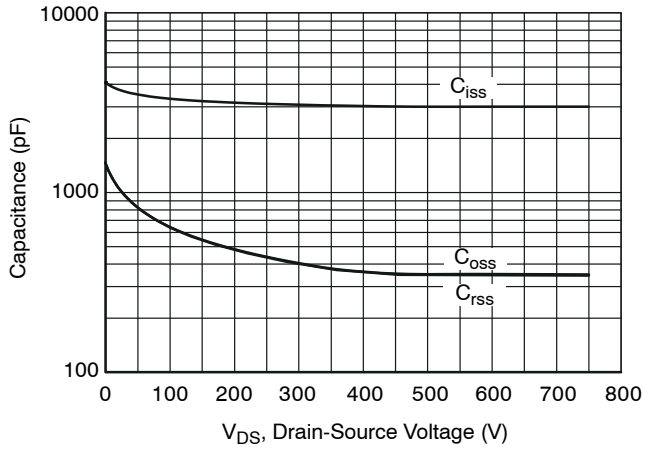


Figure 9. Typical Capacitances at $f = 100\text{ KHz}$ and $V_{GS} = -20\text{ V}$

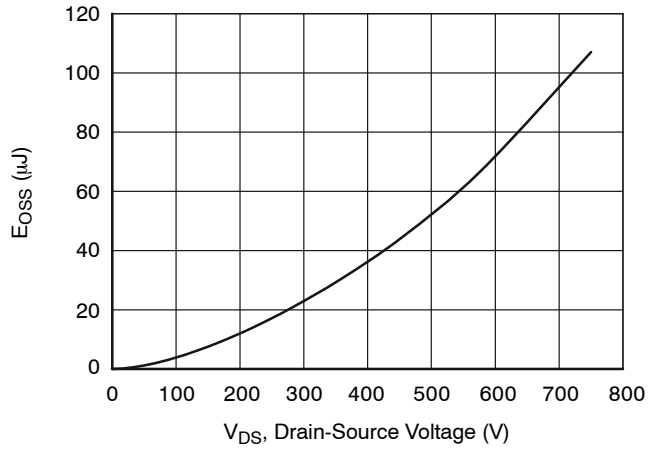


Figure 10. Typical Stored Energy in C_{OSS} at $V_{GS} = -20\text{ V}$

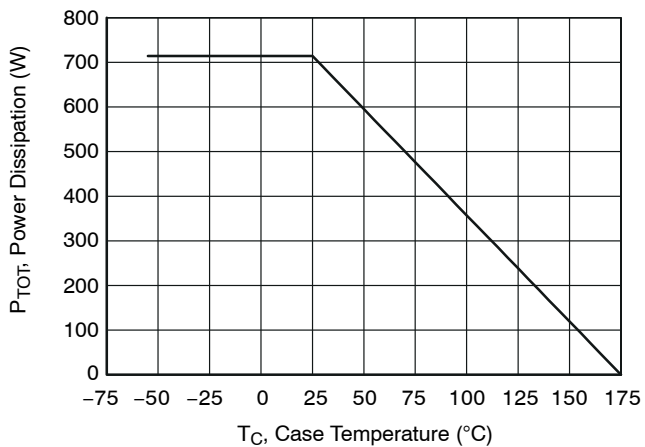


Figure 11. Total Power Dissipation

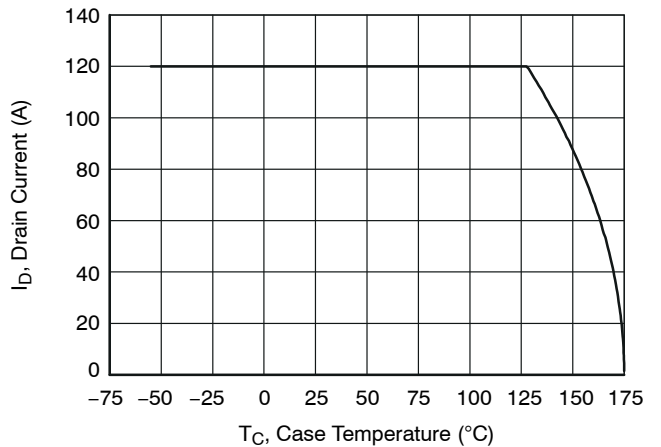


Figure 12. DC Drain Current Derating

UJ4N075005K4S

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

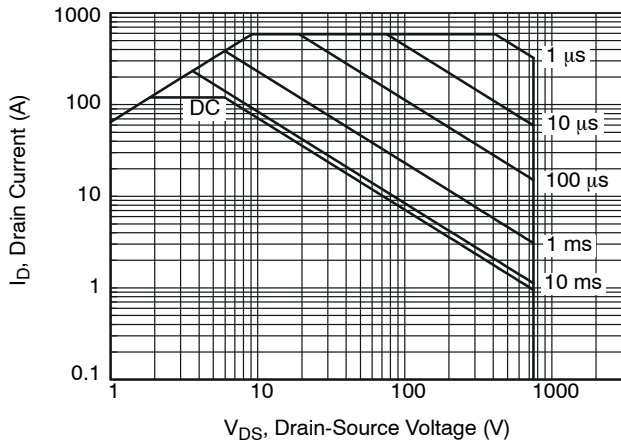


Figure 13. Safe Operation Area at $T_C = 25\text{ }^\circ\text{C}$, Parameter t_p

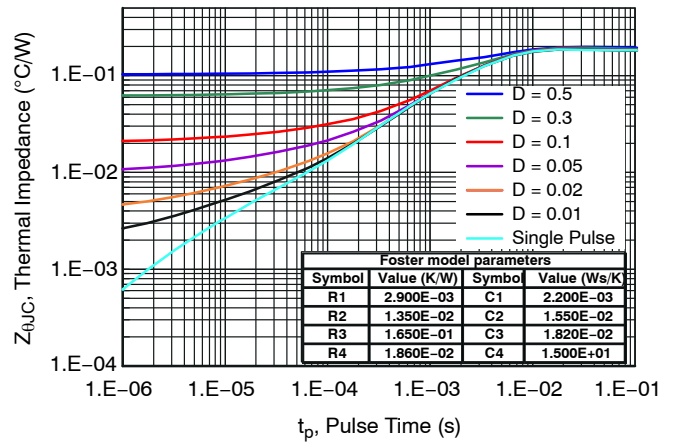


Figure 14. Maximum Transient Thermal Impedance

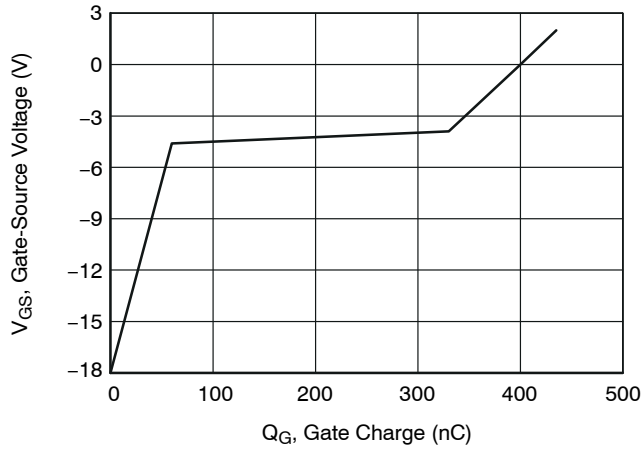
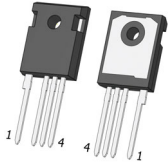


Figure 15. Typical Gate Charge at $V_{DS} = 400\text{ V}$ and $I_D = 80\text{ A}$

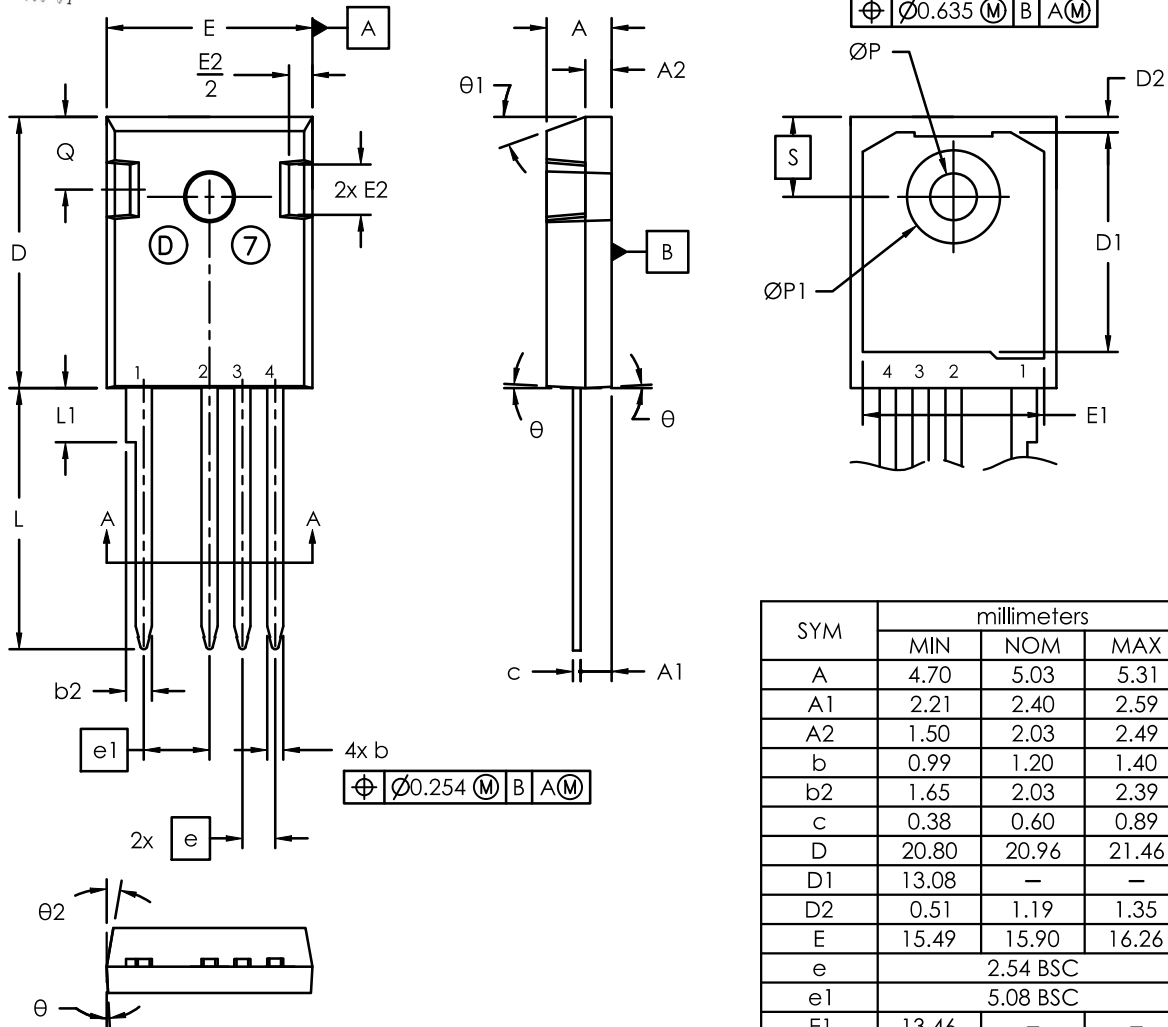
ORDERING INFORMATION

Part Number	Marking	Package	Shipping
UJ4N075005K4S	UJ4N075005K4S	TO247-4 (Pb-Free, Halogen Free)	600 Units / Tube



TO247-4 15.90x20.96x5.03, 5.44P
CASE 340AN
ISSUE E

DATE 20 JUN 2025



$\text{M} \text{ B } \text{A} \text{ (M)}$
 $\text{M} \text{ B } \text{A} \text{ (M)}$
 $\text{M} \text{ B } \text{A} \text{ (M)}$

$\text{M} \text{ B } \text{A} \text{ (M)}$
 $\text{M} \text{ B } \text{A} \text{ (M)}$

SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
c	0.38	0.60	0.89
D	20.80	20.96	21.46
D1	13.08	—	—
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	2.54 BSC		
e1	5.08 BSC		
E1	13.46	—	—
E2	3.43	3.89	5.20
L	19.81	20.17	20.32
L1	—	—	4.50
ØP	3.40	3.60	3.80
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.17 BSC		
θ	3°		
θ1	20°		
θ2	10°		

NOTE:

1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.
5. Through Hole diameter value = End Hole diameter
6. PCB Through Hole pattern as per IPC-2221/IPC-2222

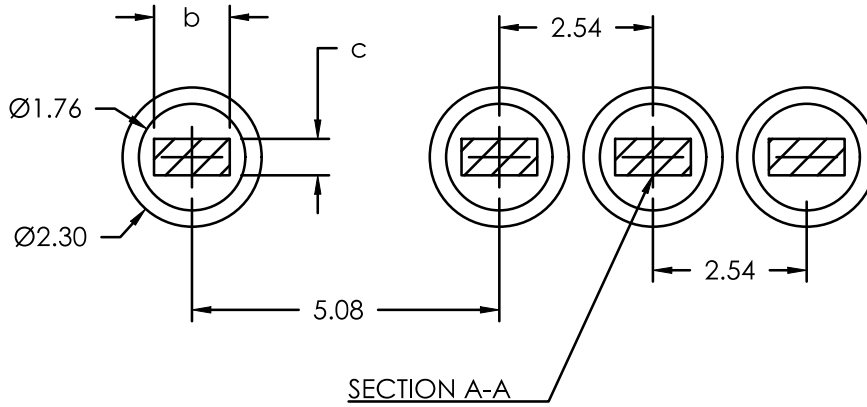
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TO247-4 15.90x20.96x5.03, 5.44P
CASE 340AN
ISSUE E

DATE 20 JUN 2025

RECOMMENDED PCB THROUGH HOLE



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.
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