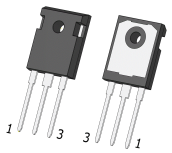
Silicon Carbide (SiC) JFET – EliteSiC, Power N-Channel, TO247-3, 1200 V, 70 mohm

UJ3N120070K3S



TO247-3
CASE 340AK

Description

onsemi offers the high-performance G3 SiC normally-on JFET transistors. This series exhibits ultra-low on resistance ($R_{DS(ON)}$) and gate charge (Q_G) allowing for low conduction and switching loss. The device normally-on characteristics with low $R_{DS(ON)}$ at $V_{GS} = 0$ V is also ideal for current protection circuits without the need for active control, as well as for cascode operation.

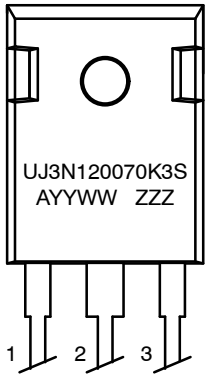
Features

- Typical On-resistance $R_{DS(on)}$, Typ of 70 mΩ
- Voltage Controlled
- Maximum Operating Temperature of 175 °C
- Extremely Fast Switching not Dependent on Temperature
- Low Gate Charge
- Low Intrinsic Capacitance
- This Device is Pb-Free, Halogen Free and is ROHS Compliant

Typical Applications

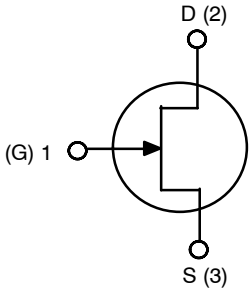
- Over Current Protection Circuits
- DC–AC Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating

MARKING DIAGRAM



UJ3N120070K3S	= Specific Device Code
A	= Assembly Location
YY	= Year
WW	= Work Week
ZZZ	= Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		1200	V
Gate-source Voltage	V_{GS}	DC	−20 to +3	V
		AC (Note 1)	−20 to +20	
Continuous Drain Current (Note 2)	I_D	T_C = 25 °C	33.5	A
		T_C = 100 °C	24.5	
Pulsed Drain Current (Note 3)	I_{DM}	T_C = 25 °C	85	A
Power Dissipation	P_{tot}	T_C = 25 °C	254	W
Maximum Junction Temperature	$T_{J, max}$		175	°C
Operating and Storage Temperature	T_J, T_{STG}		−55 to 175	°C
Max. Lead Temperature for Soldering, 1/8” from Case for 5 Seconds	T_L		250	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. +20 V AC rating applies for turn-on pulses <200 ns applied with external R_G > 1 Ω.
2. Limited by $T_{J, max}$.
3. Pulse width tp limited by $T_{J, max}$

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Value			Unit
			Min	Typ	Max	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		–	0.45	0.59	°C/W

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC						
Drain-source Breakdown Voltage	BV_{DS}	V_{GS} = −20 V, I_D = 1 mA	1200	–	–	V
Total Drain Leakage Current	I_D	V_{DS} = 1200 V, V_{GS} = −20 V, T_J = 25 °C	–	5	30	μA
		V_{DS} = 1200 V, V_{GS} = −20 V, T_J = 175°C	–	18	–	
Total Gate Leakage Current	I_G	V_{GS} = −20 V, T_J = 25 °C	–	5	50	μA
		V_{GS} = −20 V, T_J = 175 °C	–	20	–	
Drain-source On-resistance	$R_{DS(on)}$	V_{GS} = 2 V, I_D = 10 A, T_J = 25°C	–	63	–	mΩ
		V_{GS} = 0 V, I_D = 10 A, T_J = 25°C	–	70	90	
		V_{GS} = 2 V, I_D = 10 A, T_J = 175°C	–	139	–	
		V_{GS} = 0 V, I_D = 10 A, T_J = 175°C	–	154	–	
Gate Threshold Voltage	$V_{G(th)}$	V_{DS} = 5 V, I_D = 35 mA	−14	−11.5	−6	V
Gate Resistance	R_G	f = 1 MHz, open drain	–	3.3	–	Ω
TYPICAL PERFORMANCE – DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 100 V, V_{GS} = −20 V, f = 100 kHz	–	985	–	pF
Output Capacitance	C_{oss}		–	100	–	
Reverse Transfer Capacitance	C_{rss}		–	95	–	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	V_{DS} = 0 V to 800 V, V_{GS} = −20 V	–	52	–	pF
Total Gate Charge	Q_G	V_{DS} = 800 V, I_D = 25 A, V_{GS} = −18 V to 0 V	–	116	–	nC
Gate-drain Charge	Q_{GD}		–	63	–	
Gate-source Charge	Q_{GS}		–	11	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 800 V, I_D = 25 A, Gate Driver = −18 V to 0 V, $R_{G, EXT}$ = 1 Ω, Inductive Load, FWD: UJ2D1215T T_J = 25 °C	–	17	–	ns
Rise Time	t_r		–	25	–	
Turn-off Delay Time	$t_{d(off)}$		–	29	–	
Fall Time	t_f		–	39	–	
Turn-on Energy	E_{ON}		–	434	–	μJ
Turn-off Energy	E_{OFF}		–	393	–	
Total Switching Energy	E_{TOTAL}		–	827	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 800 V, I_D = 25 A, Gate Driver = −18 V to 0 V, $R_{G, EXT}$ = 1 Ω, Inductive Load, FWD: UJ2D1215T T_J = 150 °C	–	17	–	ns
Rise Time	t_r		–	23	–	
Turn-off Delay Time	$t_{d(off)}$		–	25	–	
Fall Time	t_f		–	24	–	
Turn-on Energy	E_{ON}		–	418	–	μJ
Turn-off Energy	E_{OFF}		–	278	–	
Total Switching Energy	E_{TOTAL}		–	696	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE DIAGRAMS

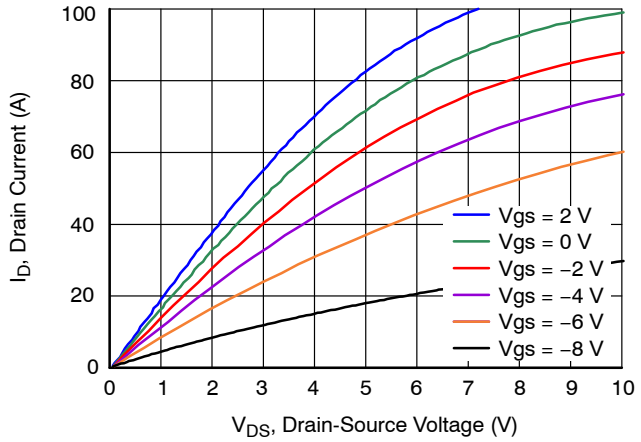


Figure 1. Typical Output Characteristics at T_J = −55 °C

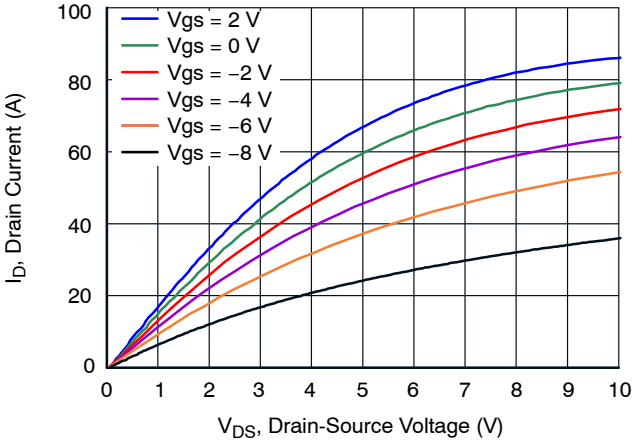


Figure 2. Typical Output Characteristics at T_J = 25 °C

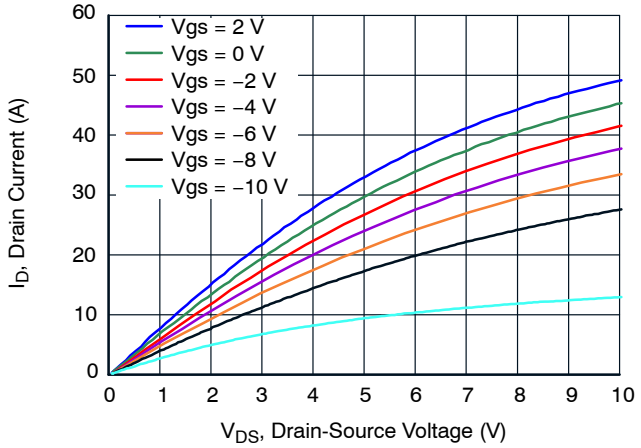


Figure 3. Typical Output Characteristics at T_J = 175 °C

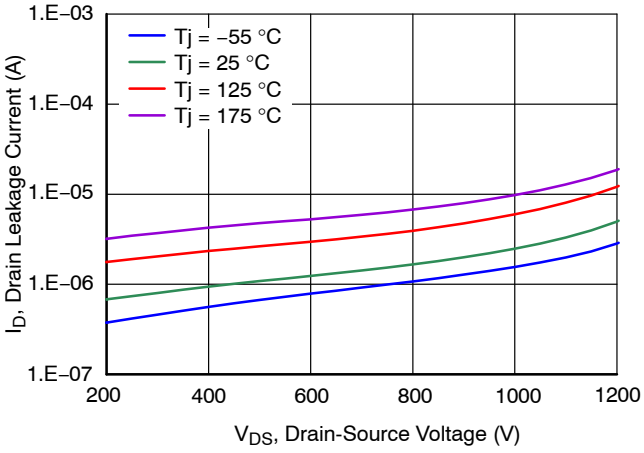


Figure 4. Typical Drain-Source Leakage at V_{GS} = −20 V

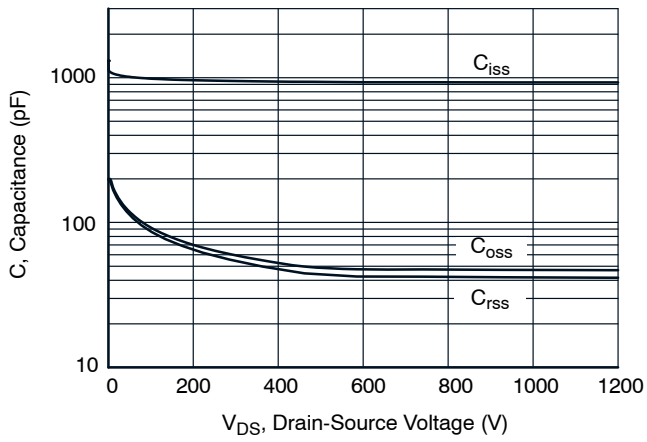


Figure 5. Typical Capacitances at 100 kHz and V_{GS} = −20 V

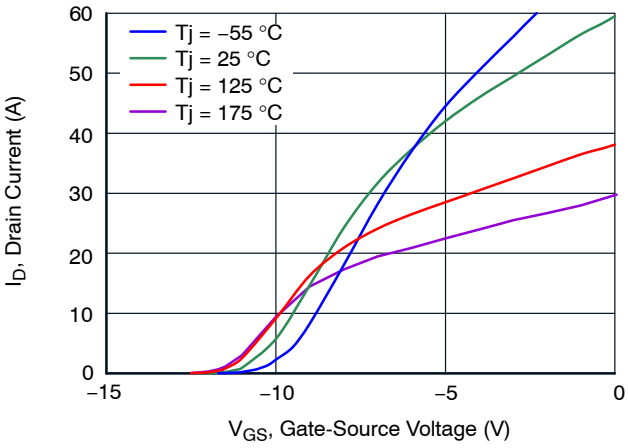


Figure 6. Typical Transfer Characteristics at V_{DS} = 5 V

TYPICAL PERFORMANCE DIAGRAMS (continued)

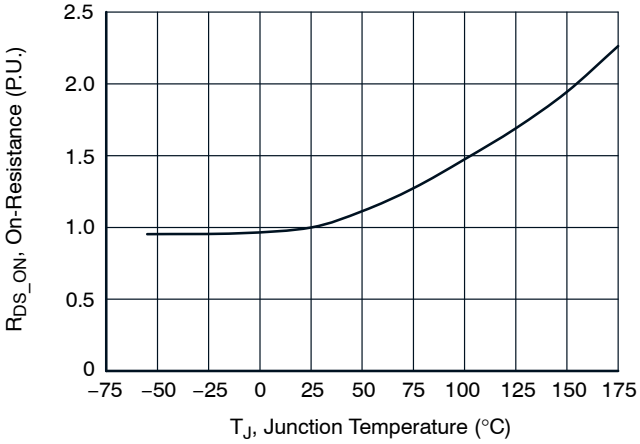


Figure 7. Normalized On-Resistance vs. Temperature at V_{GS} = 0 V and I_D = 10 A

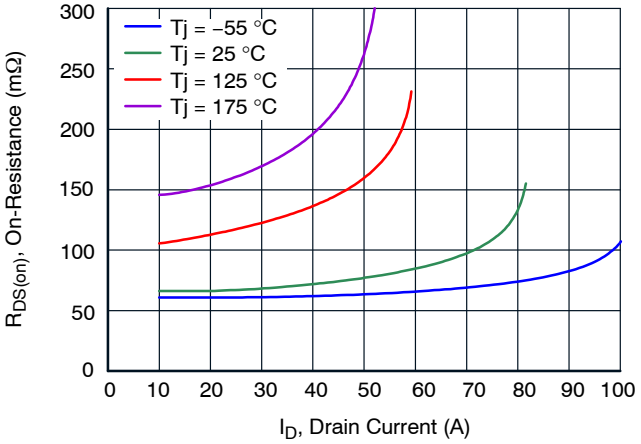


Figure 8. Typical Drain-Source On-Resistance at V_{GS} = 0 V

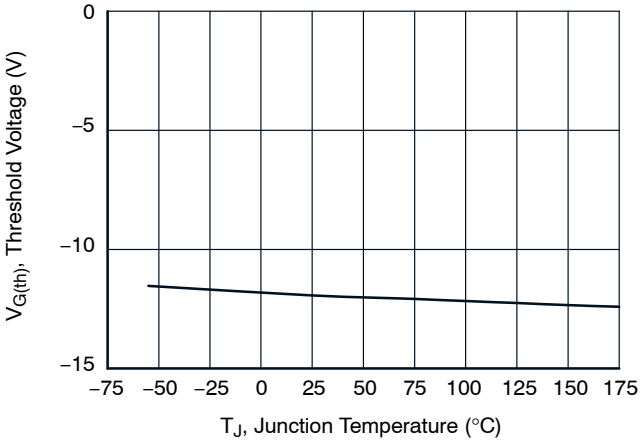


Figure 9. Threshold Voltage vs. T_J at V_{DS} = 5 V and I_D = 35 mA

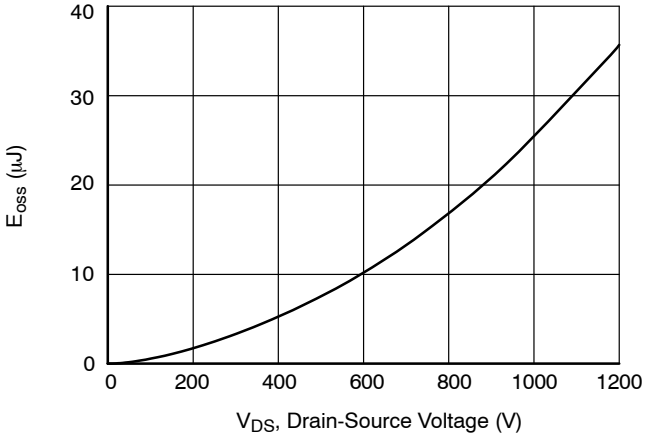


Figure 10. Typical Stored Energy in C_{oss} at V_{GS} = −20 V

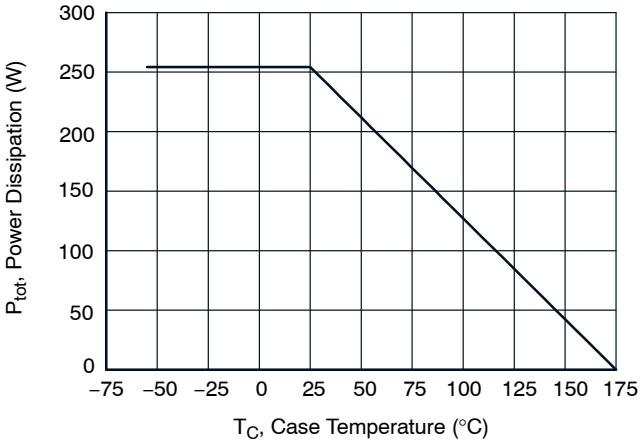


Figure 11. Total Power Dissipation

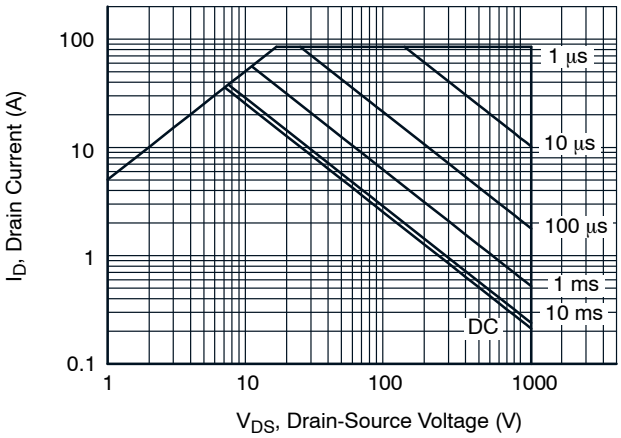


Figure 12. Safe Operation Area T_C = 25 °C, Parameter t_p

TYPICAL PERFORMANCE DIAGRAMS (continued)

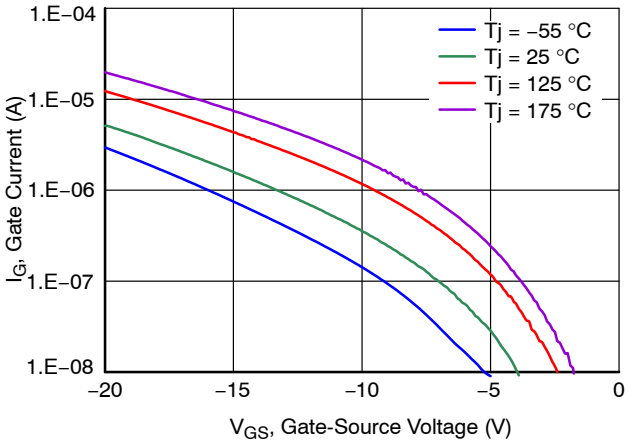


Figure 13. Typical Gate Leakage Current at V_{DS} = 0 V

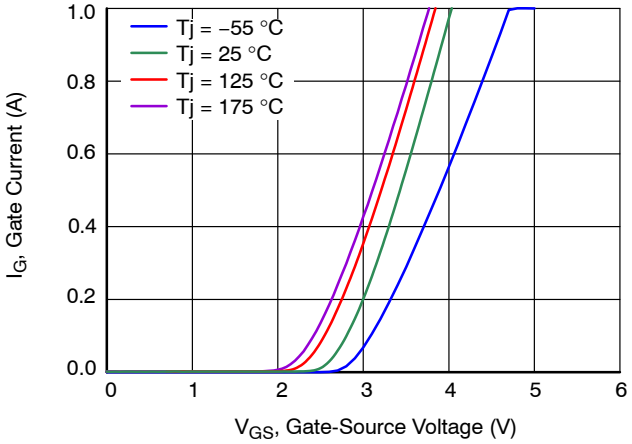


Figure 14. Typical Gate Forward Current at V_{DS} = 0 V

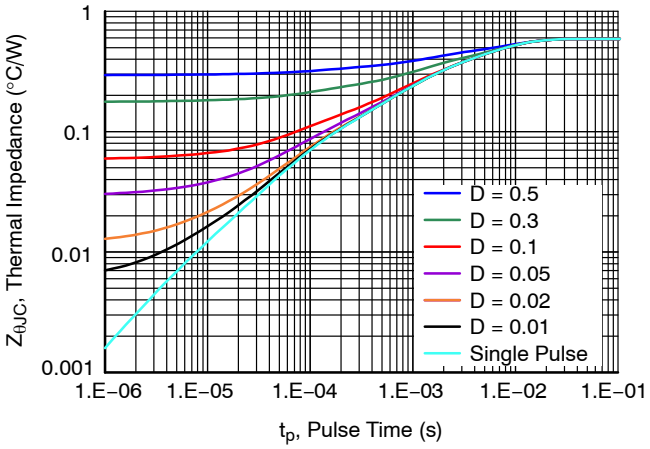


Figure 15. Maximum Transient Thermal Impedance

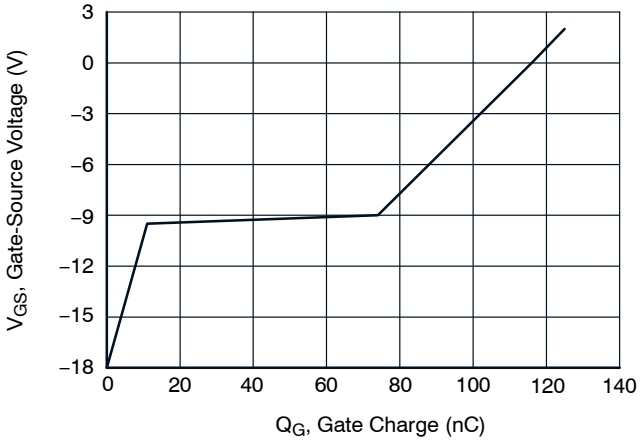


Figure 16. Typical Gate Charge at V_{DS} = 800 V and I_D = 25 A

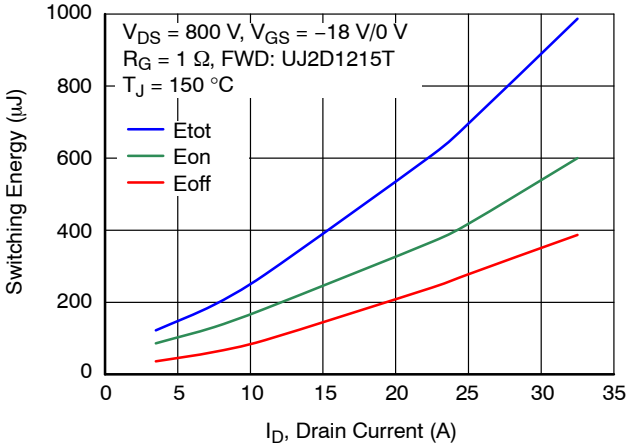


Figure 17. Clamped Inductive Switching Energy vs. Drain Current at T_J = 150 °C

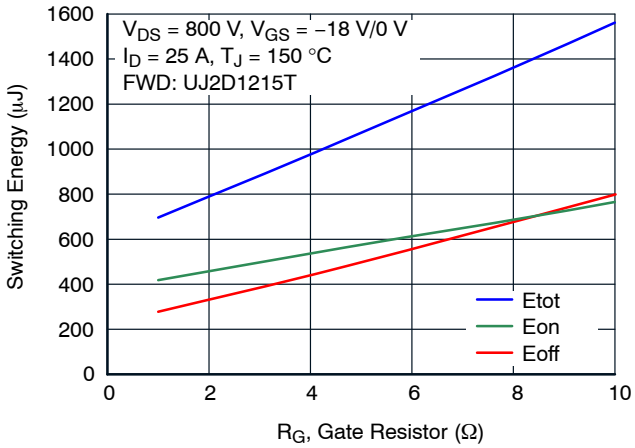


Figure 18. Clamped Inductive Switching Energy vs. Gate Resistor R_G

TYPICAL PERFORMANCE DIAGRAMS (continued)

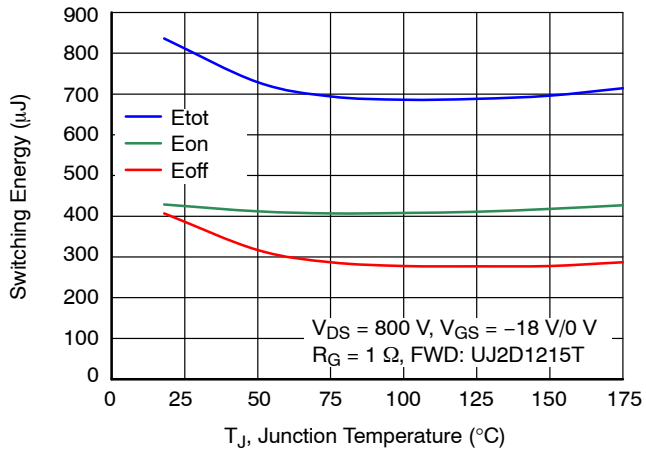


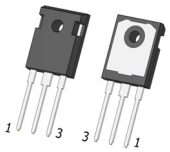
Figure 19. Clamped Inductive Switching Energy vs. Junction Temperature at I_D = 25 A

ORDERING INFORMATION

Part Number	Marking	Package	Shipping
UJ3N120070K3S	UJ3N120070K3S	TO247-3 (Pb-Free, Halogen Free)	600 Units / Tube

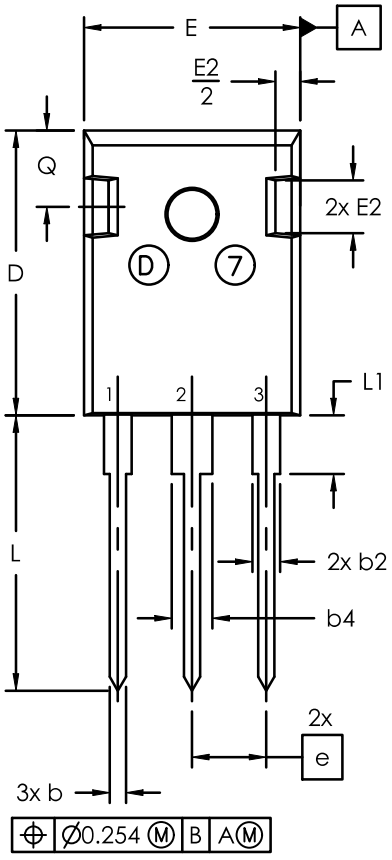
REVISION HISTORY

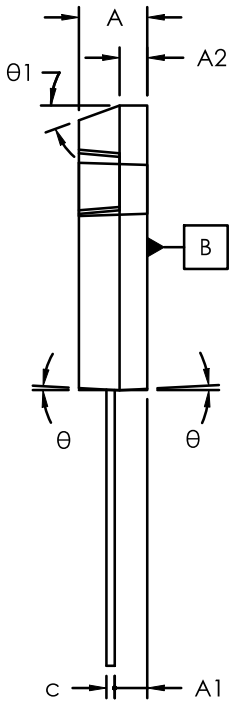
Revision	Description of Changes	Date
C	Acquired the original Qorvo JFET Division Data Sheet and updated the main document title to comply with **onsemi** standards for SiC products.	3/21/2025
3	Converted the Data Sheet to **onsemi** format.	6/3/2025

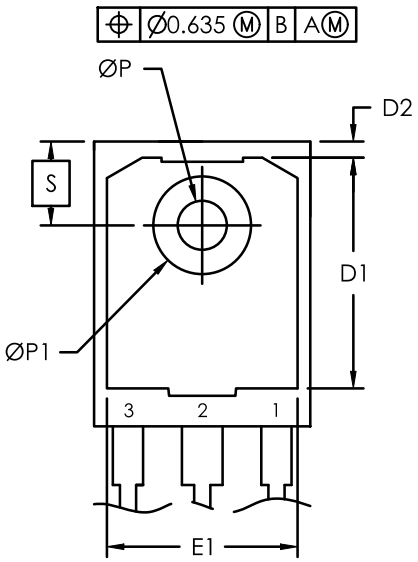


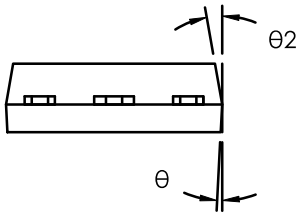
TO247−3 15.90x20.96x5.03, 5.44P
CASE 340AK
ISSUE B

DATE 14 APR 2025









SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
b4	2.59	3.00	3.43
c	0.38	0.60	0.89
D	20.70	20.96	21.46
D1	13.08	—	—
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	5.44 BSC		
E1	13.00	13.30	13.60
E2	3.43	3.89	5.20
L	19.62	20.27	20.32
L1	—	—	4.50
ØP	3.40	3.60	3.80
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.15 BSC		
θ	3°		
θ1	20°		
θ2	10°		

NOTE:
1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.

DOCUMENT NUMBER:	**98AON88794E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**TO247−3 15.90x20.96x5.03, 5.44P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
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