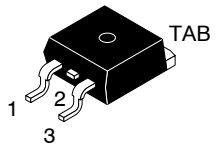
Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, D2PAK-3, 650 V, 27 mohm

UJ3C065030B3



D²PAK-3 (TO-263, 3-LEAD)
CASE 418AJ

Description

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si super-junction devices. Available in the D²PAK-3 package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

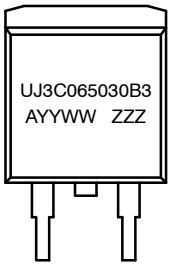
Features

- Typical On-resistance $R_{DS(on),typ}$ of 27 mΩ
- Maximum Operating Temperature of 175 °C
- Excellent Reverse Recovery
- Low Gate Charge
- Low Intrinsic Capacitance
- ESD Protected: HBM Class 2 and CDM Class C3
- This Device is Halogen Free and RoHS Compliant with Exemption 7a, Pb−Free 2LI (on second level interconnection)

Typical Applications

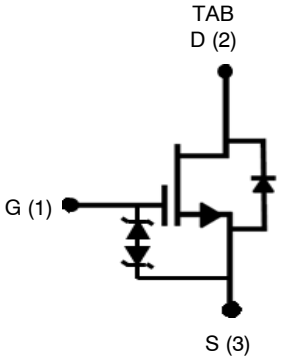
- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating

MARKING DIAGRAM



UJ3C065030B3	= Specific Device Number
A	= Assembly Location
YY	= Year
WW	= Work Week
ZZZ	= Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		650	V
Gate-source Voltage	V_{GS}	DC	−25 to +25	V
Continuous Drain Current (Note 1)	I_D	T_C = 25 °C	65	A
		T_C = 100 °C	47	A
Pulsed Drain Current (Note 2)	I_{DM}	T_C = 25 °C	230	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	L = 15 mH, I_{AS} = 4 A	120	mJ
Power Dissipation	P_{tot}	T_C = 25 °C	242	W
Maximum Junction Temperature	$T_{J,max}$		175	°C
Operating and Storage Temperature	T_J, T_{STG}		−55 to 175	°C
Reflow Soldering Temperature	T_{solder}	Reflow MSL1	245	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by $T_{J,max}$
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25 °C

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		–	0.48	0.62	°C/W

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC							
Drain-source Breakdown Voltage	BV_{DS}	V_{GS} = 0 V, I_D = 1 mA		650	–	–	V
Total Drain Leakage Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V, T_J = 25 °C		–	6	150	μA
		V_{DS} = 650 V, V_{GS} = 0 V, T_J = 175°C		–	30	–	
Total Gate Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = −20 V / +20 V		–	6	±20	μA
Drain-source On-resistance	$R_{DS(on)}$	V_{GS} = 12 V, I_D = 50 A	T_J = 25 °C	–	27	35	mΩ
			T_J = 125 °C	–	35	–	
			T_J = 175 °C	–	43	–	
Gate Threshold Voltage	$V_{G(th)}$	V_{DS} = 5 V, I_D = 10 mA		4	5	6	V
Gate Resistance	R_G	f = 1 MHz, open drain		–	4.5	–	Ω
TYPICAL PERFORMANCE – REVERSE DIODE							
Diode Continuous Forward Current (Note 4)	I_S	T_C = 25 °C		–	–	65	A
Diode Pulse Current (Note 5)	$I_{S,pulse}$	T_C = 25 °C		–	–	230	A
Forward Voltage	V_{FSD}	V_{GS} = 0 V, I_S = 20 A, T_J = 25 °C		–	1.3	1.4	V
		V_{GS} = 0 V, I_S = 20 A, T_J = 175 °C		–	1.35	–	
Reverse Recovery Charge	Q_{rr}	V_{DS} = 400 V, I_S = 50 A, V_{GS} = 0 V, R_{G_EXT} = 20 Ω, di/dt = 1550 A/μs, T_J = 150 °C		–	400	–	nC
Reverse Recovery Time	t_{rr}			–	33	–	ns

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 100 V, V_{GS} = 0 V, f = 100 kHz	–	1500	–	pF
Output Capacitance	C_{oss}		–	320	–	
Reverse Transfer Capacitance	C_{rss}		–	2.3	–	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	230	–	pF
Effective Output Capacitance, Time Related	$C_{oss(tr)}$		–	520	–	pF
C_{oss} Stored Energy	E_{oss}	V_{DS} = 400 V, V_{GS} = 0 V	–	18.5	–	μJ
Total Gate Charge	Q_G	V_{DS} = 400 V, I_D = 40 A, V_{GS} = −5 V to 15 V	–	51	–	nC
Gate-drain Charge	Q_{GD}		–	11	–	
Gate-source Charge	Q_{GS}		–	19	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 400 V, I_D = 40 A, Gate Driver = −5 V to +15 V, Turn-on $R_{G,EXT}$ = 1 Ω, Turn-off $R_{G,EXT}$ = 20 Ω, Inductive Load, FWD: UJ3D065030TS, T_J = 150 °C	–	32	–	ns
Rise Time	t_r		–	19	–	
Turn-off Delay Time	$t_{d(off)}$		–	58	–	
Fall Time	t_f		–	15	–	
Turn-on Energy	E_{ON}		–	341	–	μJ
Turn-off Energy	E_{OFF}		–	180	–	
Total Switching Energy	E_{TOTAL}		–	521	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Limited by $T_{J,max}$.
5. Pulse width t_p limited by $T_{J,max}$.

TYPICAL PERFORMANCE DIAGRAMS

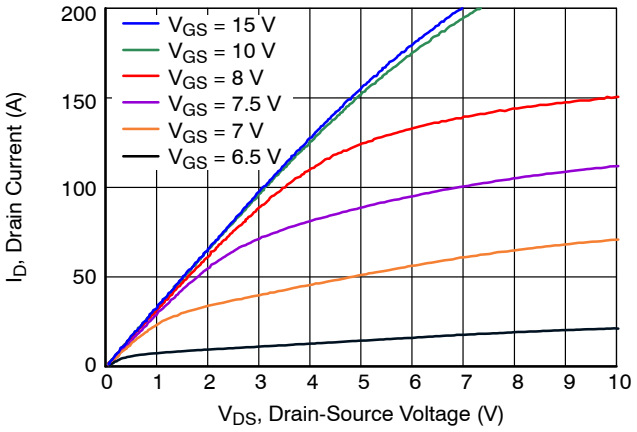


Figure 1. Typical Output Characteristics at T_J = −55 °C, t_p < 250 μs

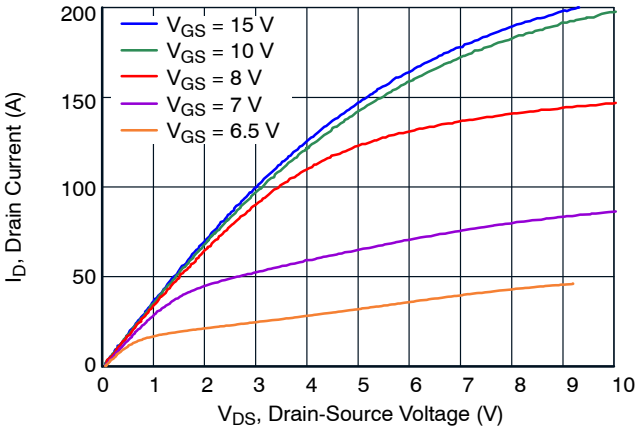


Figure 2. Typical Output Characteristics at T_J = 25 °C, t_p < 250 μs

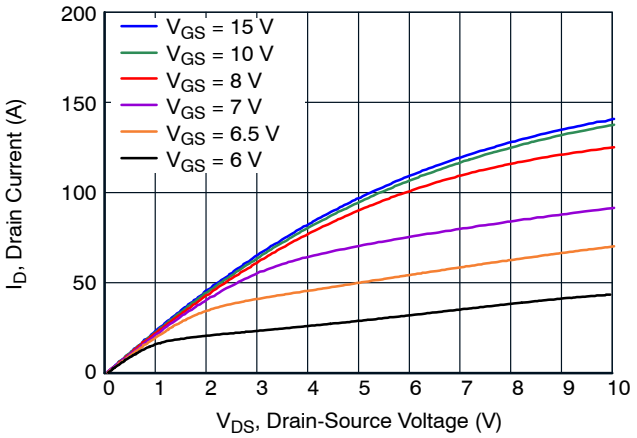


Figure 3. Typical Output Characteristics at T_J = 175 °C, t_p < 250 μs

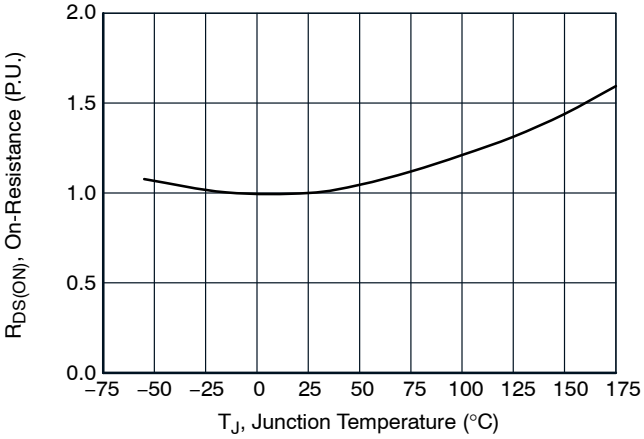


Figure 4. Normalized On-Resistance vs. Temperature at V_{GS} = 12 V and I_D = 50 A

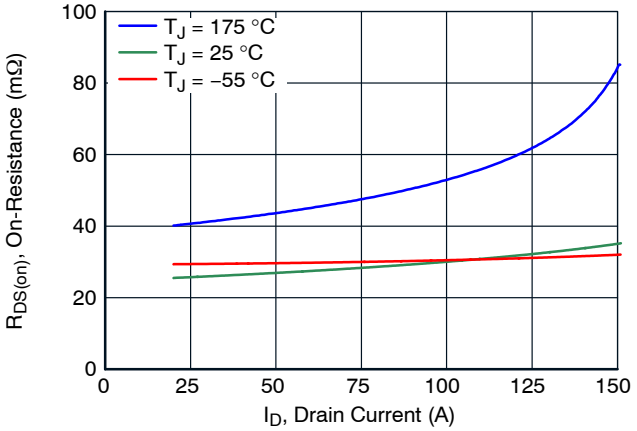


Figure 5. Typical Drain-Source On-Resistances at V_{GS} = 12 V

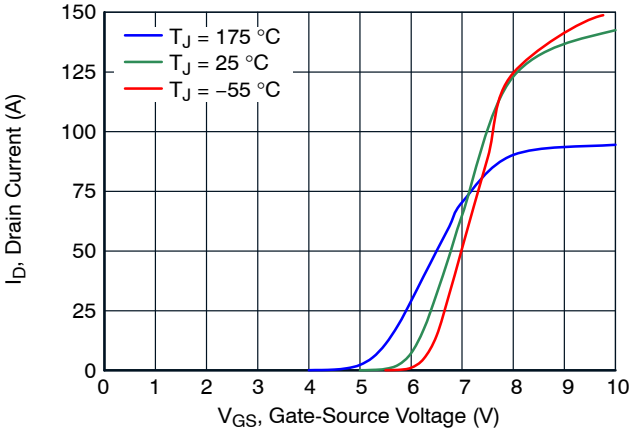


Figure 6. Typical Transfer Characteristics at V_{DS} = 5 V

TYPICAL PERFORMANCE DIAGRAMS (continued)

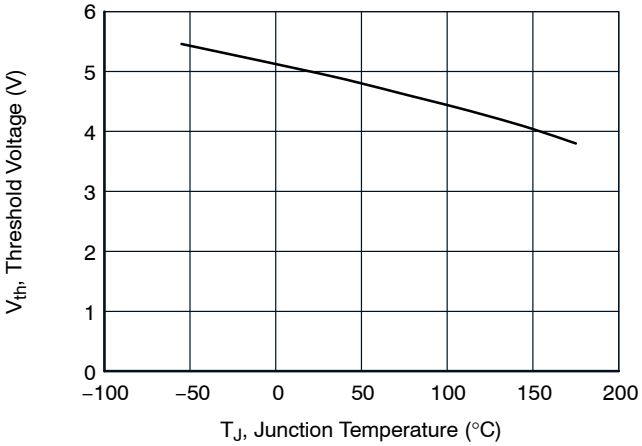


Figure 7. Threshold Voltage vs. Junction Temperature at V_{DS} = 5 V and I_D = 10 mA

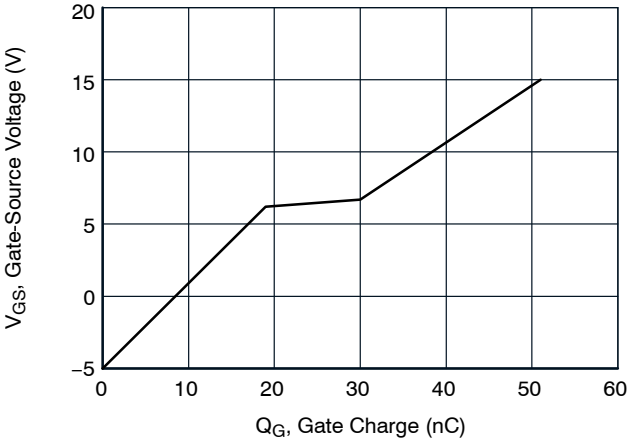


Figure 8. Typical Gate Charge at V_{DS} = 400 V and I_D = 40 A

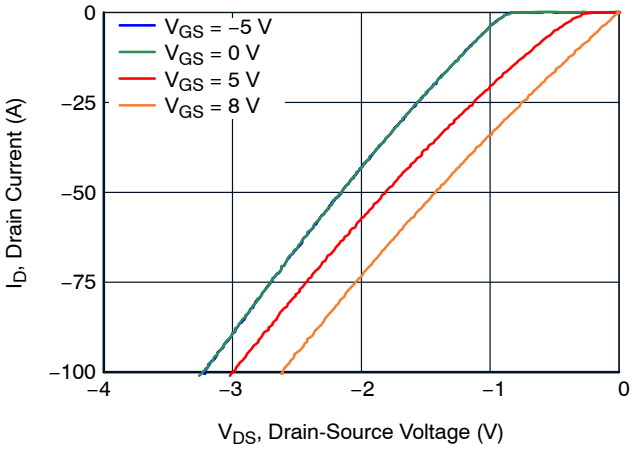


Figure 9. 3rd Quadrant Characteristics at T_J = −55 °C

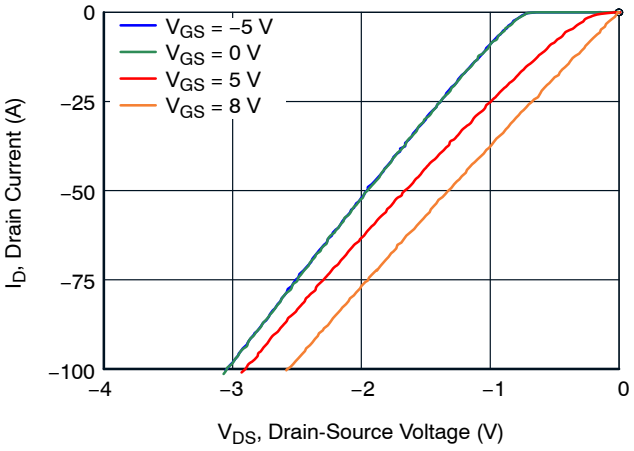


Figure 10. 3rd Quadrant Characteristics at T_J = 25 °C

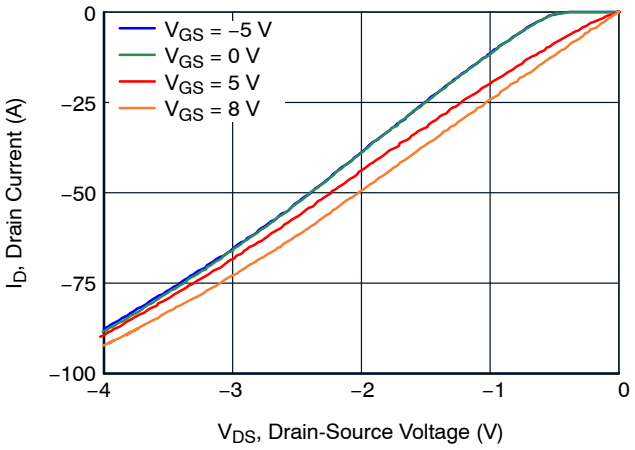


Figure 11. 3rd Quadrant Characteristics at T_J = 175 °C

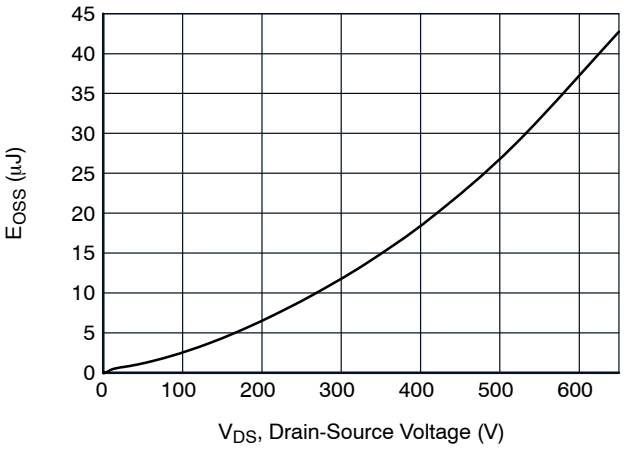


Figure 12. Typical Stored Energy in C_{OSS} at V_{GS} = 0 V

TYPICAL PERFORMANCE DIAGRAMS (continued)

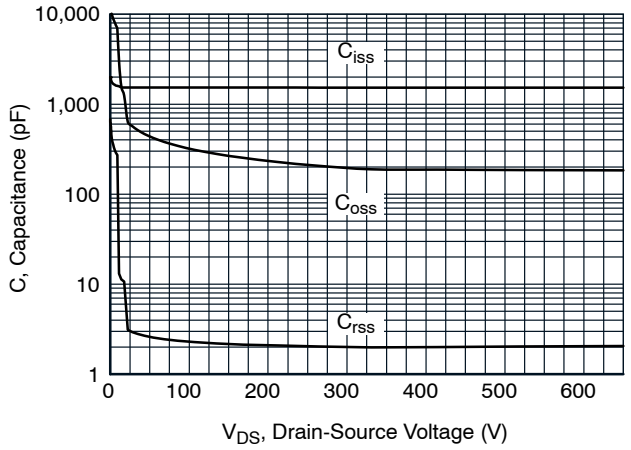


Figure 13. Typical Capacitances at f = 100 kHz and V_{GS} = 0 V

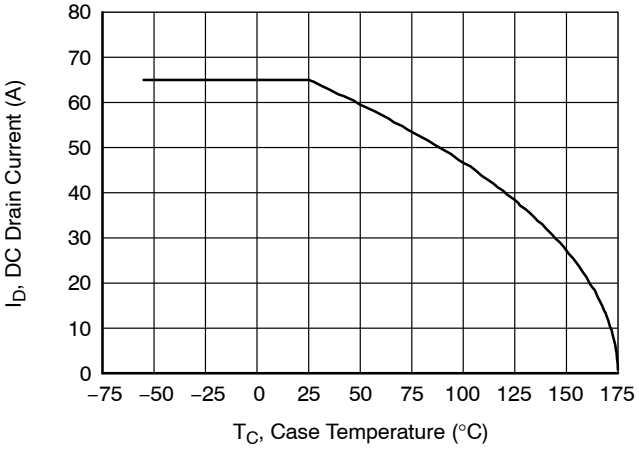


Figure 14. DC Drain Current Derating

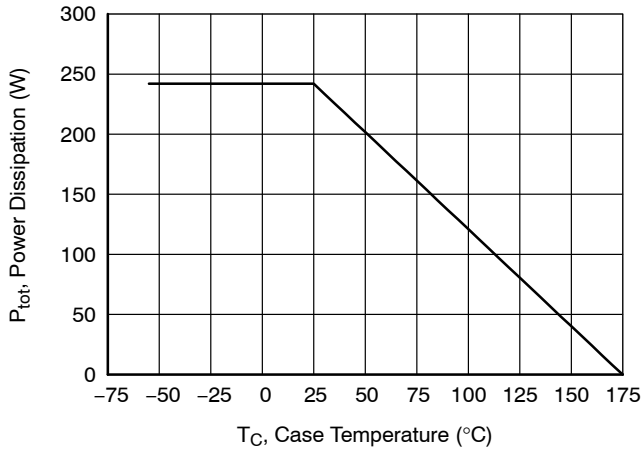


Figure 15. Total Power Dissipation

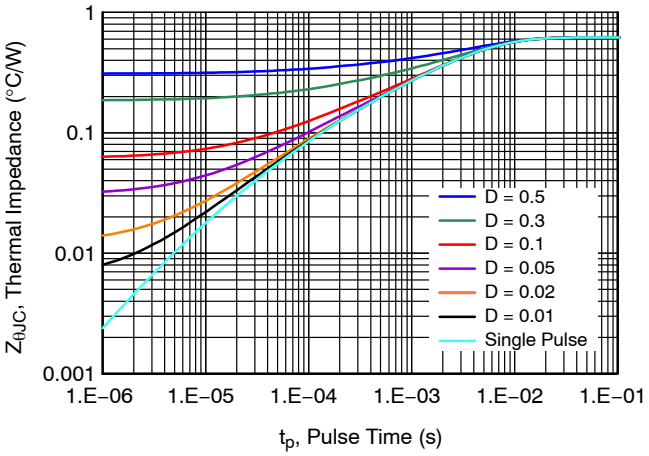


Figure 16. Maximum Transient Thermal Impedance

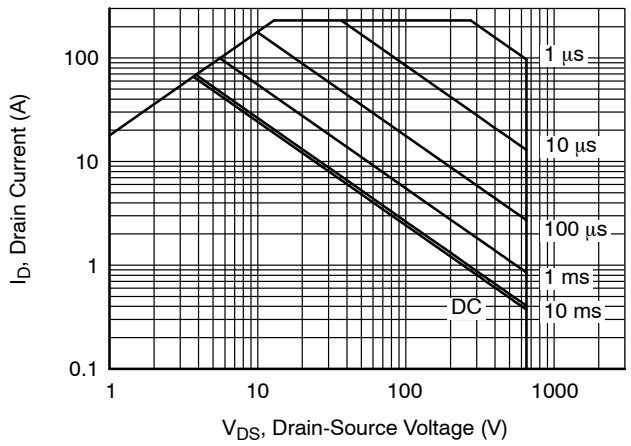


Figure 17. Safe Operation Area at T_C = 25 °C, D = 0, Parameter t_p

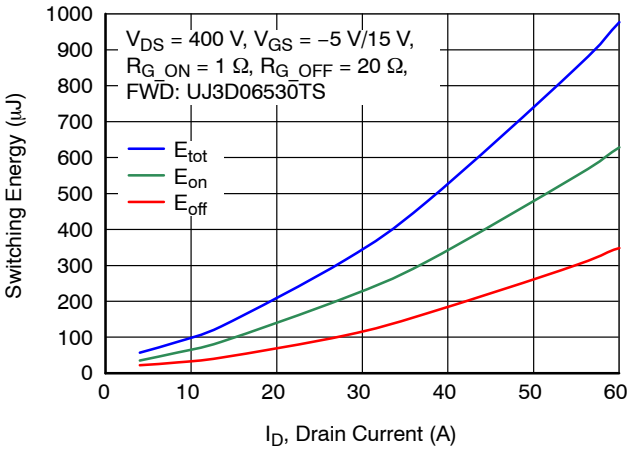


Figure 18. Clamped Inductive Switching Energy vs. Drain Current at T_J = 150 °C

TYPICAL PERFORMANCE DIAGRAMS (continued)

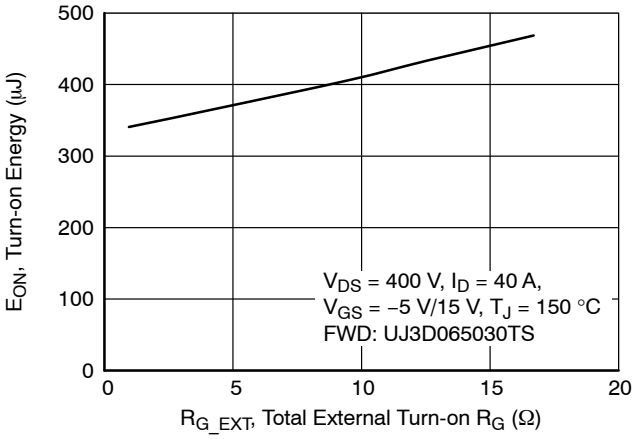


Figure 19. Clamped Inductive Switching Turn-on Energy vs. R_{G,EXT_ON}

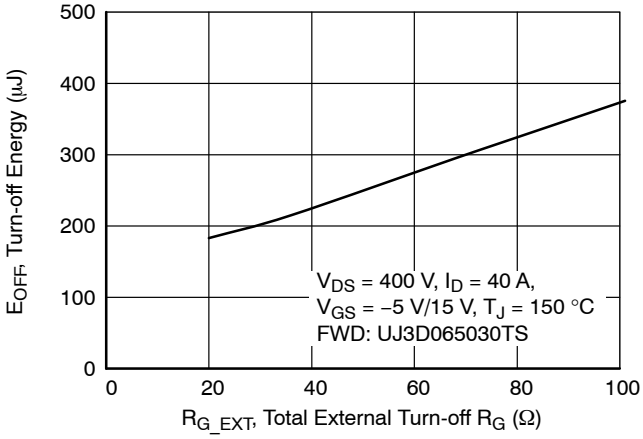


Figure 20. Clamped Inductive Switching Turn-on Energy vs. R_{G,EXT_OFF}

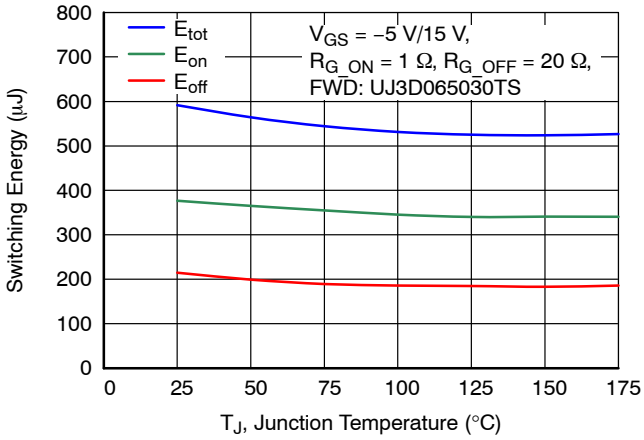


Figure 21. Clamped Inductive Switching Energy vs. Junction Temperature at V_{DS} = 400 V and I_D = 40 A

APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.onsemi.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the **onsemi** website at www.onsemi.com.

ORDERING INFORMATION

Part Number	Marking	Package	Shipping†
UJ3C065030B3	UJ3C065030B3	D^2PAK–3 (TO–263, 3–LEAD) (Halogen Free)	800 / Tape and Reel

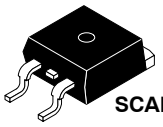
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

REVISION HISTORY

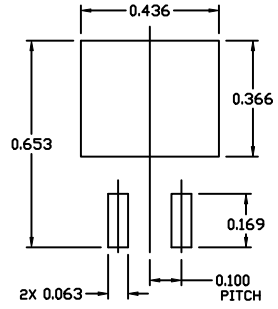
Revision	Description of Changes	Date
D	Acquired the original Qorvo JFET Division Data Sheet and updated the main document title to comply with **onsemi** standards for SiC products.	1/15/2025
4	Converted the Data Sheet to **onsemi** format.	5/23/2025

D²PAK–3 (TO–263, 3–LEAD)
CASE 418AJ
ISSUE F

DATE 11 MAR 2021



SCALE 1:1



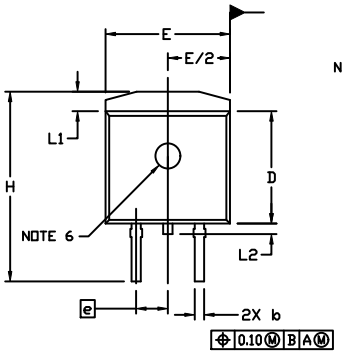
RECOMMENDED
MOUNTING FOOTPRINT

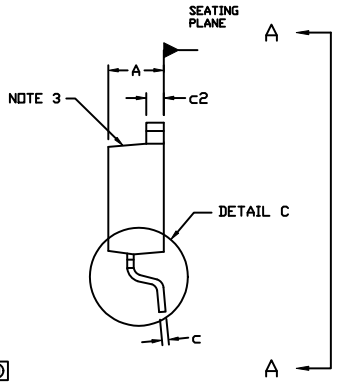
* For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

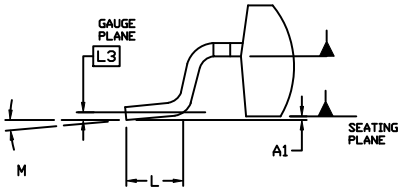
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② … OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

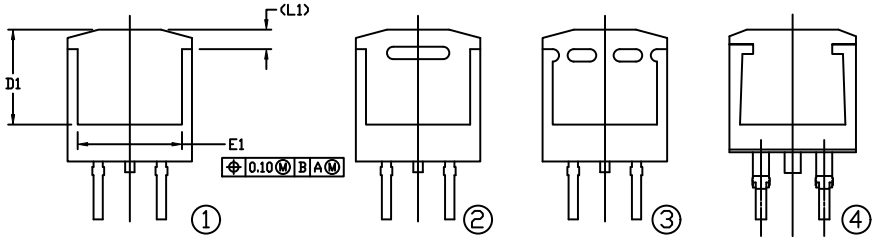
	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°







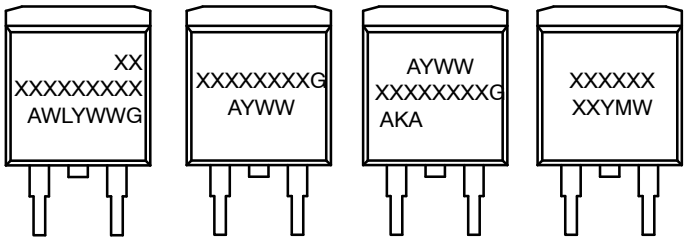
DETAIL C
TIP LEADFORM
ROTATED 90° CW



VIEW A–A

VIEW A–A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC **Standard** **Rectifier** **SSG**

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb–Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON56370E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**D²PAK–3 (TO–263, 3–LEAD)**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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