

Silicon Carbide (SiC) Combo JFET – EliteSiC, Power N-Channel, TO247-4, 1200 V, 8.8 mohm

UG3SC120009K4S

Description

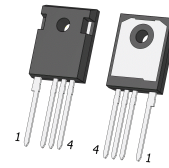
onsemi's UG3SC120009K4S "Combo-FET" integrates both a 1200 V SiC JFET and a Low Voltage Si MOSFET into a single TO247-4 package. This innovative approach allows users to create circuitry that would enable a normally-off switch while leveraging the benefits of a normally-on SiC JFET. These benefits include ultra-low on-resistance ($R_{DS(on)}$) to minimize conduction losses and the exceptional robustness characteristic of a simplified JFET device structure, making it capable of handling the high-energy switching required in circuit protection applications. For switch-mode power conversion application, this device provides separate access to the JFET and MOSFET gates for improved speed control and ease of paralleling multiple devices.

Features

- Single Digit $R_{DS(on)}$
- Normally-off Capability
- Improved Speed Control
- Improved Parallel Device Operation (3+ FETs)
- Operating Temperature: 175 °C (Max)
- High Pulse Current Capability
- Excellent Device Robustness
- Silver-sintered Die Attach for Excellent Thermal Resistance
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

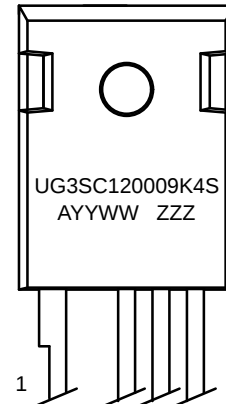
Typical Applications

- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control
- High Power Switch Mode Converters (>25 kW)



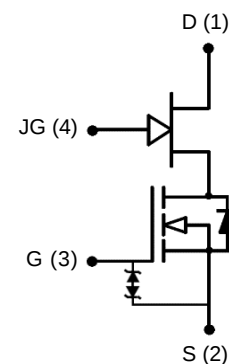
TO247-4
CASE 340AN

MARKING DIAGRAM



UG3SC120009K4S = Specific Device Code
A = Assembly Location
YY = Year
WW = Work Week
ZZZ = Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

UG3SC120009K4S

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		1200	V
JFET Gate (JG) to Source Voltage	V_{JGS}	DC	-30 to +3	V
		AC (Note 1)	-30 to +30	V
MOSFET Gate (G) to Source Voltage	V_{GS}	DC	-20 to +20	V
		AC ($f > 1$ Hz)	-25 to +25	V
Continuous Drain Current (Note 2)	I_D	$T_C < 112$ °C	120	A
Pulsed Drain Current (Note 3)	I_{DM}	$T_C = 25$ °C	550	A
Single Pulsed Avalanche Energy (Note 4)	E_{AS}	$L = 15$ mH, $I_{AS} = 8.6$ A	555	mJ
Power Dissipation	P_{tot}	$T_C = 25$ °C	789	W
Maximum Junction Temperature	$T_{J,max}$		175	°C
Operating and Storage Temperature	T_J, T_{STG}		-55 to 175	°C
Max. Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	T_L		250	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. +30 V ac rating applies for turn-on pulses <200 ns applied with external $R_G > 1$ Ω .
2. Limited by bondwires
3. Pulse width t_p limited by $T_{J,max}$
4. Starting $T_J = 25$ °C

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		-	0.15	0.19	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = +25$ °C and $V_{JGS} = 0$ V unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
-----------	--------	-----------------	-----	-----	-----	------

TYPICAL PERFORMANCE – STATIC

Drain-source Breakdown Voltage	BV_{DS}	$I_D = 1$ mA, $V_{GS} = 0$ V	1200	-	-	V
Total Drain Leakage Current	I_{DSS}	$V_{DS} = 1200$ V, $T_J = 25$ °C, $V_{GS} = 0$ V	-	6	600	μ A
		$V_{DS} = 1200$ V, $T_J = 175$ °C, $V_{GS} = 0$ V	-	65	-	
Total JFET Gate Leakage Current	I_{JGSS}	$V_{JGS} = -20$ V, $V_{GS} = 12$ V	-	15	300	μ A
Total MOSFET Gate Leakage Current	I_{GSS}	$V_{GS} = -20$ V / +20 V	-	5	20	μ A
Drain-source On-resistance	$R_{DS(on)}$	$V_{GS} = 12$ V, $I_D = 100$ A	$V_{JGS} = 2$ V, $T_J = 25$ °C	-	7.6	m Ω
			$T_J = 25$ °C	-	8.8	
			$T_J = 125$ °C	-	13.7	
			$T_J = 175$ °C	-	18.5	
JFET Gate Threshold Voltage	$V_{JG(th)}$	$V_{DS} = 5$ V, $V_{GS} = 12$ V, $I_D = 320$ mA	-9.3	-7	-4.7	V
MOSFET Gate Threshold Voltage	$V_{G(th)}$	$V_{DS} = 5$ V, $V_{JGS} = 0$ V, $I_D = 10$ mA	4	4.7	6	V
JFET Gate Resistance	R_{JG}	$f = 1$ MHz, open drain	-	0.54	-	Ω
MOSFET Gate Resistance	R_G	$f = 1$ MHz, open drain	-	3.5	6	Ω



UG3SC120009K4S

ELECTRICAL CHARACTERISTICS ($T_J = +25\text{ }^{\circ}\text{C}$ and $V_{JGS} = 0\text{ V}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
-----------	--------	-----------------	-----	-----	-----	------

TYPICAL PERFORMANCE – REVERSE DIODE

Diode Continuous Forward Current (Note 5)	I_S	$T_C < 112\text{ }^{\circ}\text{C}$	–	–	120	A
Diode Pulse Current (Note 6)	$I_{S,pulse}$	$T_C = 25\text{ }^{\circ}\text{C}$	–	–	550	A
Forward Voltage	V_{FSD}	$V_{GS} = 0\text{ V}, I_S = 100\text{ A}, T_J = 25\text{ }^{\circ}\text{C}$	–	1.65	2	V
		$V_{GS} = 0\text{ V}, I_S = 100\text{ A}, T_J = 175\text{ }^{\circ}\text{C}$	–	2.4	–	
Reverse Recovery Charge	Q_{rr}	$V_{DS} = 800\text{ V}, I_S = 100\text{ A},$ $V_{GS} = V_{JGS} = 0\text{ V}, R_{JG} = 0.7\text{ }\Omega,$ $di/dt = 1200\text{ A}/\mu\text{s}, T_J = 25\text{ }^{\circ}\text{C}$	–	785	–	nC
Reverse Recovery Time	t_{rr}		–	119	–	ns
Reverse Recovery Charge	Q_{rr}	$V_{DS} = 800\text{ V}, I_S = 100\text{ A},$ $V_{GS} = V_{JGS} = 0\text{ V}, R_{JG} = 0.7\text{ }\Omega,$ $di/dt = 1200\text{ A}/\mu\text{s}, T_J = 150\text{ }^{\circ}\text{C}$	–	815	–	nC
Reverse Recovery Time	t_{rr}		–	124	–	ns

TYPICAL PERFORMANCE – DYNAMIC WITH MOSFET GATE AS CONTROL TERMINAL AND $V_{JGS} = 0\text{ V}$

MOSFET Input Capacitance	C_{iss}	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V},$ $f = 100\text{ kHz}$	–	8157	–	pF
Output Capacitance	C_{oss}		–	351	–	
Reverse Transfer Capacitance	C_{rss}		–	2	–	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	$V_{DS} = 0\text{ V to } 800\text{ V}, V_{GS} = 0\text{ V}$	–	394	–	pF
Effective Output Capacitance, Time Related	$C_{oss(tr)}$		–	920	–	pF
C_{oss} Stored Energy	E_{oss}	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	–	125	–	μJ
Total Gate Charge	Q_G	$V_{DS} = 800\text{ V}, I_D = 100\text{ A},$ $V_{GS} = 0\text{ V to } 15\text{ V}$	–	196	–	nC
Gate-drain Charge	Q_{GD}		–	41	–	
Gate-source Charge	Q_{GS}		–	41	–	
Turn-on Delay Time	$t_{d(on)}$	Notes 7 and 8 $V_{DS} = 800\text{ V}, I_D = 100\text{ A},$ $V_{GS} = 0\text{ V to } +15\text{ V}, R_{G_ON} = 1\text{ }\Omega,$ $R_{G_OFF} = 2\text{ }\Omega, R_{JG_ON} = 0.7\text{ }\Omega,$ $R_{JG_OFF} = 3.3\text{ }\Omega, \text{Inductive Load},$ FWD: same device with $V_{GS} = 0\text{ V},$ $V_{JGS} = 0\text{ V}, R_G = 2\text{ }\Omega,$ $R_{JG_ON} = 0.7\text{ }\Omega, T_J = 25\text{ }^{\circ}\text{C}$	–	160	–	ns
Rise Time	t_r		–	73	–	
Turn-off Delay Time	$t_{d(off)}$		–	210	–	
Fall Time	t_f		–	59	–	
Turn-on Energy	E_{ON}		–	11.5	–	mJ
Turn-off Energy	E_{OFF}		–	2.5	–	
Total Switching Energy	E_{TOTAL}		–	14	–	
Turn-on Delay Time	$t_{d(on)}$	Notes 7 and 8 $V_{DS} = 800\text{ V}, I_D = 100\text{ A},$ $V_{GS} = 0\text{ V to } +15\text{ V}, R_{G_ON} = 1\text{ }\Omega,$ $R_{G_OFF} = 2\text{ }\Omega, R_{JG_ON} = 0.7\text{ }\Omega,$ $R_{JG_OFF} = 3.3\text{ }\Omega, \text{Inductive Load},$ FWD: same device with $V_{GS} = 0\text{ V},$ $R_G = 2\text{ }\Omega, V_{JGS} = 0\text{ V},$ $R_{JG_ON} = 0.7\text{ }\Omega, T_J = 150\text{ }^{\circ}\text{C}$	–	158	–	ns
Rise Time	t_r		–	79	–	
Turn-off Delay Time	$t_{d(off)}$		–	53	–	
Fall Time	t_f		–	212	–	
Turn-on Energy	E_{ON}		–	12.3	–	mJ
Turn-off Energy	E_{OFF}		–	2.8	–	
Total Switching Energy	E_{TOTAL}		–	15.1	–	

TYPICAL PERFORMANCE – DYNAMIC WITH JFET GATE AS CONTROL TERMINAL AND $V_{GS} = +12\text{ V}$

JFET Input Capacitance	C_{Jiss}	$V_{DS} = 800\text{ V}, V_{JGS} = -20\text{ V},$ $f = 100\text{ kHz}$	–	8110	–	pF
JFET Output Capacitance	C_{Joss}		–	368	–	
JFET Reverse Transfer Capacitance	C_{Jrss}		–	358	–	
JFET Total Gate Charge	Q_{JG}	$V_{DS} = 800\text{ V}, I_D = 100\text{ A},$ $V_{JGS} = -18\text{ V to } 0\text{ V}$	–	830	–	nC
JFET Gate-drain Charge	Q_{JGD}		–	520	–	
JFET Gate-source Charge	Q_{JGS}		–	120	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Limited by bondwires.

6. Pulse width t_p limited by $T_{J,max}$.

7. Measured with the half-bridge mode switching test circuit in Figure 23.

8. Driven with the ClampDRIVE method as described in the section “Recommended Gate Drive Approach: ClampDRIVE Method”.



TYPICAL PERFORMANCE DIAGRAMS – MOSFET GATE AS CONTROL TERMINAL AND $V_{JGS} = 0$ V

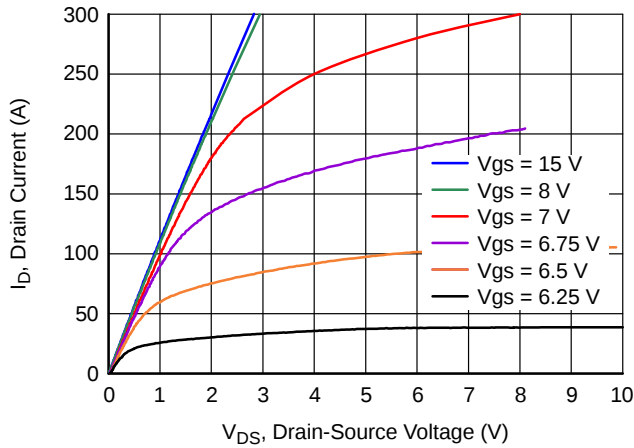


Figure 1. Typical Output Characteristics at $T_J = -55\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

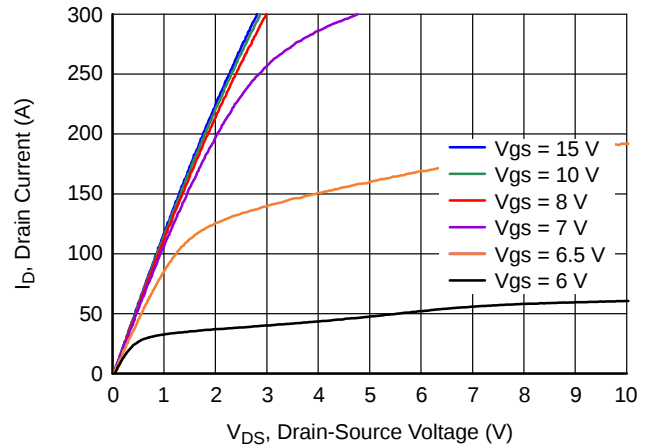


Figure 2. Typical Output Characteristics at $T_J = 25\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

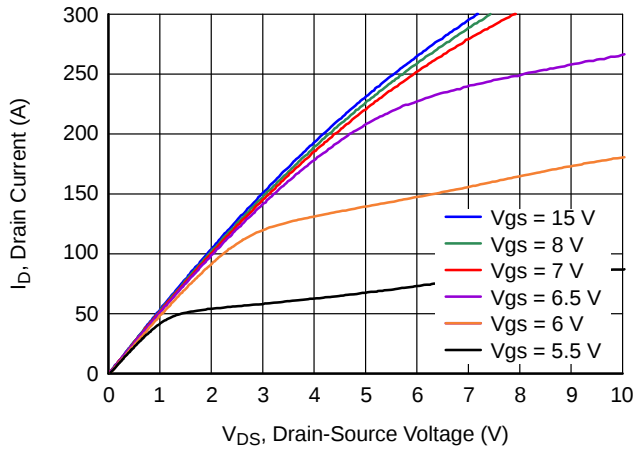


Figure 3. Typical Output Characteristics at $T_J = 175\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

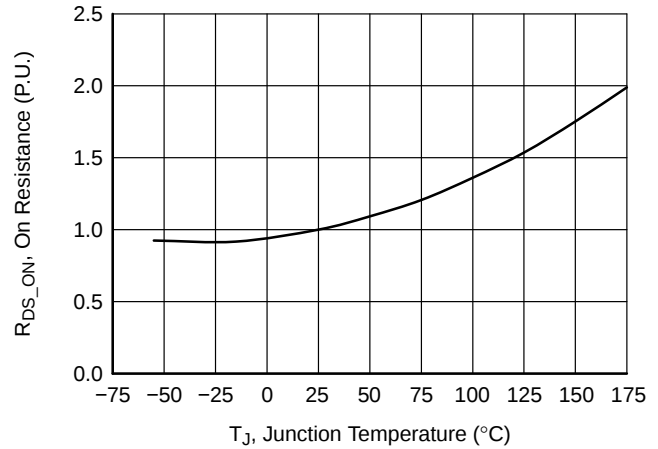


Figure 4. Normalized On-Resistance vs. Temperature at $V_{GS} = 12\text{ V}$ and $I_D = 100\text{ A}$

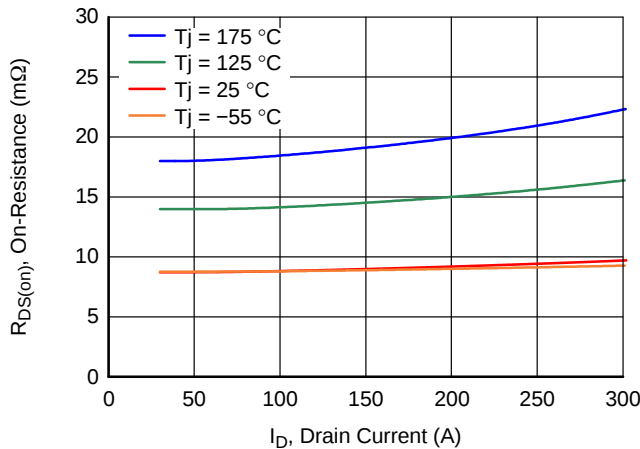


Figure 5. Typical Drain-Source On-Resistances at $V_{GS} = 12\text{ V}$

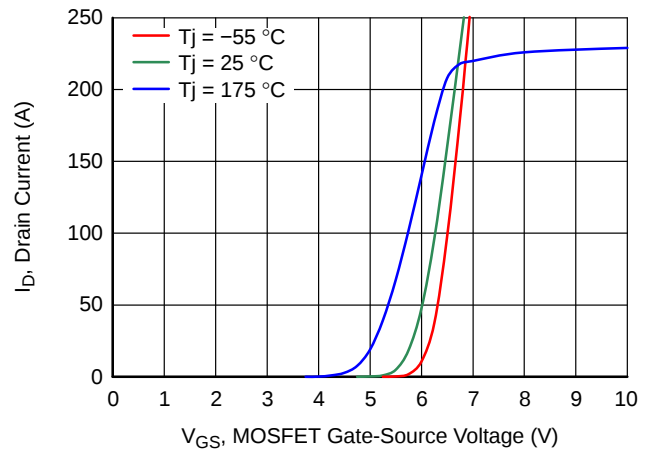


Figure 6. Typical Transfer Characteristics at $V_{DS} = 5\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS – MOSFET GATE AS CONTROL TERMINAL AND $V_{JGS} = 0\text{ V}$
(CONTINUED)

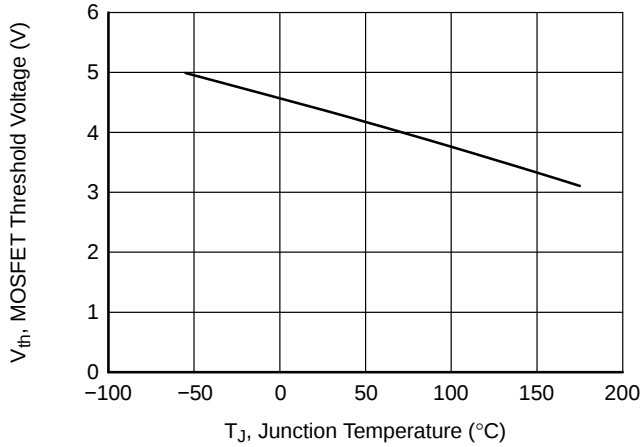


Figure 7. MOSFET Threshold Voltage vs. Junction Temperature at $V_{DS} = 5\text{ V}$ and $I_D = 10\text{ mA}$

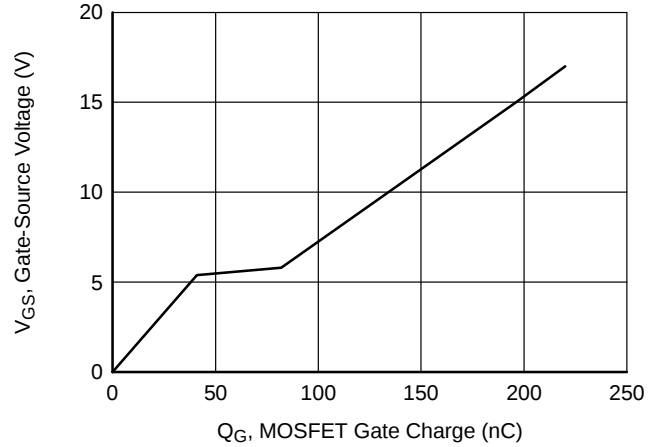


Figure 8. Typical MOSFET Gate Charge at $V_{DS} = 800\text{ V}$ and $I_D = 100\text{ A}$

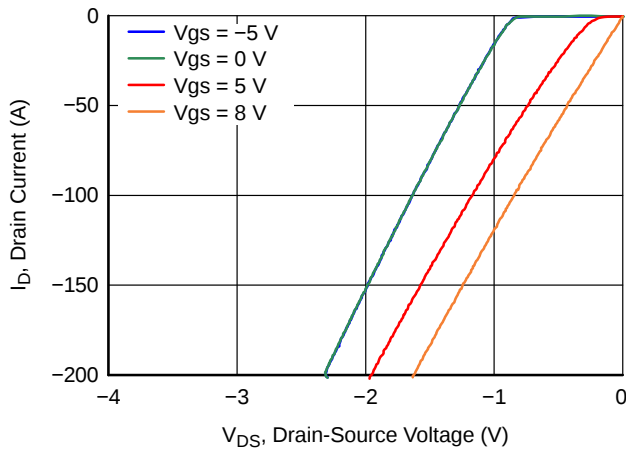


Figure 9. 3rd Quadrant Characteristics at $T_J = -55\text{ °C}$

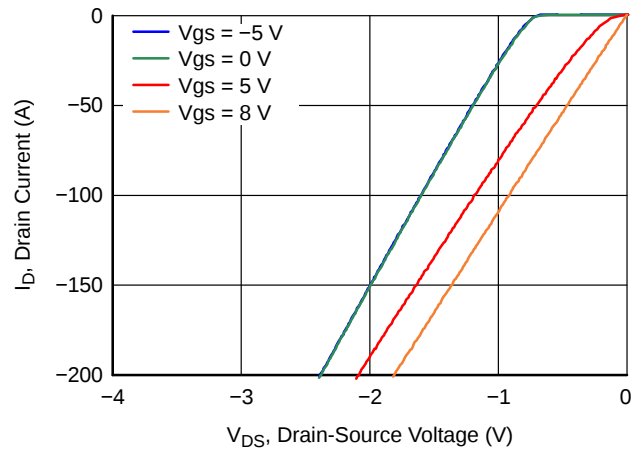


Figure 10. 3rd Quadrant Characteristics at $T_J = 25\text{ °C}$

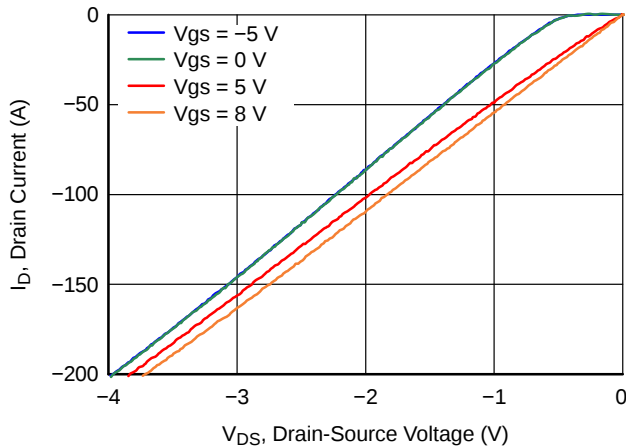


Figure 11. 3rd Quadrant Characteristics at $T_J = 175\text{ °C}$

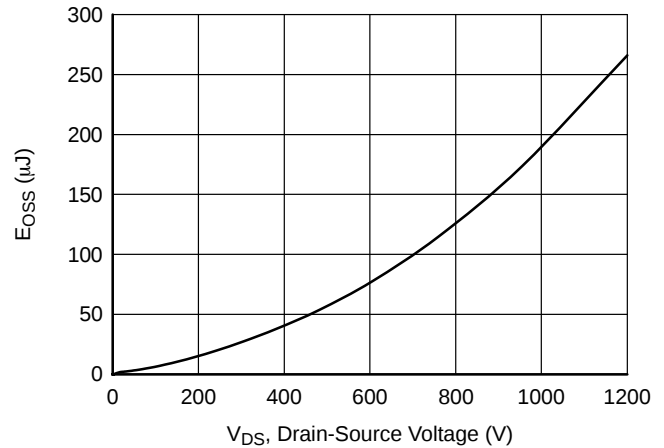


Figure 12. Typical Stored Energy in C_{OSS} at $V_{GS} = 0\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS – MOSFET GATE AS CONTROL TERMINAL AND $V_{JGS} = 0\text{ V}$
(CONTINUED)

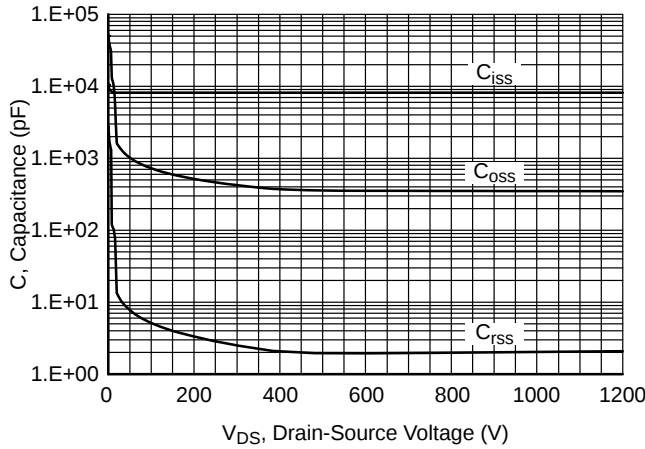


Figure 13. Typical Capacitances at $f = 100\text{ kHz}$ and $V_{GS} = 0\text{ V}$

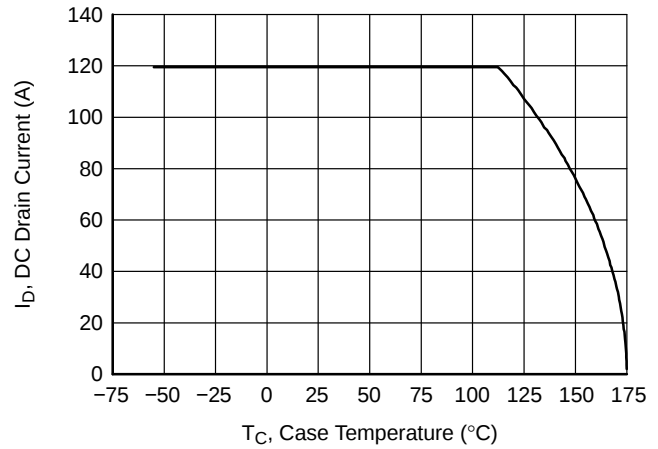


Figure 14. DC Drain Current Derating

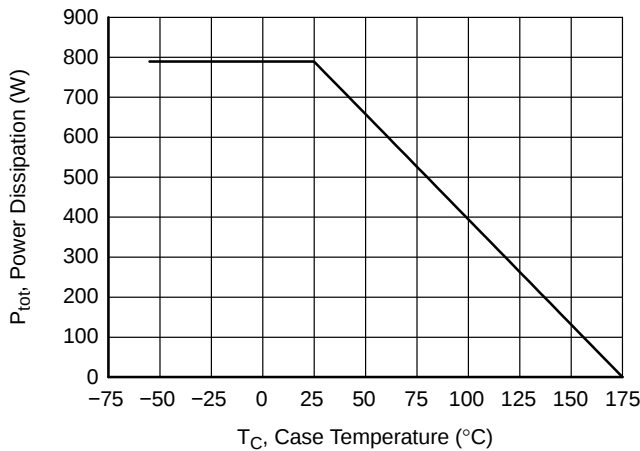


Figure 15. Total Power Dissipation

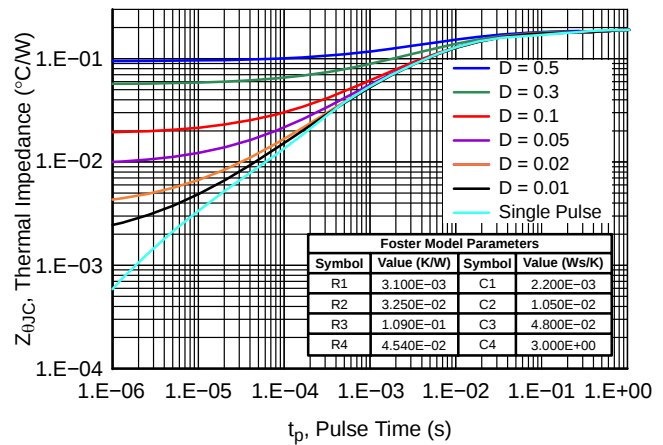


Figure 16. Maximum Transient Thermal Impedance

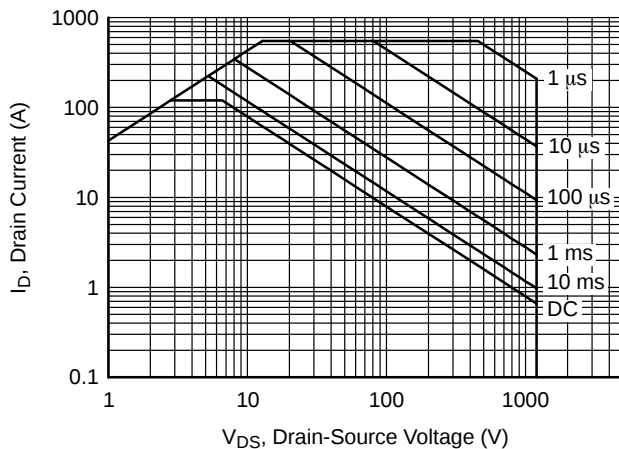


Figure 17. Safe Operation Area at $T_C = 25\text{ °C}$, $D = 0$, Parameter t_p

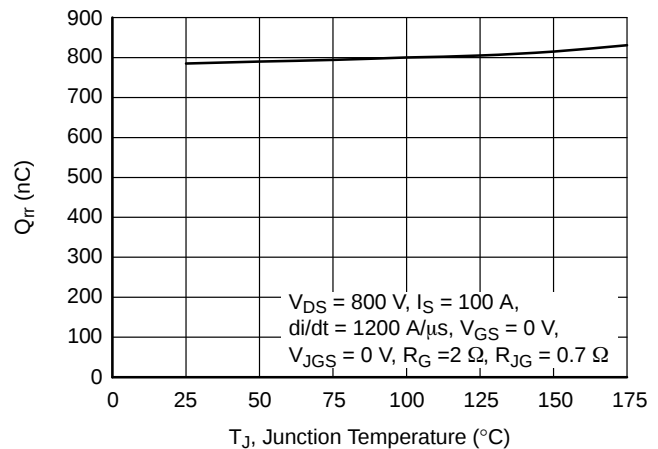


Figure 18. Reverse Recovery Charge Q_{rr} vs. Junction Temperature

TYPICAL PERFORMANCE DIAGRAMS – MOSFET GATE AS CONTROL TERMINAL AND $V_{JGS} = 0$ V
(CONTINUED)

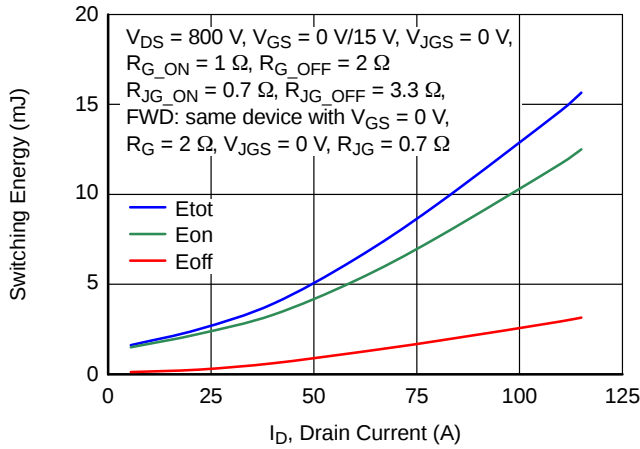


Figure 19. Clamped Inductive Switching Energy vs. Drain Current at $T_J = 25^\circ\text{C}$

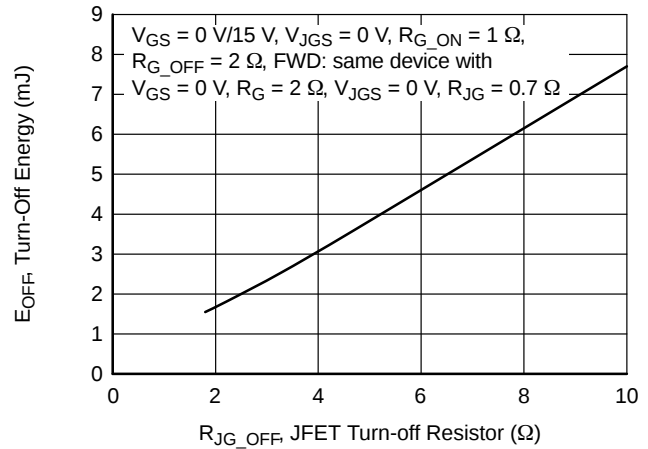


Figure 20. Clamped Inductive Turn-Off Energy vs. JFET Gate Resistor R_{JG_OFF} at $V_{DS} = 800$ V, $I_D = 100$ A, and $T_J = 25^\circ\text{C}$

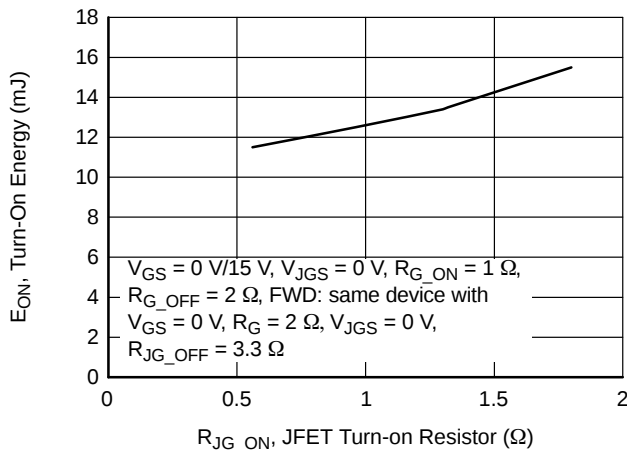


Figure 21. Clamped Inductive Switching Turn-On Energy vs. JFET Gate Resistor R_{JG_ON} at $V_{DS} = 800$ V, $I_D = 100$ A, and $T_J = 25^\circ\text{C}$

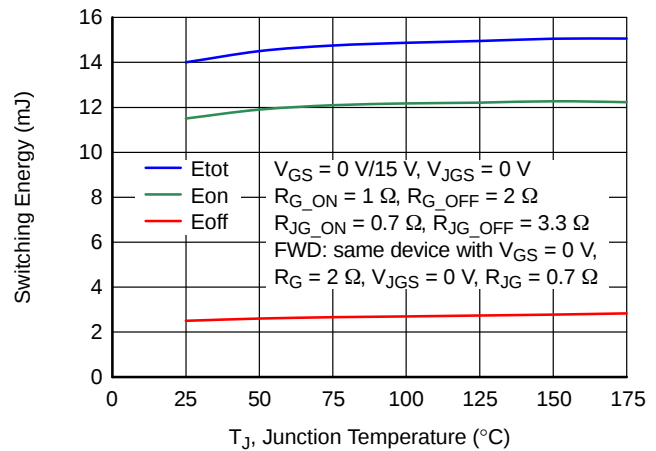


Figure 22. Clamped Inductive Switching Energy vs. Junction Temperature at $V_{DS} = 800$ V and $I_D = 100$ A

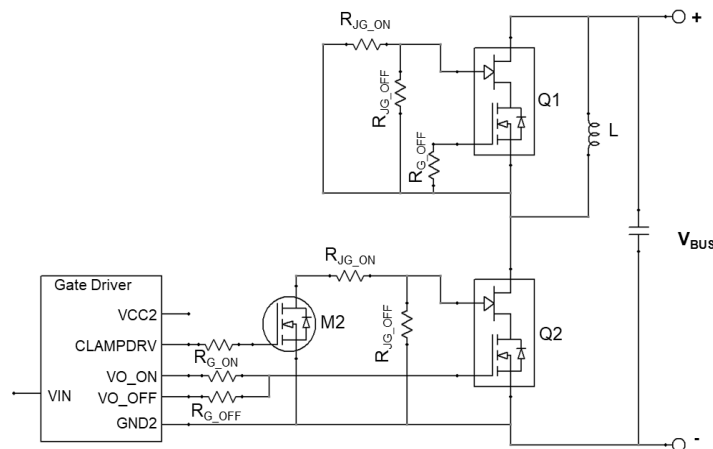


Figure 23. Schematic of the Half-bridge Mode Switching Test Circuit with ClampDRIVE Method

TYPICAL PERFORMANCE DIAGRAMS – JFET GATE AS CONTROL TERMINAL AND $V_{GS} = +12\text{ V}$

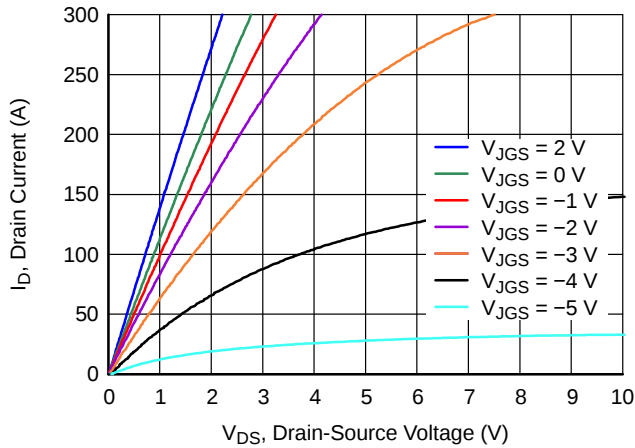


Figure 24. Typical Output Characteristics with JFET Gate as Control at $T_J = -55\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

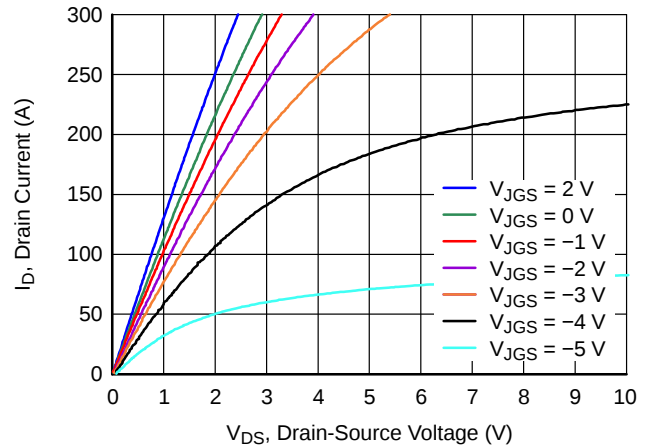


Figure 25. Typical Output Characteristics with JFET Gate as Control at $T_J = 25\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

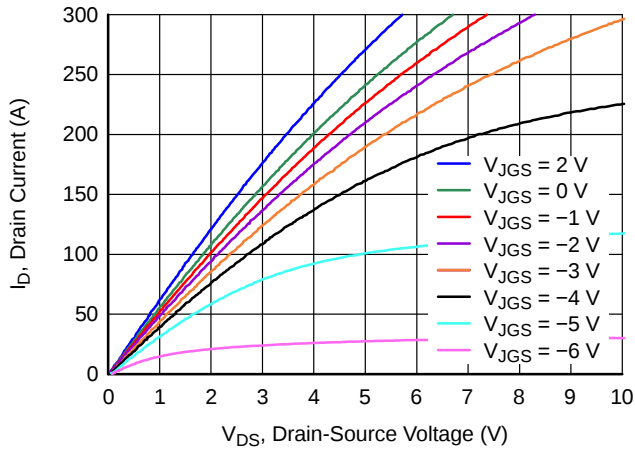


Figure 26. Typical Output Characteristics with JFET Gate as Control at $T_J = 175\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

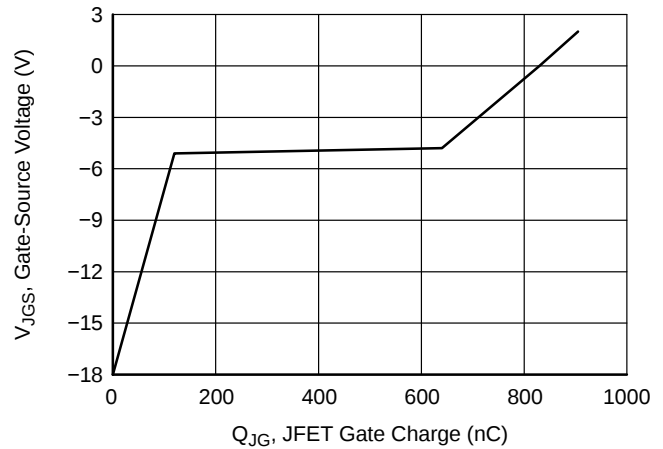


Figure 27. Typical JFET Gate Charge at $V_{DS} = 800\text{ V}$ and $I_D = 100\text{ A}$

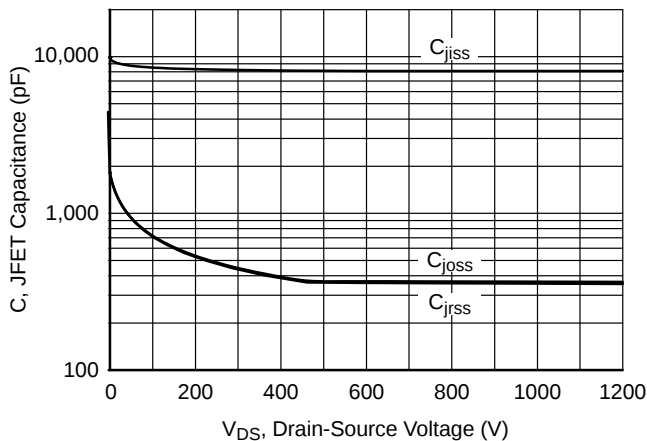


Figure 28. Typical JFET Capacitances at $f = 100\text{ kHz}$ and $V_{GS} = -20\text{ V}$

RECOMMENDED GATE DRIVE APPROACH: CLAMPDRIVE METHOD

Since both JFET gate and MOSFET gate are accessible, more parameters and approaches can be used to control the switching behaviors of the device and make the device suitable for a wide range applications from solid state circuit breakers requiring ultra-high current turn-off capability to motor drives requiring fast switching speed. The recommended gate drive approach is the ClampDRIVE method, with which the desired turn-on speed, turn-off speed and reverse recovery performance can be achieved at the same time. The main idea of this method is to dynamically tune the JFET gate resistor value R_{JG} such that, in the off-state, R_{JG} is small enough not to cause a reverse recovery issue, and during turn-off transient, R_{JG} is set to a higher value for the desired turn-off performance. This method can be easily implemented using a commercial off-the-shelf gate driver with miller clamp pre-driver output, as illustrated in Figure 29. VIN is the gate driver input signal. VO is the gate driver output and CLAMPDRV is the gate driver miller clamp pre-driver output. M2 is the clamp MOSFET used to control the JFET gate resistance. The MOSFET M2 is directly controlled by the CLAMPDRV signal.

In the on-state, CLAMPDRV is low which turns the MOSFET M2 off, thus, the effective JFET gate resistance is R_{JG_OFF} . During the turn-off transient, CLAMPDRV is kept low until the device is fully off. This means the JFET gate resistance is R_{JG_OFF} during the turn-off process, and R_{JG_OFF} can be used to effectively control turn-off speed. After the device is fully off, CLAMPDRV is changed to high level, which turns the MOSFET M2 on.

In the off-state, CLAMPDRV is high and the clamp MOSFET M2 is in on-state. The effective JFET gate resistance is equal to the parallel combination of R_{JG_OFF} and R_{JG_ON} . R_{JG_ON} can be selected small enough to prevent the reverse recovery issue. During the turn-on transient, the JFET gate current may flow from the cascode source through the body diode of the MOSFET M2 and R_{JG_ON} into the JFET gate, so, the turn-on process is also determined by R_{JG_ON} .

In summary, the optimum switching performance of the SiC cascode FETs can be realized with the ClampDRIVE method by selecting proper JFET gate resistors R_{JG_ON} and R_{JG_OFF} .

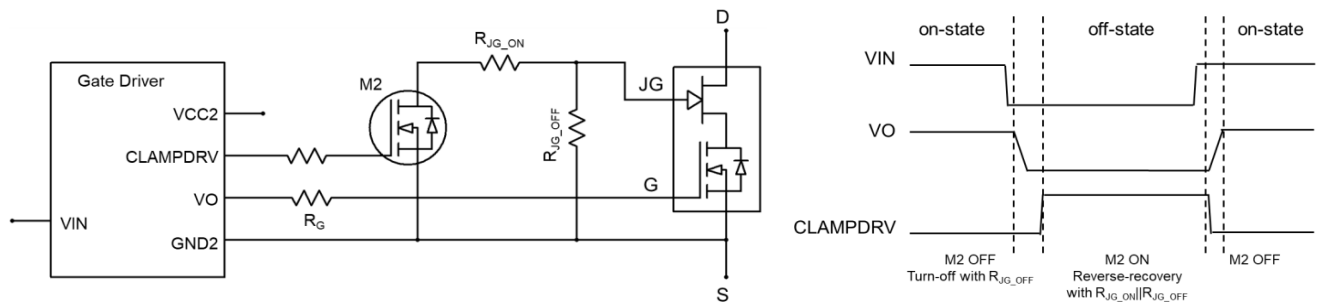


Figure 29. Circuit Schematic and Timing Diagram of the ClampDRIVE Method

ORDERING INFORMATION

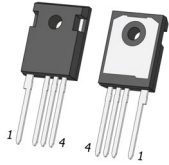
Part Number	Marking	Package	Shipping [†]
UG3SC120009K4S	UG3SC120009K4S	TO247-4 15.90x20.96x5.03, 5.44P (Pb-Free, Halogen Free)	600 / Tube

UG3SC120009K4S

REVISION HISTORY

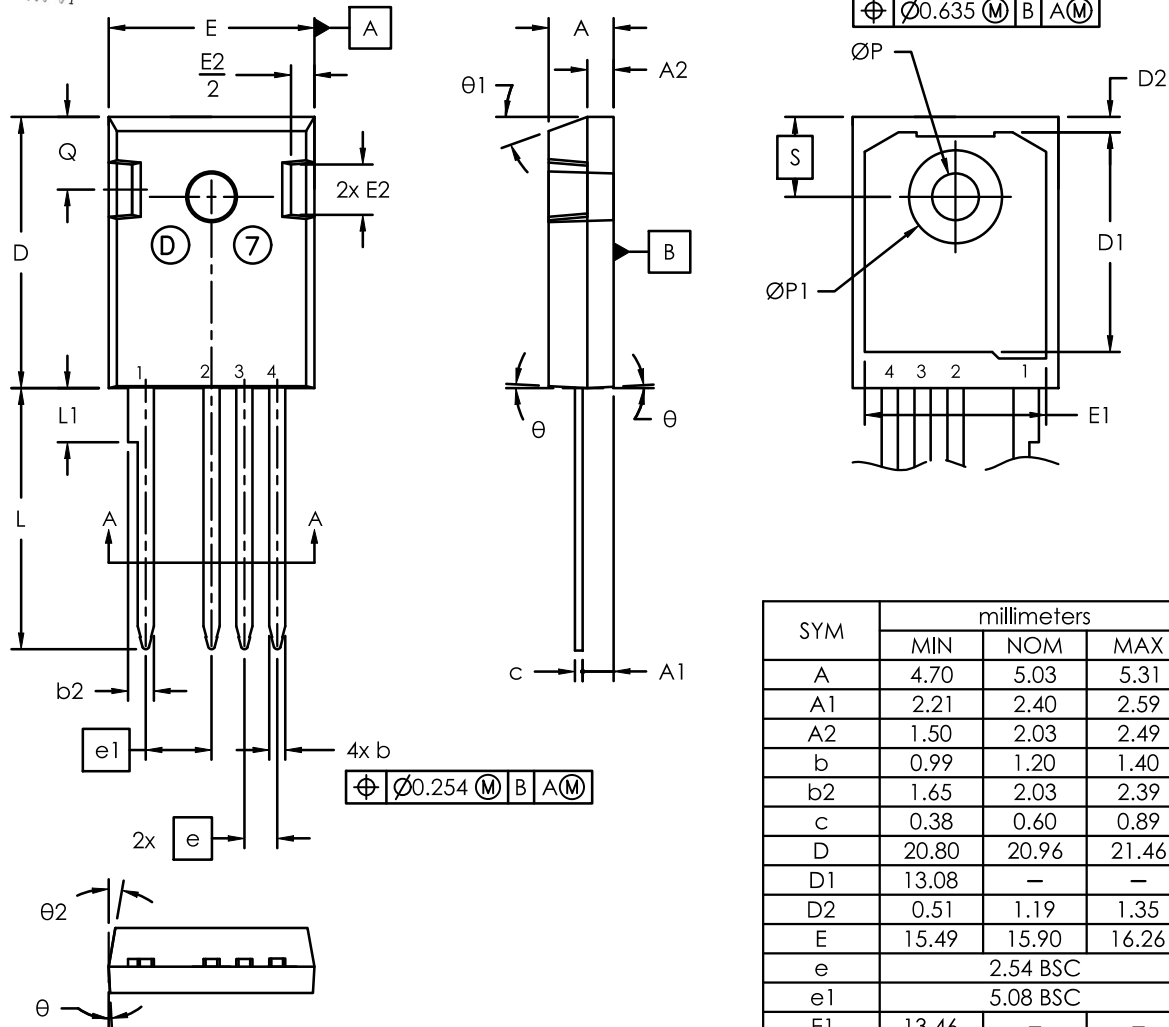
Revision	Description of Changes	Date
C	Acquired the original Qorvo JFET Division Data Sheet and updated the main document title to comply with onsemi standards for SiC products.	1/15/2025
3	Converted the Data Sheet to onsemi format.	6/3/2025





TO247-4 15.90x20.96x5.03, 5.44P
CASE 340AN
ISSUE E

DATE 20 JUN 2025



NOTE:

1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. $\varnothing P$ to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.
5. Through Hole diameter value = End Hole diameter
6. PCB Through Hole pattern as per IPC-2221/IPC-2222

SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
c	0.38	0.60	0.89
D	20.80	20.96	21.46
D1	13.08	—	—
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	2.54 BSC		
e1	5.08 BSC		
E1	13.46	—	—
E2	3.43	3.89	5.20
L	19.81	20.17	20.32
L1	—	—	4.50
$\varnothing P$	3.40	3.60	3.80
$\varnothing P1$	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.17 BSC		
θ	3°		
$\theta 1$	20°		
$\theta 2$	10°		

DOCUMENT NUMBER: 98AON86067F

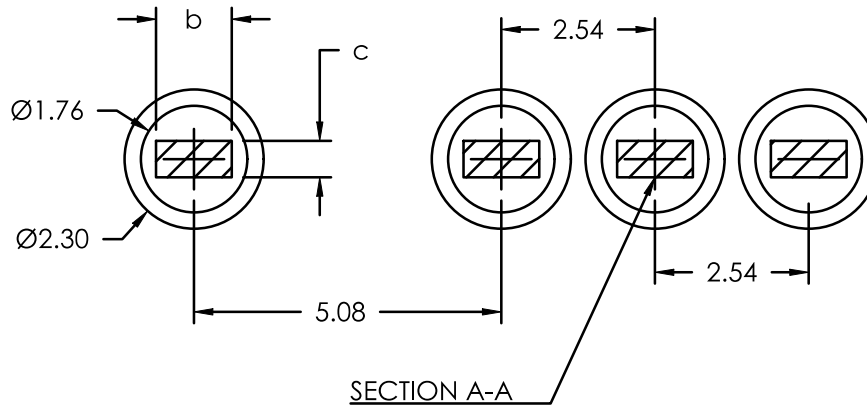
Electronic versions are uncontrolled except when accessed directly from the Document Repository.
Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

DESCRIPTION: TO247-4 15.90x20.96x5.03, 5.44P

PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

RECOMMENDED PCB THROUGH HOLE



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.
END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

DOCUMENT NUMBER:	98AON86067F	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO247-4 15.90x20.96x5.03, 5.44P	PAGE 2 OF 2

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales