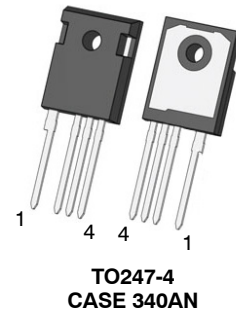


# Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, TO247-4, 1200 V, 23 mohm

## UF4SC120023K4S



TO247-4  
 CASE 340AN

### Description

The UF4SC120023K4S is a 1200 V, 23 mΩ G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-247-4L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

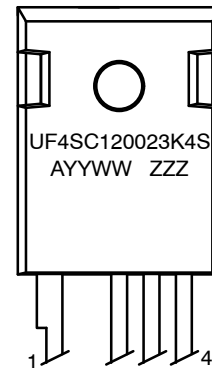
### Features

- On-resistance  $R_{DS(on)}$ : 23 mΩ (typ)
- Operating Temperature: 175 °C (max)
- Excellent Reverse Recovery:  $Q_{rr} = 341$  nC
- Low Body Diode  $V_{FSD}$ : 1.2 V
- Low Gate Charge:  $Q_G = 37.8$  nC
- Threshold Voltage  $V_{G(th)}$ : 4.8 V (typ) Allowing 0 to 15 V Drive
- Low Intrinsic Capacitance
- ESD Protected: HBM Class 2 and CDM Class C3
- TO-247-4L Package for Faster Switching, Clean Gate Waveforms
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

### Typical Applications

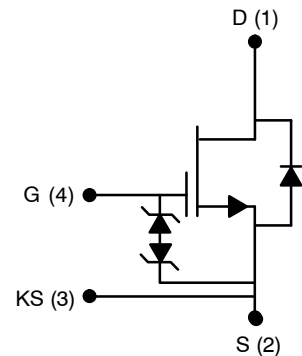
- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating

### MARKING DIAGRAM



UF4SC120023K4S = Specific Device Code  
 A = Assembly Location  
 YY = Year  
 WW = Work Week  
 ZZZ = Lot Code

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

# UF4SC120023K4S

## MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	$V_{DS}$		1200	V
Gate-source Voltage	$V_{GS}$	DC	-20 to +20	V
		AC ( $f > 1$ Hz)	-25 to +25	
Continuous Drain Current (Note 1)	$I_D$	$T_C \leq 95$ °C	53	A
Pulsed Drain Current (Note 2)	$I_{DM}$	$T_C = 25$ °C	204	A
Single Pulsed Avalanche Energy (Note 3)	$E_{AS}$	$L = 15$ mH, $I_{AS} = 4.1$ A	126	mJ
SiC FET dv/dt Ruggedness	dv/dt	$V_{DS} \leq 800$ V	150	V/ns
Power Dissipation	$P_{tot}$	$T_C = 25$ °C	385	W
Maximum Junction Temperature	$T_{J, max}$		175	°C
Operating and Storage Temperature	$T_J, T_{STG}$		-55 to 175	°C
Max. Lead Temperature for Soldering, 1/8" from Case for 5 seconds	$T_L$		250	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Limited by bondwires.
- Pulse width  $t_p$  limited by  $T_{J, max}$ .
- Starting  $T_J = 25$  °C.

## THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		-	0.3	0.39	°C/W

## ELECTRICAL CHARACTERISTICS ( $T_J = +25$ °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### TYPICAL PERFORMANCE – STATIC

Drain-source Breakdown Voltage	$BV_{DS}$	$V_{GS} = 0$ V, $I_D = 1$ mA	1200	-	-	V
Total Drain Leakage Current	$I_{DSS}$	$V_{DS} = 1200$ V, $V_{GS} = 0$ V, $T_J = 25$ °C	-	2	60	$\mu$ A
		$V_{DS} = 1200$ V, $V_{GS} = 0$ V, $T_J = 175$ °C	-	20	-	
Total Gate Leakage Current	$I_{GSS}$	$V_{DS} = 0$ V, $T_J = 25$ °C, $V_{GS} = -20$ V / +20 V	-	6	20	$\mu$ A
Drain-source On-resistance	$R_{DS(on)}$	$V_{GS} = 12$ V, $I_D = 40$ A, $T_J = 25$ °C	-	23	29	m $\Omega$
		$V_{GS} = 12$ V, $I_D = 40$ A, $T_J = 125$ °C	-	42	-	
		$V_{GS} = 12$ V, $I_D = 40$ A, $T_J = 175$ °C	-	57	-	
Gate Threshold Voltage	$V_{G(th)}$	$V_{DS} = 5$ V, $I_D = 10$ mA	4	4.8	6	V
Gate Resistance	$R_G$	$f = 1$ MHz, open drain	-	4.5	-	$\Omega$

### TYPICAL PERFORMANCE – REVERSE DIODE

Diode Continuous Forward Current (Note 1)	$I_S$	$T_C \leq 95$ °C	-	-	53	A
Diode Pulse Current (Note 2)	$I_{S, pulse}$	$T_C = 25$ °C	-	-	204	A
Forward Voltage	$V_{FSD}$	$V_{GS} = 0$ V, $I_S = 20$ A, $T_J = 25$ °C	-	1.2	1.35	V
		$V_{GS} = 0$ V, $I_S = 20$ A, $T_J = 175$ °C	-	1.65	-	
Reverse Recovery Charge	$Q_{rr}$	$V_{DS} = 800$ V, $I_S = 40$ A, $V_{GS} = 0$ V, $R_G = 30$ $\Omega$ , $di/dt = 2100$ A/ $\mu$ s, $T_J = 25$ °C	-	341	-	nC
Reverse Recovery Time	$t_{rr}$		-	27	-	ns
Reverse Recovery Charge	$Q_{rr}$	$V_{DS} = 800$ V, $I_S = 40$ A, $V_{GS} = 0$ V, $R_G = 30$ $\Omega$ , $di/dt = 2100$ A/ $\mu$ s, $T_J = 150$ °C	-	374	-	nC
Reverse Recovery Time	$t_{rr}$		-	30	-	ns

# UF4SC120023K4S

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = +25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>TYPICAL PERFORMANCE – DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 0 V, f = 100 kHz	–	1430	–	pF
Output Capacitance	C <sub>oss</sub>		–	85	–	
Reverse Transfer Capacitance	C <sub>rss</sub>		–	2	–	
Effective Output Capacitance, Energy Related	C <sub>oss(er)</sub>	V <sub>DS</sub> = 0 V to 800 V, V <sub>GS</sub> = 0 V	–	108	–	pF
Effective Output Capacitance, Time Related	C <sub>oss(tr)</sub>		–	200	–	
C <sub>oss</sub> Stored Energy	E <sub>oss</sub>	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 0 V	–	35	–	μJ
Total Gate Charge	Q <sub>G</sub>	V <sub>DS</sub> = 800 V, I <sub>D</sub> = 40 A, V <sub>GS</sub> = 0 V to 15 V	–	37.8	–	nC
Gate-drain Charge	Q <sub>GD</sub>		–	8	–	
Gate-source Charge	Q <sub>GS</sub>		–	11.8	–	
Turn-on Delay Time	t <sub>d(on)</sub>	(Note 4) and (Note 5) V <sub>DS</sub> = 800 V, I <sub>D</sub> = 40 A, Gate Driver = 0 V to +15 V, R <sub>G_ON</sub> = 1 Ω, R <sub>G_OFF</sub> = 18 Ω Inductive Load, FWD: same device with V <sub>GS</sub> = 0 V and R <sub>G</sub> = 18 Ω, Snubber: R <sub>s</sub> = 20 Ω, C <sub>s</sub> = 100 pF, T <sub>J</sub> = 25 °C	–	10	–	ns
Rise Time	t <sub>r</sub>		–	24	–	
Turn-off Delay Time	t <sub>d(off)</sub>		–	72	–	
Fall Time	t <sub>f</sub>		–	13.6	–	
Turn-on Energy Including R <sub>S</sub> Energy	E <sub>ON</sub>		–	599	–	μJ
Turn-off Energy Including R <sub>S</sub> Energy	E <sub>OFF</sub>		–	195	–	
Total Switching Energy	E <sub>TOTAL</sub>		–	794	–	
Snubber R <sub>S</sub> Energy During Turn-on	E <sub>RS_ON</sub>		–	7	–	
Snubber R <sub>S</sub> Energy During Turn-off	E <sub>RS_OFF</sub>		–	10	–	
Turn-on Delay Time	t <sub>d(on)</sub>		(Note 4) and (Note 5) V <sub>DS</sub> = 800 V, I <sub>D</sub> = 40 A, Gate Driver = 0 V to +15 V, R <sub>G_ON</sub> = 1 Ω, R <sub>G_OFF</sub> = 18 Ω Inductive Load, FWD: same device with V <sub>GS</sub> = 0 V and R <sub>G</sub> = 18 Ω, Snubber: R <sub>s</sub> = 20 Ω, C <sub>s</sub> = 100 pF, T <sub>J</sub> = 150 °C	–	9.2	
Rise Time	t <sub>r</sub>	–		26	–	
Turn-off Delay Time	t <sub>d(off)</sub>	–		81	–	
Fall Time	t <sub>f</sub>	–		14	–	
Turn-on Energy Including R <sub>S</sub> Energy	E <sub>ON</sub>	–		678	–	μJ
Turn-off Energy Including R <sub>S</sub> Energy	E <sub>OFF</sub>	–		239	–	
Total Switching Energy	E <sub>TOTAL</sub>	–		917	–	
Snubber R <sub>S</sub> Energy During Turn-on	E <sub>RS_ON</sub>	–		6	–	
Snubber R <sub>S</sub> Energy During Turn-off	E <sub>RS_OFF</sub>	–		9	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Measured with the switching test circuit in Figure 26.

5. All the switching energies (turn-on energy, turn-off energy and total energy) presented in this table include the device RC snubber energy losses.

TYPICAL PERFORMANCE DIAGRAMS

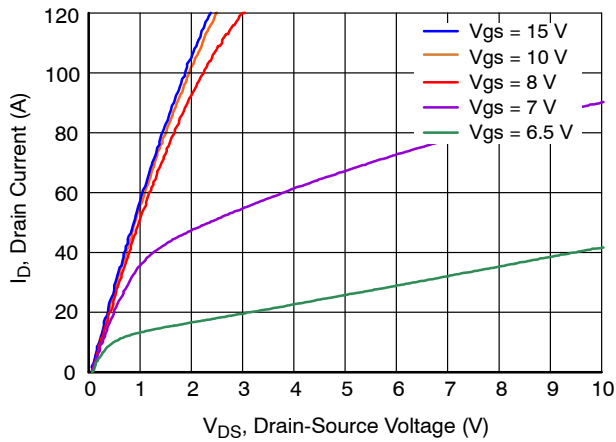


Figure 1. Typical Output Characteristics at  $T_J = -55^\circ\text{C}$

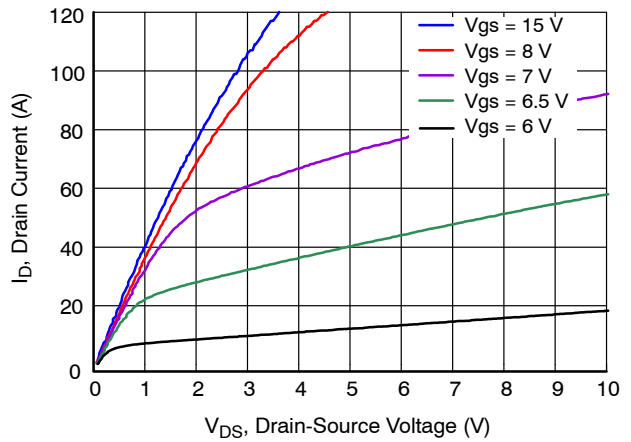


Figure 2. Typical Output Characteristics at  $T_J = 25^\circ\text{C}$

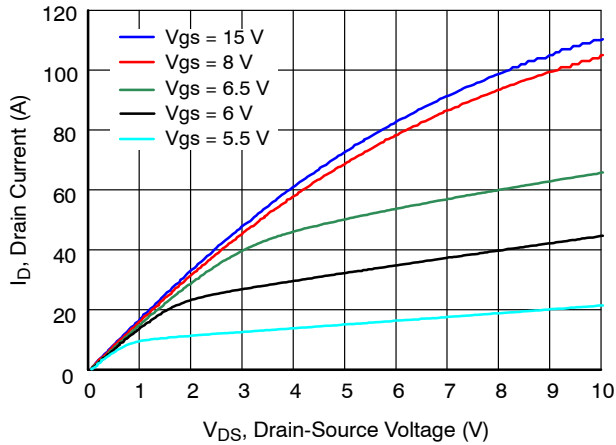


Figure 3. Typical Output Characteristics at  $T_J = 175^\circ\text{C}$ ,  $t_p < 250\ \mu\text{s}$

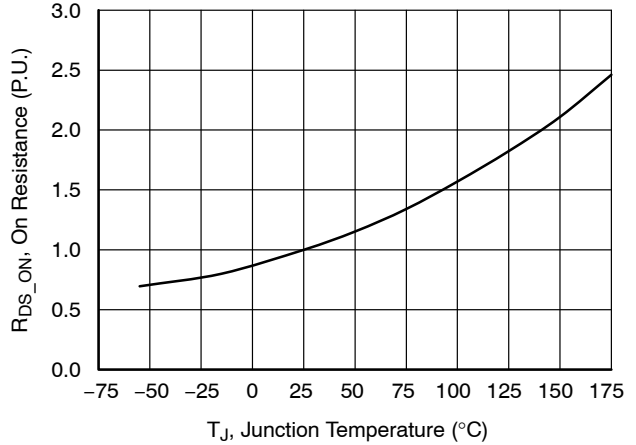


Figure 4. Normalized On-Resistance vs. Temperature at  $V_{GS} = 12\ \text{V}$  and  $I_D = 40\ \text{A}$

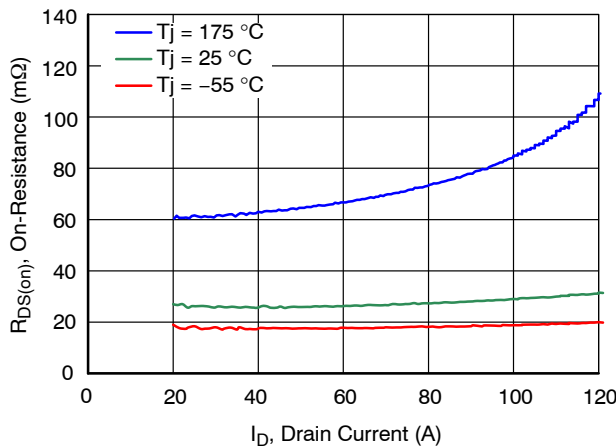


Figure 5. Typical Drain-Source On-Resistances at  $V_{GS} = 12\ \text{V}$

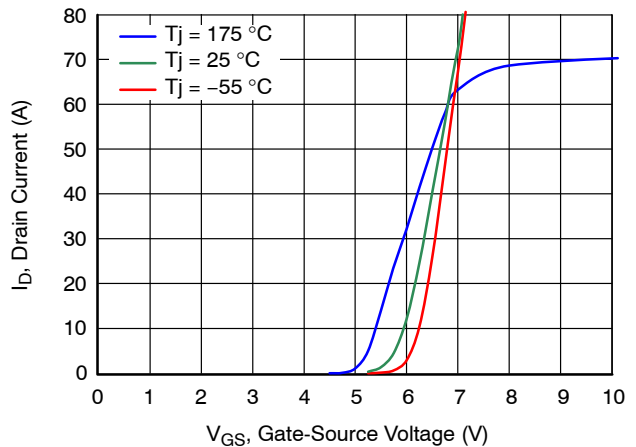


Figure 6. Typical Transfer Characteristics at  $V_{DS} = 5\ \text{V}$

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

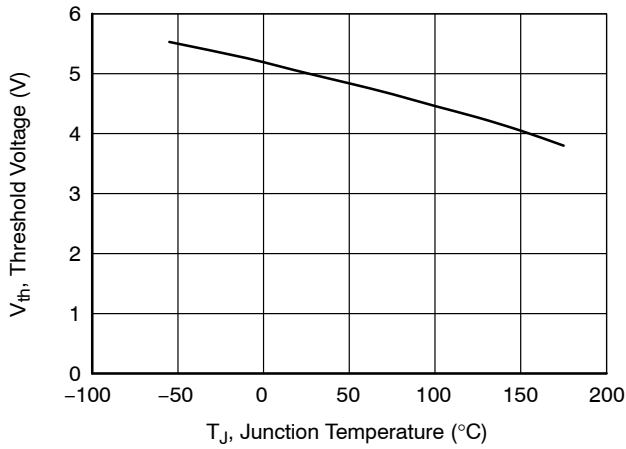


Figure 7. Threshold Voltage vs. Junction Temperature at  $V_{DS} = 5\text{ V}$  and  $I_D = 10\text{ mA}$

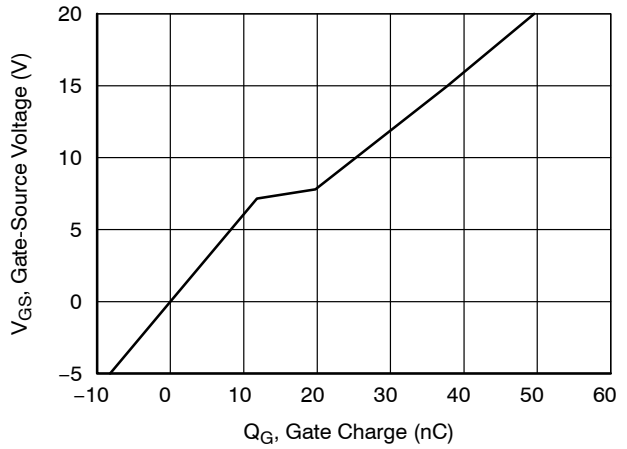


Figure 8. Typical Gate Charge at  $V_{DS} = 800\text{ V}$  and  $I_D = 40\text{ A}$

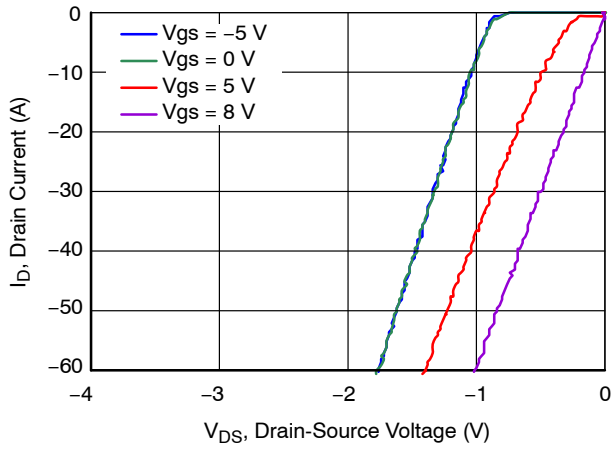


Figure 9. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = -55\text{ }^\circ\text{C}$

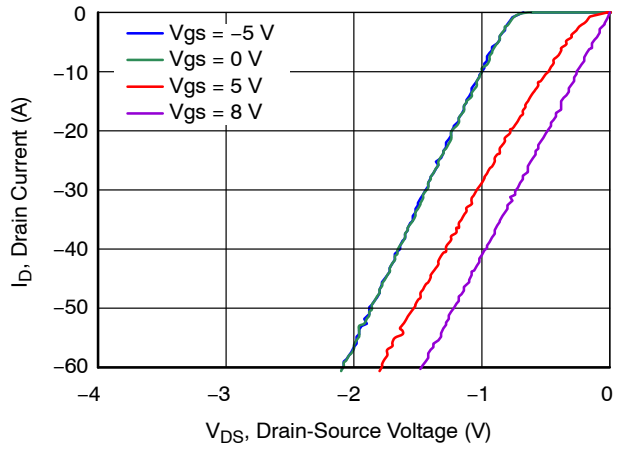


Figure 10. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = 25\text{ }^\circ\text{C}$

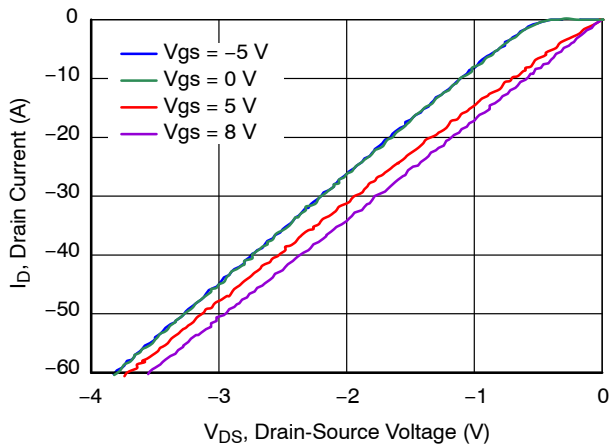


Figure 11. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = 175\text{ }^\circ\text{C}$

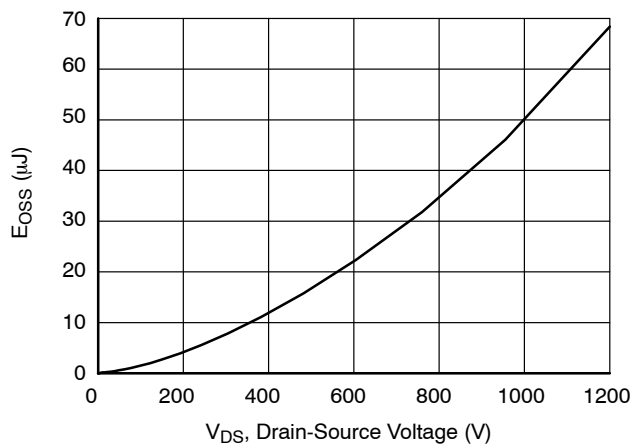


Figure 12. Typical Stored Energy in  $C_{OSS}$  at  $V_{GS} = 0\text{ V}$

# UF4SC120023K4S

## TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

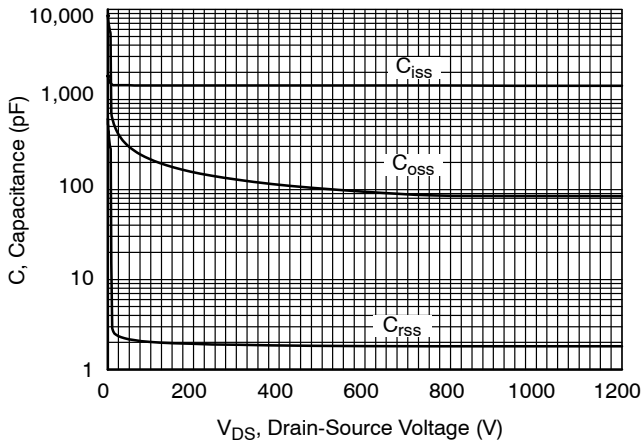


Figure 13. Typical Capacitances at  $f = 100$  kHz and  $V_{GS} = 0$  V

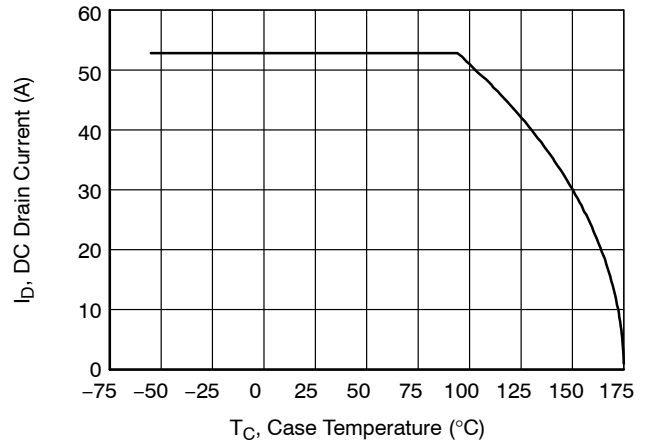


Figure 14. DC Drain Current Derating

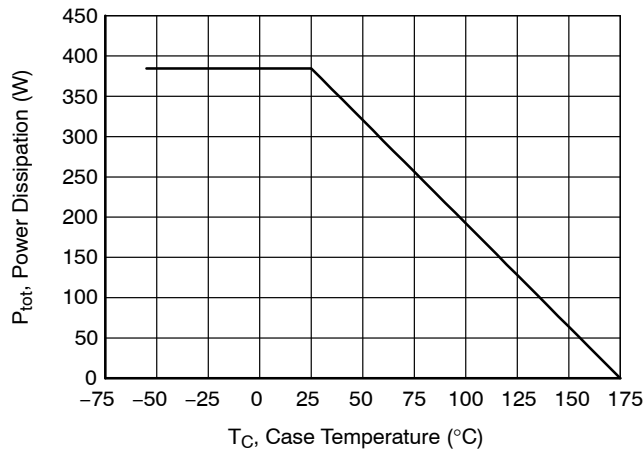


Figure 15. Total Power Dissipation

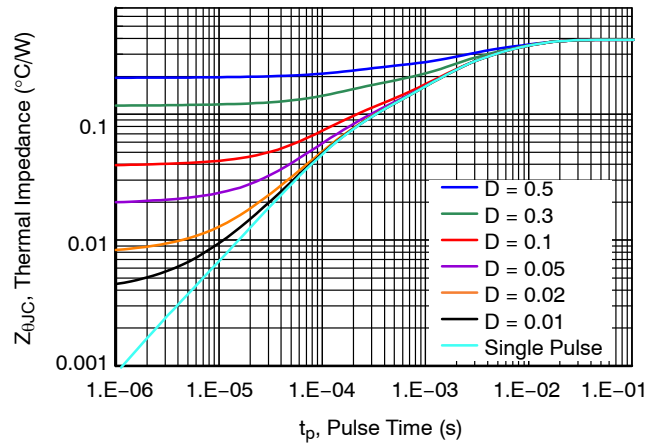


Figure 16. Maximum Transient Thermal Impedance

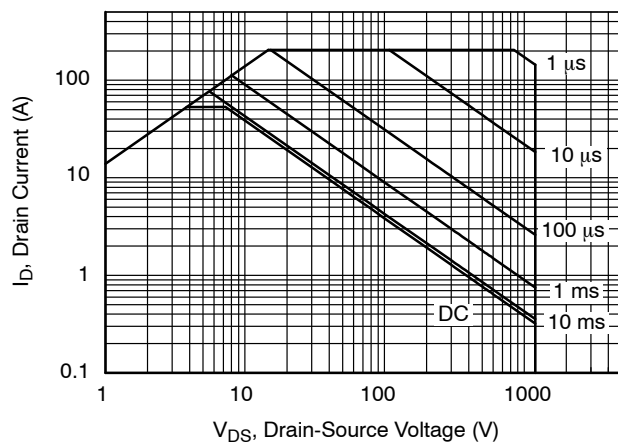


Figure 17. Safe Operation Area at  $T_C = 25$   $^{\circ}C$ ,  $D = 0$ , Parameter  $t_p$

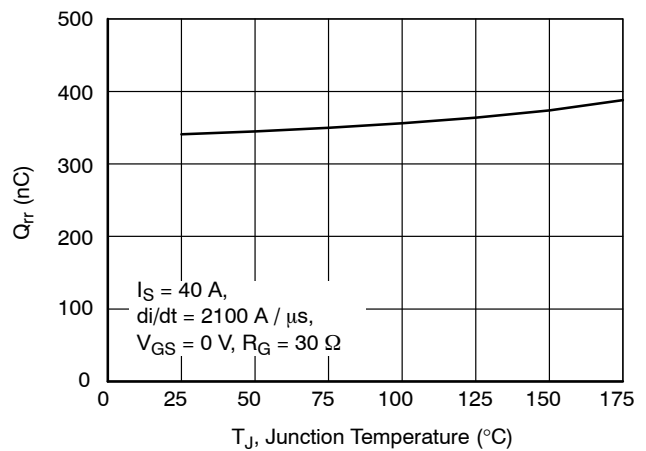


Figure 18. Reverse Recovery Charge  $Q_{rr}$  vs. Junction Temperature at  $V_{DS} = 800$  V

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

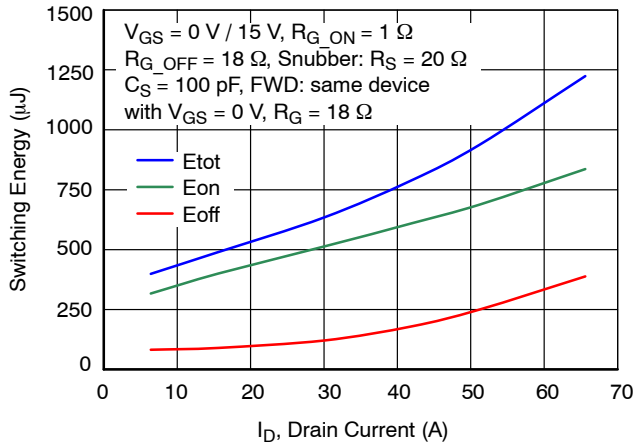


Figure 19. Clamped Inductive Switching Energies vs. Drain Current at  $V_{DS} = 800\text{ V}$  and  $T_J = 25\text{ }^\circ\text{C}$

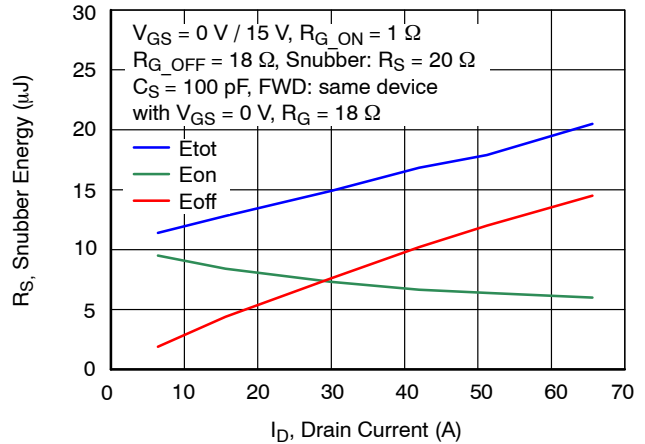


Figure 20. RC Snubber Energy Losses vs. Drain Current at  $V_{DS} = 800\text{ V}$  and  $T_J = 25\text{ }^\circ\text{C}$

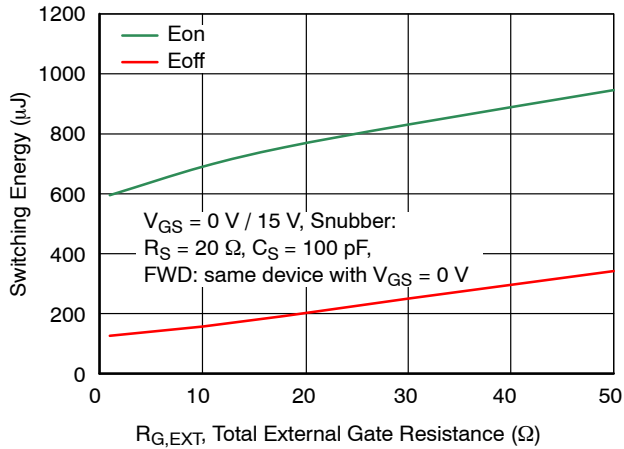


Figure 21. Clamped Inductive Switching Energies vs.  $R_{G,EXT}$  at  $V_{DS} = 800\text{ V}$ ,  $I_D = 40\text{ A}$ , and  $T_J = 25\text{ }^\circ\text{C}$

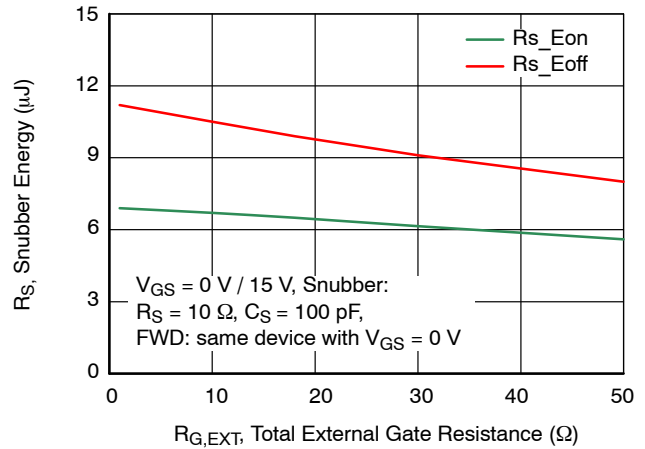


Figure 22. RC Snubber Energy Losses vs.  $R_{G,EXT}$  at  $V_{DS} = 800\text{ V}$ ,  $I_D = 40\text{ A}$ , and  $T_J = 25\text{ }^\circ\text{C}$

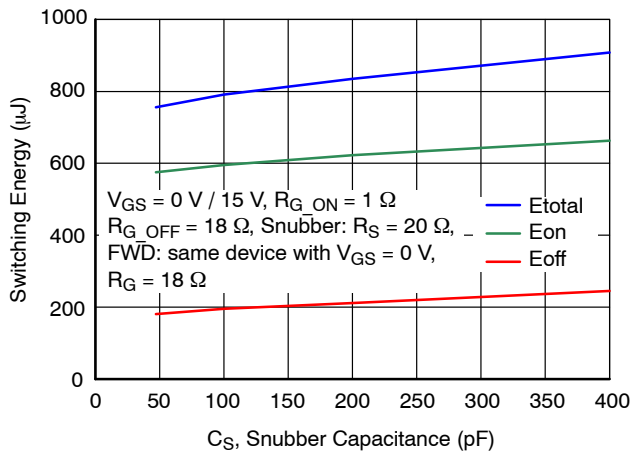


Figure 23. Clamped Inductive Switching Energies vs. Snubber Capacitance  $C_S$  at  $V_{DS} = 800\text{ V}$ ,  $I_D = 40\text{ A}$ , and  $T_J = 25\text{ }^\circ\text{C}$

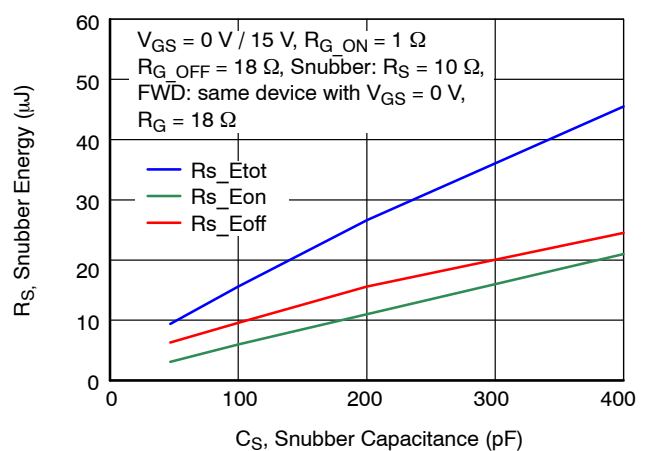
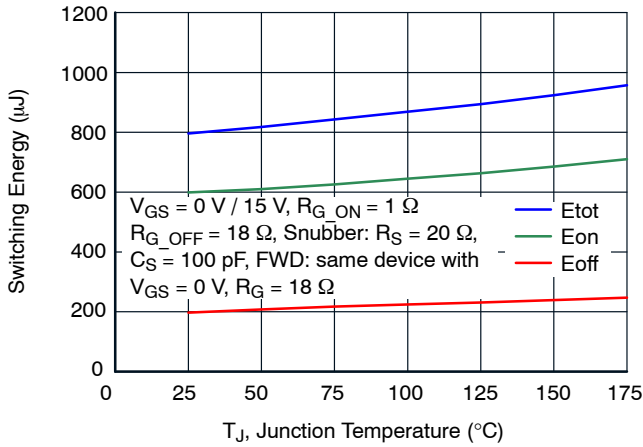
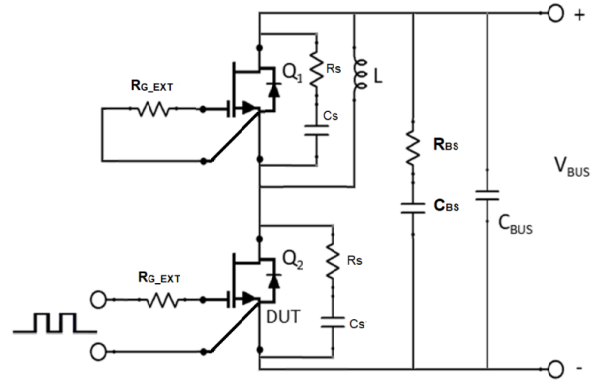


Figure 24. RC Snubber Energy Losses vs. Snubber Capacitance  $C_S$  at  $V_{DS} = 800\text{ V}$ ,  $I_D = 40\text{ A}$ , and  $T_J = 25\text{ }^\circ\text{C}$

# UF4SC120023K4S



**Figure 25. Clamped Inductive Switching Energy vs. Junction Temperature at  $V_{DS} = 800\text{ V}$  and  $I_D = 40\text{ A}$**



**Figure 26. Schematic of the Half-Bridge Mode Switching Test Circuit. Note, a Bus RC Snubber ( $R_{BS} = 5\ \Omega$ ,  $C_{BS} = 100\text{ nF}$ ) is Used to Reduce the Power Loop High Frequency Oscillations.**

## APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ( $R_{DS(on)}$ ), output capacitance ( $C_{oss}$ ), gate charge ( $Q_G$ ), and reverse recovery charge ( $Q_{rr}$ ) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high  $dv/dt$  and  $di/dt$  rates. An external gate resistor is recommended when the FET is

working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see [www.onsemi.com](http://www.onsemi.com).

A snubber circuit with a small  $R_{(G)}$ , or gate resistor, provides better EMI suppression with higher efficiency compared to using a high  $R_{(G)}$ , value. There is no extra gate delay time when using the snubber circuitry, and a small  $R_{(G)}$ , will better control both the turn-off  $V_{(DS)}$  peak spike and ringing duration, while a high  $R_{(G)}$  will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high  $R_{(G)}$ , while greatly reducing  $E_{(OFF)}$  from mid-to-full load range with only a small increase in  $E_{(ON)}$ . Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the [onsemi](http://www.onsemi.com) website at [www.onsemi.com](http://www.onsemi.com).

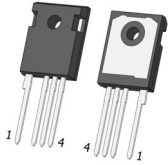
## ORDERING INFORMATION

Part Number	Marking	Package	Shipping
UF4SC120023K4S	UF4SC120023K4S	TO247-4	600 Units / Tube

# UF4SC120023K4S

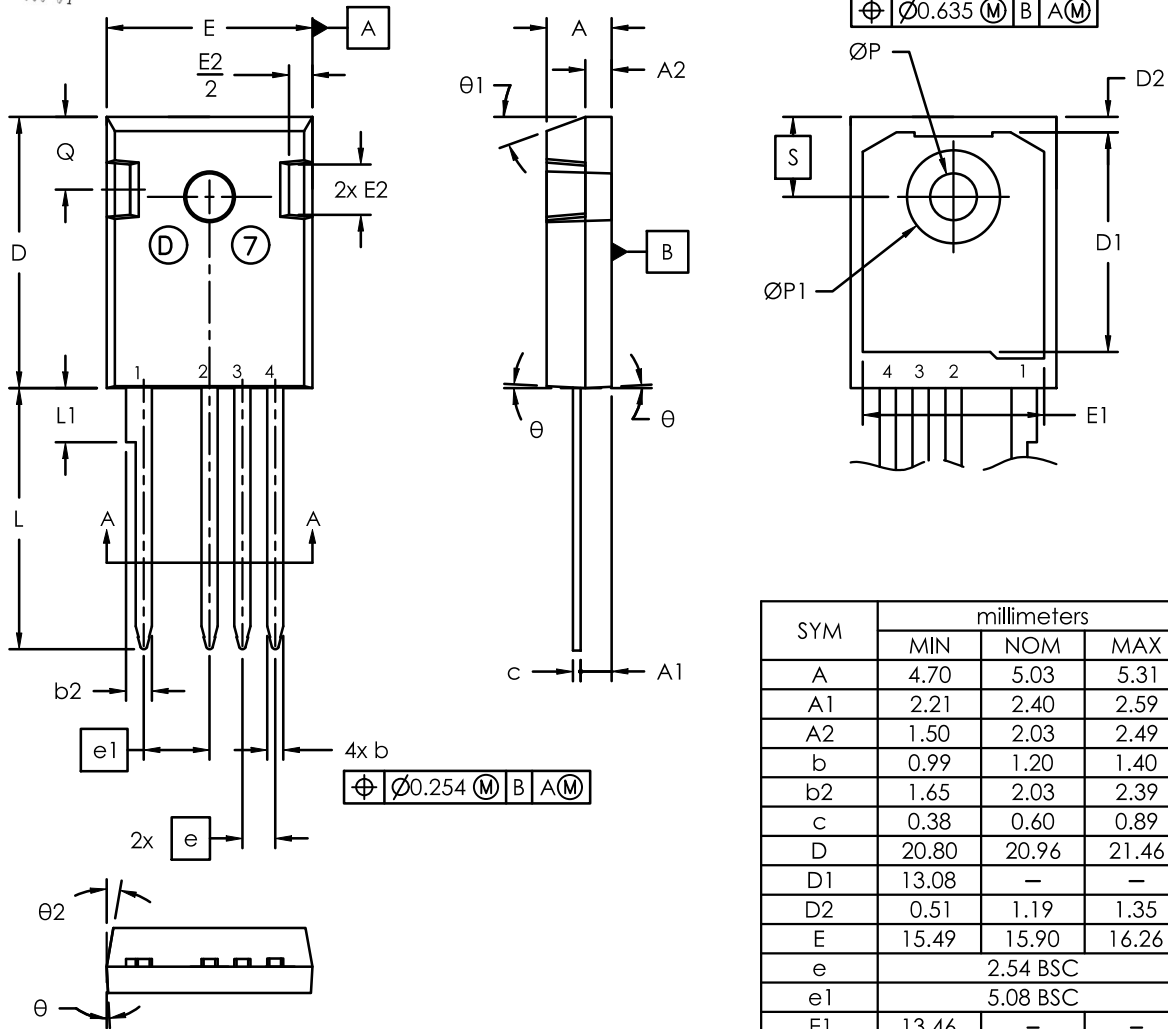
## REVISION HISTORY

Revision	Description of Changes	Date
B	Acquired the original Qorvo JFET Division Data Sheet and updated the main document title to comply with <b>onsemi</b> standards for SiC products.	1/15/2025
2	Converted the Data Sheet to <b>onsemi</b> format.	06/25/2025



TO247-4 15.90x20.96x5.03, 5.44P  
CASE 340AN  
ISSUE E

DATE 20 JUN 2025



$\text{Ø} \ 0.254 \text{ (M) B A (M)}$

$\text{Ø} \ 0.635 \text{ (M) B A (M)}$

SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
c	0.38	0.60	0.89
D	20.80	20.96	21.46
D1	13.08	—	—
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	2.54 BSC		
e1	5.08 BSC		
E1	13.46	—	—
E2	3.43	3.89	5.20
L	19.81	20.17	20.32
L1	—	—	4.50
ØP	3.40	3.60	3.80
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.17 BSC		
θ	3°		
θ1	20°		
θ2	10°		

NOTE:

1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.
5. Through Hole diameter value = End Hole diameter
6. PCB Through Hole pattern as per IPC-2221/IPC-2222

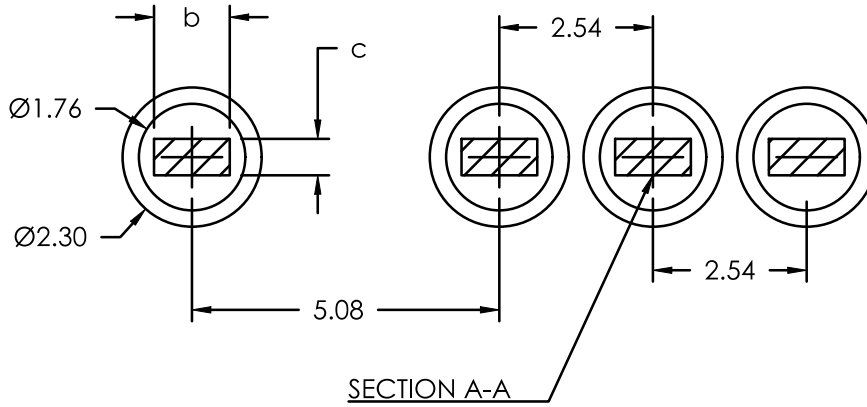
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**TO247-4 15.90x20.96x5.03, 5.44P**  
**CASE 340AN**  
**ISSUE E**

DATE 20 JUN 2025

RECOMMENDED PCB THROUGH HOLE



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.  
 END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

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