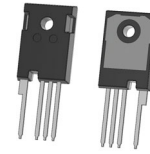


# Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, TO247-4LH, 1200 V, 9.1 mohm


 TO247-4LH  
 CASE 340CV

## UF4SC120009K4SH

### Description

The UF4SC120009K4SH is a 1200 V, 9.1 mΩ G4 SiC FET. It is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows use of off-the-shelf gate drivers hence requiring minimal redesign when replacing Si IGBTs, Si superjunction devices or SiC MOSFETs. Available in the TO247-4LH HV package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

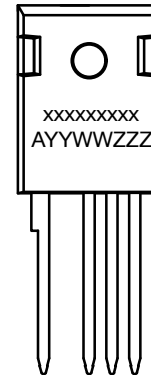
### Features

- On-resistance  $R_{DS(on)}$ , of 9.1 mΩ (typ)
- Operating Temperature of 175 °C
- Excellent Reverse Recovery:  $Q_{rr} = 615$  nC
- Low Body Diode  $V_{FSD}$ : 1.09 V
- Low Gate Charge:  $Q_G = 168$  nC
- Threshold Voltage  $V_{G(th)}$ : 4.7 V (typ) Allowing 0 to 15 V Drive
- Low Intrinsic Capacitance
- Kelvin Source Pin for Optimized Switching Performance
- HV Package With 8 mm D-S Creepage Distance
- ESD Protected, HBM Class 2 and CDM Class C3
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

### Typical Applications

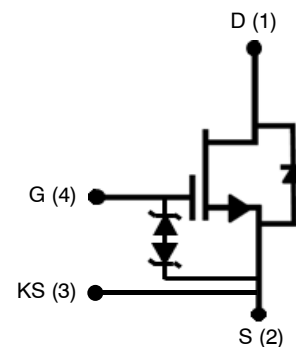
- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating

### MARKING DIAGRAM



XXXXXXXX = Specific Device Number  
 A = Assembly Location  
 YY = Year  
 WW = Work Week  
 ZZZ = Lot ID

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

# UF4SC120009K4SH

## MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	$V_{DS}$		1200	V
Gate-source Voltage	$V_{GS}$	DC	-20 to +20	V
		AC (f > 1 Hz)	-25 to +25	V
Continuous Drain Current (Note 1)	$I_D$	$T_C < 100\text{ }^\circ\text{C}$	120	A
Pulsed Drain Current (Note 2)	$I_{DM}$	$T_C = 25\text{ }^\circ\text{C}$	550	A
Single Pulsed Avalanche Energy (Note 3)	$E_{AS}$	L = 15 mH, $I_{AS} = 6.5\text{ A}$	317	mJ
Power Dissipation	$P_{tot}$	$T_C = 25\text{ }^\circ\text{C}$	750	W
SiC FET dv/dt Ruggedness	dv/dt	$V_{DS} < 800\text{ V}$	150	V/ns
Maximum Junction Temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{STG}$		-55 to 175	$^\circ\text{C}$
Max. Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	$T_L$		250	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Limited by bondwires.
- Pulse width  $t_p$  limited by  $T_{J,max}$
- Starting  $T_J = 25\text{ }^\circ\text{C}$

## THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		-	0.15	0.20	$^\circ\text{C/W}$

## ELECTRICAL CHARACTERISTICS ( $T_J = +25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### TYPICAL PERFORMANCE – STATIC

Drain-source Breakdown Voltage	$BV_{DS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	1200	-	-	V	
Total Drain Leakage Current	$I_{DSS}$	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 25\text{ }^\circ\text{C}$	-	5	300	$\mu\text{A}$	
		$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	56	-		
Total Gate Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, T_J = 25\text{ }^\circ\text{C}, V_{GS} = -20\text{ V}/+20\text{ V}$	-	6	20	$\mu\text{A}$	
Drain-source On-resistance	$R_{DS(on)}$	$V_{GS} = 12\text{ V}, I_D = 80\text{ A}$	$T_J = 25\text{ }^\circ\text{C}$	-	9.1	10.6	$\text{m}\Omega$
			$T_J = 125\text{ }^\circ\text{C}$	-	16.9	-	
			$T_J = 175\text{ }^\circ\text{C}$	-	23.3	-	
Gate Threshold Voltage	$V_{G(th)}$	$V_{DS} = 5\text{ V}, I_D = 10\text{ mA}$	4	4.7	6	V	
Gate Resistance	$R_G$	f = 1 MHz, open drain	-	0.8	1.5	$\Omega$	

### TYPICAL PERFORMANCE – REVERSE DIODE

Diode Continuous Forward Current	$I_S$	$T_C < 100\text{ }^\circ\text{C}$	-	-	120	A
Diode Pulse Current	$I_{S,pulse}$	$T_C = 25\text{ }^\circ\text{C}$	-	-	550	A
Forward Voltage	$V_{FSD}$	$V_{GS} = 0\text{ V}, I_F = 40\text{ A}, T_J = 25\text{ }^\circ\text{C}$	-	1.09	1.45	V
		$V_{GS} = 0\text{ V}, I_S = 40\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	1.31	-	
Reverse Recovery Charge	$Q_{rr}$	$V_{DS} = 800\text{ V}, I_S = 80\text{ A}, V_{GS} = 0\text{ V}, R_{G,EXT} = 2\text{ }\Omega, di/dt = 2600\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	-	615	-	nC
Reverse Recovery Time	$t_{rr}$		-	48	-	ns
Reverse Recovery Charge	$Q_{rr}$	$V_{DS} = 800\text{ V}, I_S = 80\text{ A}, V_{GS} = 0\text{ V}, R_{G,EXT} = 2\text{ }\Omega, di/dt = 2600\text{ A}/\mu\text{s}, T_J = 150\text{ }^\circ\text{C}$	-	724	-	nC
Reverse Recovery Time	$t_{rr}$		-	55	-	ns

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = +25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
<b>TYPICAL PERFORMANCE – DYNAMIC</b>							
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 0 V, f = 100 kHz	–	7218	–	pF	
Output Capacitance	C <sub>OSS</sub>		–	204	–		
Reverse Transfer Capacitance	C <sub>rss</sub>		–	0.2	–		
Effective Output Capacitance, Energy Related	C <sub>OSS(er)</sub>	V <sub>DS</sub> = 0 V to 800 V, V <sub>GS</sub> = 0 V	–	265	–	pF	
Effective Output Capacitance, Time Related	C <sub>OSS(tr)</sub>		–	528	–	pF	
C <sub>OSS</sub> Stored Energy	E <sub>OSS</sub>	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 0 V	–	85	–	μJ	
Total Gate Charge	Q <sub>G</sub>	V <sub>DS</sub> = 800 V, I <sub>D</sub> = 80 A, V <sub>GS</sub> = 0 V to 15 V	–	168	–	nC	
Gate-drain Charge	Q <sub>GD</sub>		–	28	–		
Gate-source Charge	Q <sub>GS</sub>		–	50	–		
Turn-on Delay Time	t <sub>d(on)</sub>	(Notes 4 and 5) V <sub>DS</sub> = 800 V, I <sub>D</sub> = 80 A, Gate Driver = 0 V to +15 V, R <sub>G,EXT</sub> = 2 Ω, Inductive Load, FWD: Same Device With V <sub>GS</sub> = 0 V, R <sub>G</sub> = 2 Ω, RC Snubber: R <sub>S</sub> = 5 Ω, C <sub>S</sub> = 440 pF, T <sub>J</sub> = 25 °C	–	40	–	ns	
Rise Time	t <sub>r</sub>		–	37	–		
Turn-off Delay Time	t <sub>d(off)</sub>		–	81	–		
Fall Time	t <sub>f</sub>		–	16	–	μJ	
Turn-on Energy Including R <sub>S</sub> Energy	E <sub>ON</sub>		–	1656	–		
Turn-off Energy Including R <sub>S</sub> Energy	E <sub>OFF</sub>		–	255	–		
Total Switching Energy Including R <sub>S</sub> Energy	E <sub>TOTAL</sub>		–	1911	–		
Snubber R <sub>S</sub> Energy During Turn-on	E <sub>RS_ON</sub>		–	19.5	–		
Snubber R <sub>S</sub> Energy During Turn-off	E <sub>RS_OFF</sub>		–	76.5	–		
Turn-on Delay Time	t <sub>d(on)</sub>		(Notes 4 and 5) V <sub>DS</sub> = 800 V, I <sub>D</sub> = 80 A, Gate Driver = 0 V to +15 V, R <sub>G,EXT</sub> = 2 Ω, Inductive Load, FWD: Same Device With V <sub>GS</sub> = 0 V, R <sub>G</sub> = 2 Ω, RC Snubber: R <sub>S</sub> = 5 Ω, C <sub>S</sub> = 440 pF, T <sub>J</sub> = 150 °C	–	36		–
Rise Time	t <sub>r</sub>			–	42	–	
Turn-off Delay Time	t <sub>d(off)</sub>			–	85	–	
Fall Time	t <sub>f</sub>			–	18	–	μJ
Turn-on Energy Including R <sub>S</sub> Energy	E <sub>ON</sub>	–		1940	–		
Turn-off Energy Including R <sub>S</sub> Energy	E <sub>OFF</sub>	–		283	–		
Total Switching Energy Including R <sub>S</sub> Energy	E <sub>TOTAL</sub>	–		2223	–		
Snubber R <sub>S</sub> Energy During Turn-on	E <sub>RS_ON</sub>	–		18	–		
Snubber R <sub>S</sub> Energy During Turn-off	E <sub>RS_OFF</sub>	–		71	–		
Turn-on Delay Time	t <sub>d(on)</sub>	(Notes 5 and 6) V <sub>DS</sub> = 800 V, I <sub>D</sub> = 80 A, Gate Driver = 0 V to +15 V, R <sub>G,EXT</sub> = 2 Ω, Inductive Load, FWD: UJ3D1250K2, RC Snubber: R <sub>S</sub> = 5 Ω, C <sub>S</sub> = 440 pF, T <sub>J</sub> = 25 °C		–	40	–	
Rise Time	t <sub>r</sub>			–	30	–	
Turn-off Delay Time	t <sub>d(off)</sub>			–	81	–	
Fall Time	t <sub>f</sub>			–	13	–	μJ
Turn-on Energy Including R <sub>S</sub> Energy	E <sub>ON</sub>		–	918	–		
Turn-off Energy Including R <sub>S</sub> Energy	E <sub>OFF</sub>		–	250	–		
Total Switching Energy Including R <sub>S</sub> Energy	E <sub>TOTAL</sub>		–	1168	–		
Snubber R <sub>S</sub> Energy During Turn-on	E <sub>RS_ON</sub>		–	18	–		
Snubber R <sub>S</sub> Energy During Turn-off	E <sub>RS_OFF</sub>		–	113	–		

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## ELECTRICAL CHARACTERISTICS ( $T_J = +25\text{ }^\circ\text{C}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>TYPICAL PERFORMANCE – DYNAMIC</b>						
Turn-on Delay Time	$t_{d(on)}$	(Notes 5 and 6) $V_{DS} = 800\text{ V}$ , $I_D = 80\text{ A}$ , Gate Driver = $0\text{ V}$ to $+15\text{ V}$ , $R_{G,EXT} = 2\ \Omega$ , Inductive Load, FWD: UJ3D1250K2, RC Snubber: $R_S = 5\ \Omega$ , $C_S = 440\text{ pF}$ , $T_J = 150\text{ }^\circ\text{C}$	–	36	–	ns
Rise Time	$t_r$		–	34	–	
Turn-off Delay Time	$t_{d(off)}$		–	85	–	
Fall Time	$t_f$		–	14	–	
Turn-on Energy Including $R_S$ Energy	$E_{ON}$		–	1040	–	$\mu\text{J}$
Turn-off Energy Including $R_S$ Energy	$E_{OFF}$		–	280	–	
Total Switching Energy Including $R_S$ Energy	$E_{TOTAL}$		–	1320	–	
Snubber $R_S$ Energy During Turn-on	$E_{RS\_ON}$		–	16.5	–	
Snubber $R_S$ Energy During Turn-off	$E_{RS\_OFF}$		–	110	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Measured with the switching test circuit in Figure 26.

5. In this table, the switching energies (turn-on energy, turn-off energy and total energy) presented include the device RC snubber energy losses.

6. Measured with the switching test circuit in Figure 26 where the high-side switch Q1 is replaced with the diode and no RC snubber is applied for the diode.

TYPICAL PERFORMANCE DIAGRAMS

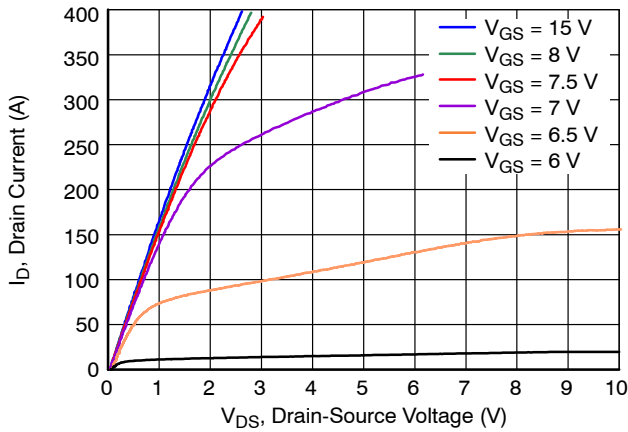


Figure 1. Typical Output Characteristics at  $T_J = -55\text{ }^\circ\text{C}$ ,  $t_p < 250\text{ }\mu\text{s}$

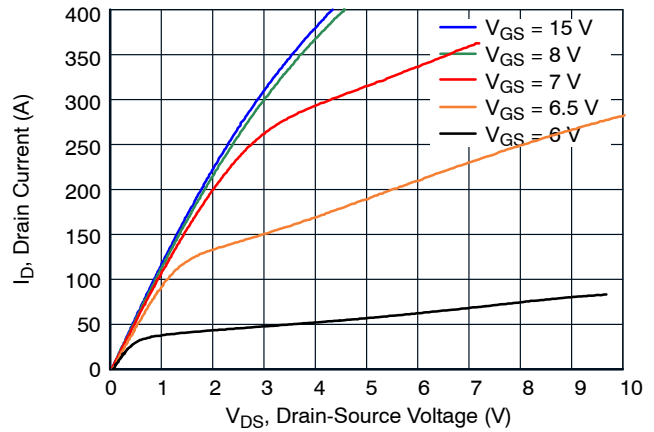


Figure 2. Typical Output Characteristics at  $T_J = 25\text{ }^\circ\text{C}$ ,  $t_p < 250\text{ }\mu\text{s}$

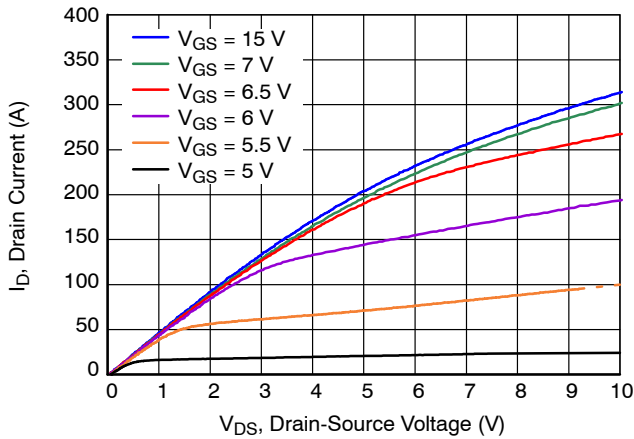


Figure 3. Typical Output Characteristics at  $T_J = 175\text{ }^\circ\text{C}$ ,  $t_p < 250\text{ }\mu\text{s}$

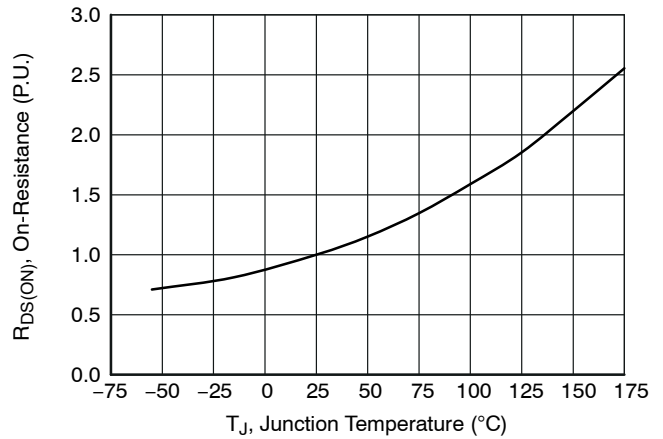


Figure 4. Normalized On-Resistance vs. Temperature at  $V_{GS} = 12\text{ V}$  and  $I_D = 80\text{ A}$

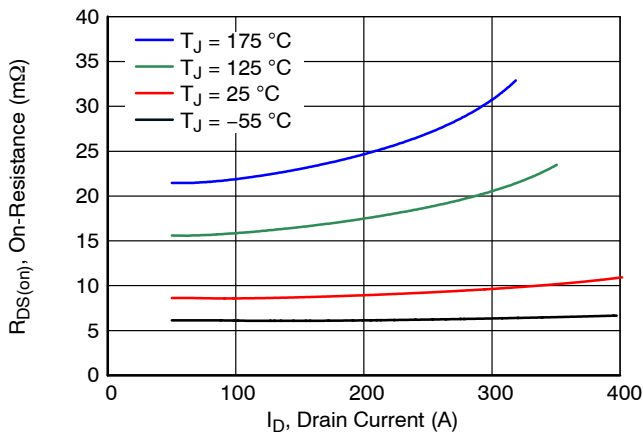


Figure 5. Typical Drain-Source On-Resistances at  $V_{GS} = 12\text{ V}$

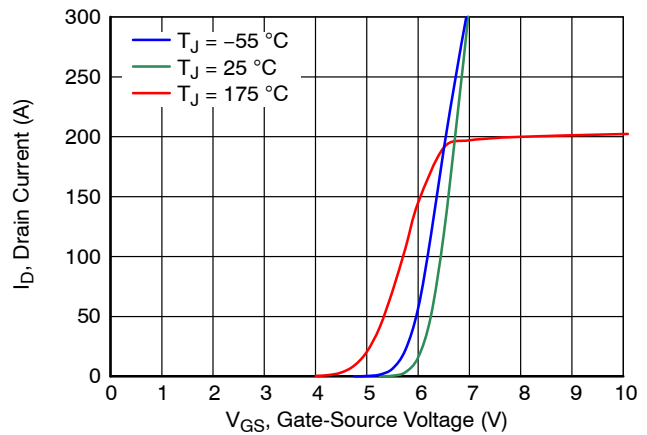


Figure 6. Typical Transfer Characteristics at  $V_{DS} = 5\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

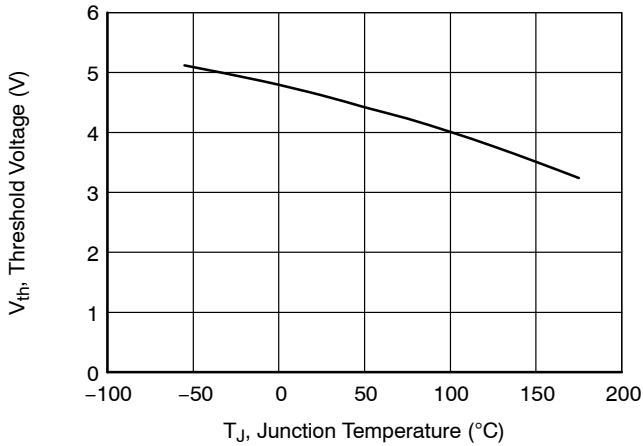


Figure 7. Threshold Voltage vs. Junction Temperature at  $V_{DS} = 5\text{ V}$  and  $I_D = 10\text{ mA}$

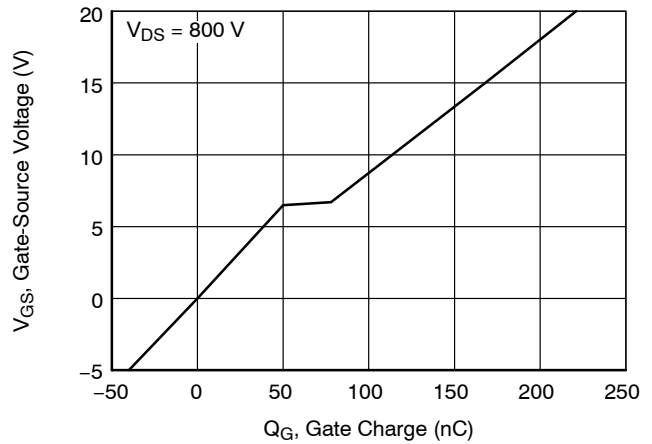


Figure 8. Typical Gate Charge at  $I_D = 80\text{ A}$

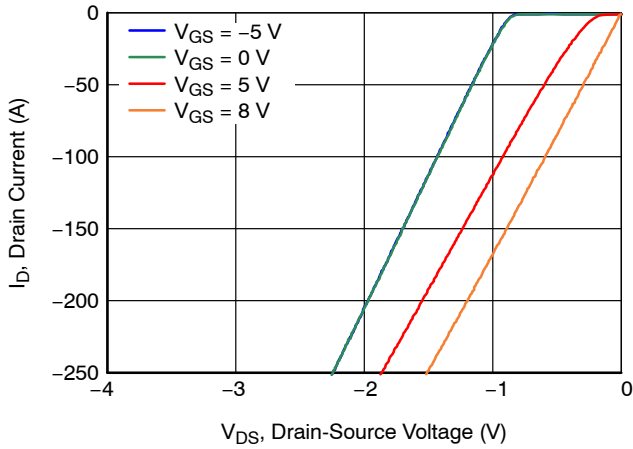


Figure 9. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = -55\text{ °C}$

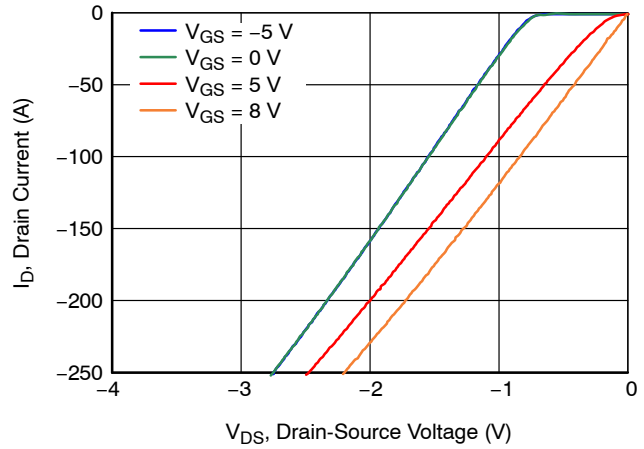


Figure 10. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = 25\text{ °C}$

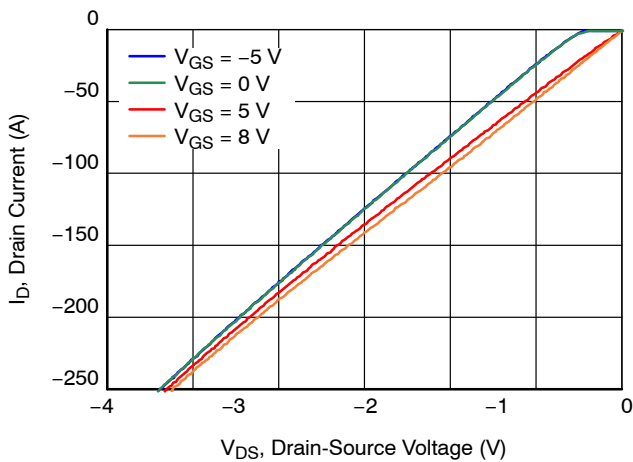


Figure 11. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = 175\text{ °C}$

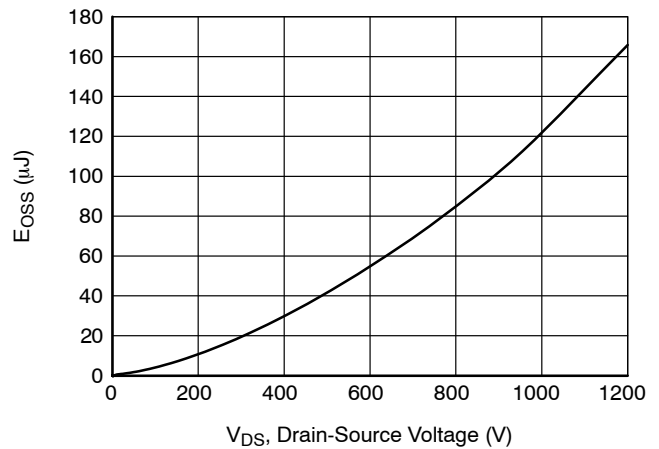
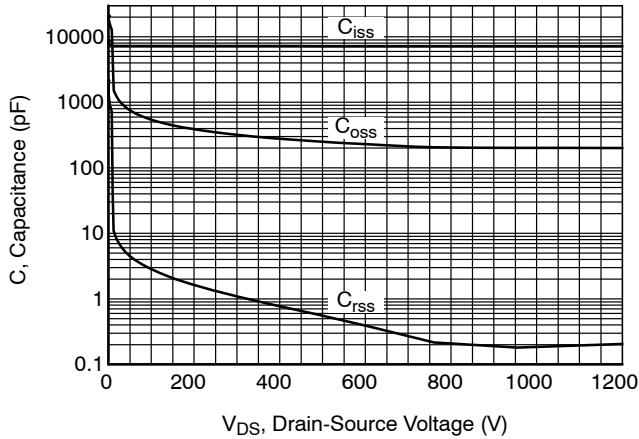


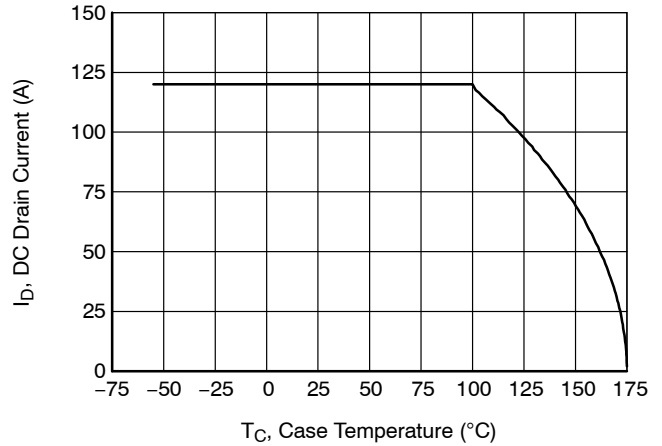
Figure 12. Typical Stored Energy in  $C_{OSS}$  at  $V_{GS} = 0\text{ V}$

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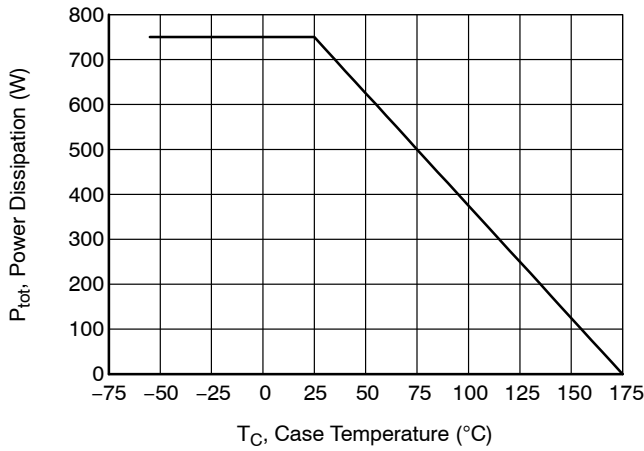
## TYPICAL PERFORMANCE DIAGRAMS (continued)



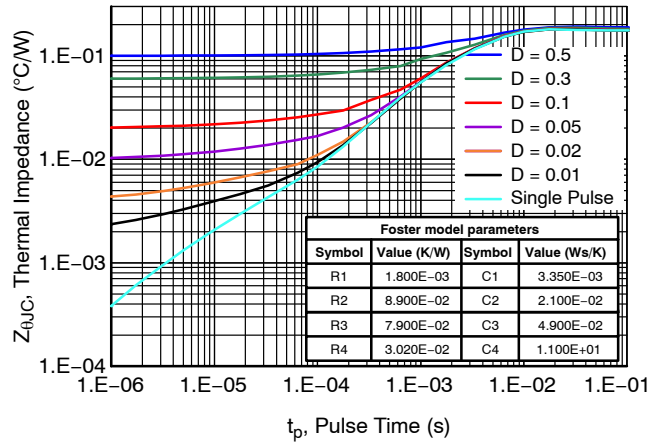
**Figure 13. Typical Capacitances at  $f = 100 \text{ kHz}$  and  $V_{GS} = 0 \text{ V}$**



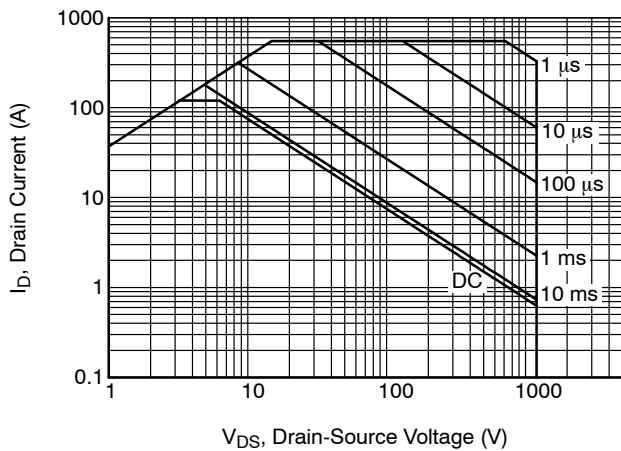
**Figure 14. DC Drain Current Derating**



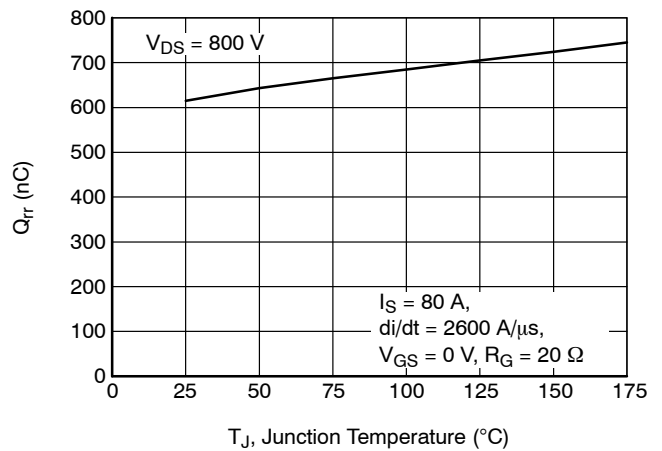
**Figure 15. Total Power Dissipation**



**Figure 16. Maximum Transient Thermal Impedance**

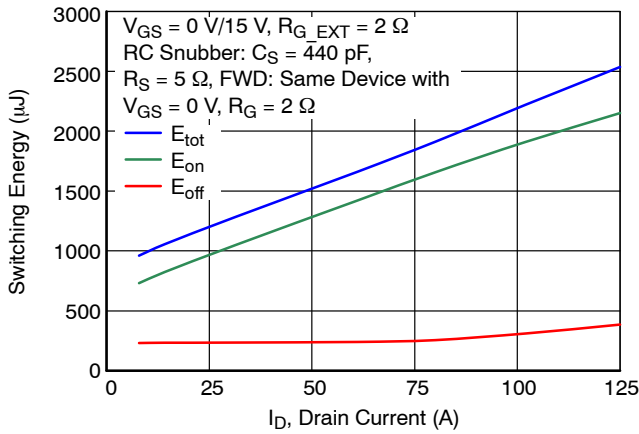


**Figure 17. Safe Operation Area at  $T_C = 25 \text{ }^\circ\text{C}$ ,  $D = 0$ , Parameter  $t_p$**

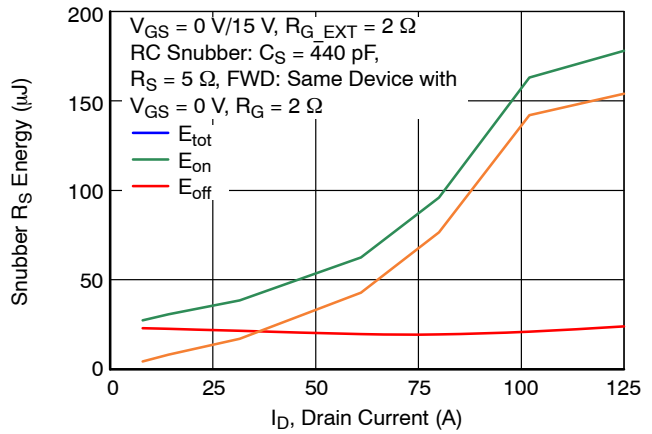


**Figure 18. Reverse Recovery Charge  $Q_{rr}$  vs. Junction Temperature**

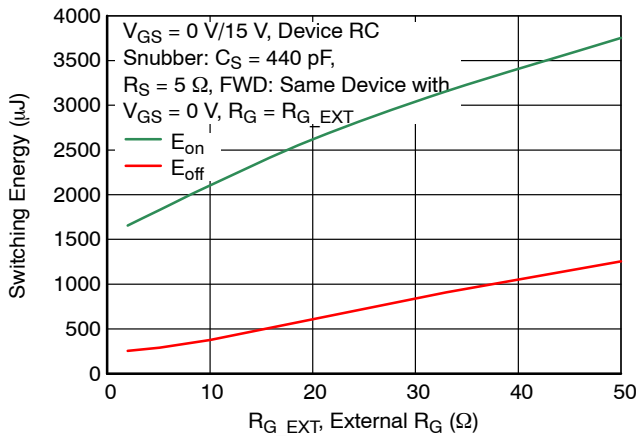
TYPICAL PERFORMANCE DIAGRAMS (continued)



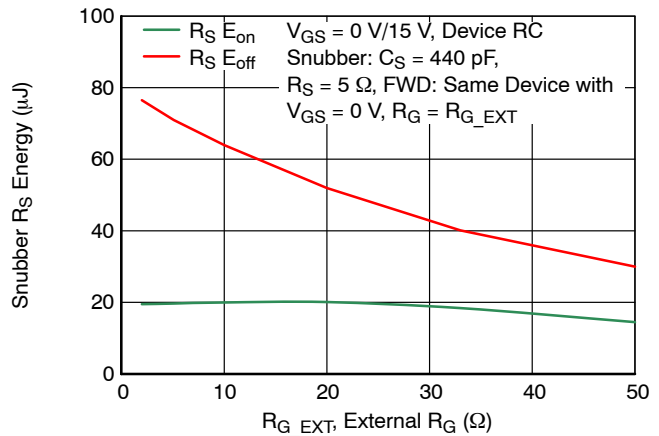
**Figure 19. Clamped Inductive Switching Energy vs. Drain Current at  $V_{DS} = 800$  V and  $T_J = 25$  °C**



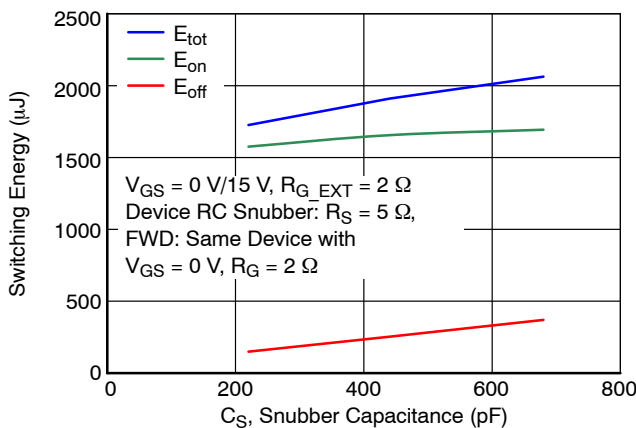
**Figure 20. RC Snubber Energy Loss vs. Drain Current at  $V_{DS} = 800$  V and  $T_J = 25$  °C**



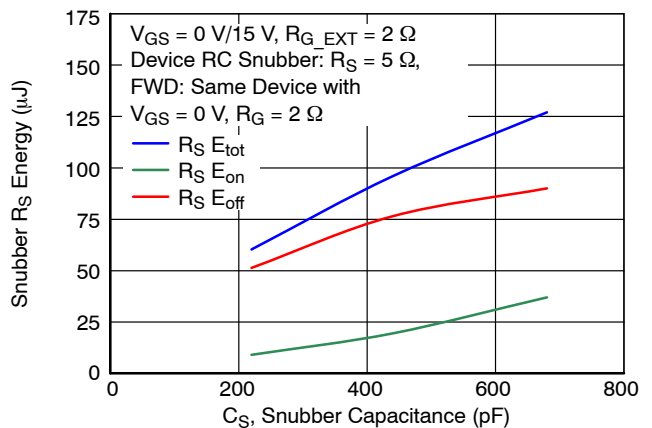
**Figure 21. Clamped Inductive Switching Energy vs.  $R_{G\_EXT}$  at  $V_{DS} = 800$  V,  $I_D = 80$  A and  $T_J = 25$  °C**



**Figure 22. Rc Snubber Energy Loss vs.  $R_{G\_EXT}$  at  $V_{DS} = 800$  V,  $I_D = 80$  A and  $T_J = 25$  °C**



**Figure 23. Clamped Inductive Switching Energies vs. Snubber Capacitance  $C_S$  at  $V_{DS} = 800$  V,  $I_D = 80$  A and  $T_J = 25$  °C**



**Figure 24. Rc Snubber Energy Losses vs. Snubber Capacitance at  $V_{DS} = 800$  V,  $I_D = 80$  A and  $T_J = 25$  °C**

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## TYPICAL PERFORMANCE DIAGRAMS (continued)

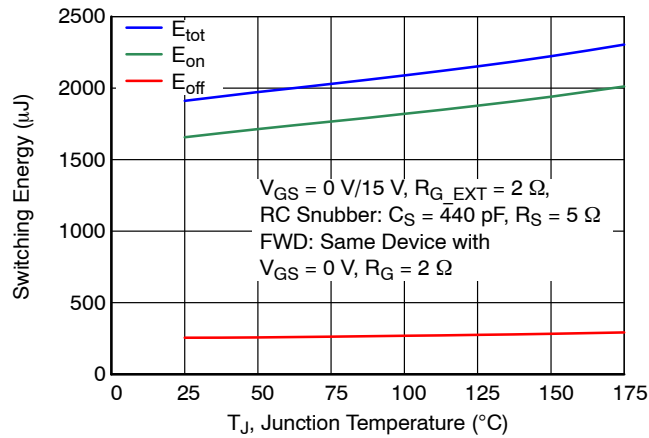


Figure 25. Clamped Inductive Switching Energy vs. Junction Temperature at  $V_{DS} = 800\text{ V}$ ,  $I_D = 80\text{ A}$

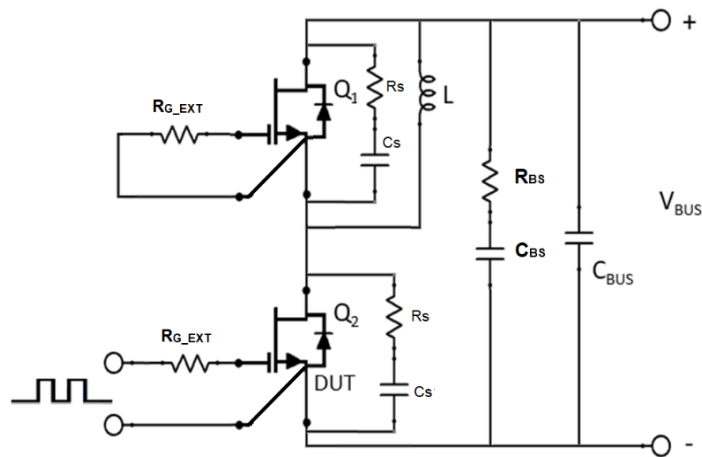
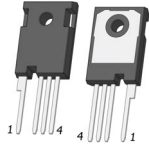


Figure 26. Schematic of the Half-Bridge Mode Switching Test Circuit. Note, a Bus RC Snubber ( $R_{BS} = 5\ \Omega$ ,  $C_{BS} = 100\text{ nF}$ ) Is Used To Reduce the Power Loop High Frequency Oscillations

### ORDERING INFORMATION

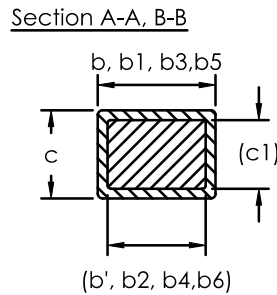
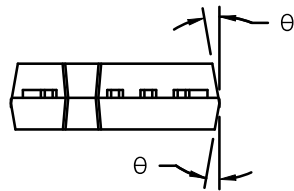
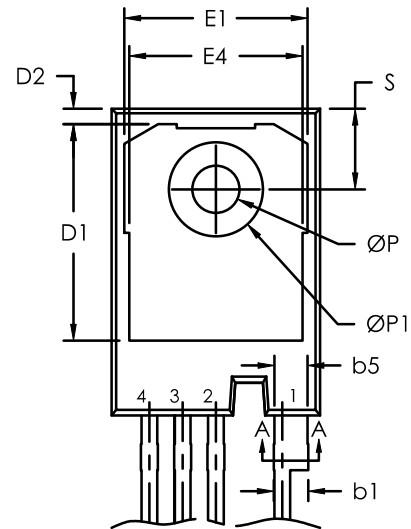
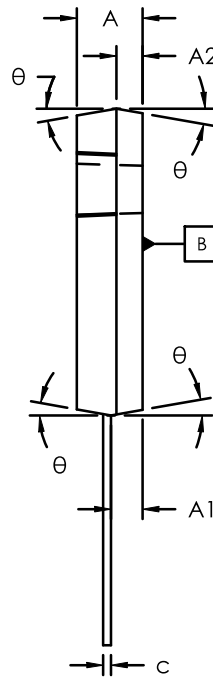
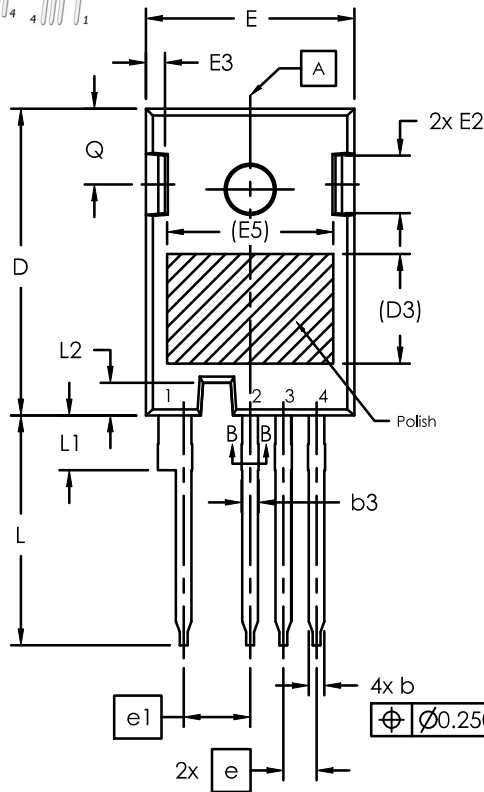
Part Number	Marking	Package	Shipping <sup>†</sup>
UF4SC120009K4SH	UF4SC120009K4SH	TO247-4LH (Pb-Free, Halogen Free)	600 / Tube

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



TO247-4LH 15.94x23.45x5.02, 2.54P  
CASE 340CV  
ISSUE B

DATE 16 APR 2025



TO247-4LH			
mm			
SYM	MIN	NOM	MAX
A	4.80	5.02	5.21
A1	2.21	2.41	2.61
A2	1.80	2.00	2.20
b	1.06	1.20	1.36
b'	1.07	1.20	1.28
b1	2.33	2.53	2.94
b3	1.07	1.20	1.60
b5	2.40	2.54	2.69
b6	2.39	2.53	2.64
c	0.51	0.60	0.75
c'	0.51	0.60	0.72
D	23.30	23.45	23.60
D1	16.25	16.55	17.65
D2	0.95	1.19	1.25
D3	8.38 REF		
E	15.74	15.94	16.14
E1	13.10	14.02	14.32
E2	3.68	4.40	5.10
E3	1.00	1.45	1.90
E4	12.38	13.26	13.43
E5	12.70 REF		
e	2.54 BSC		
e1	5.08 BSC		
L	17.27	17.57	17.87
L1	3.97	4.19	4.39
L2	2.35	2.50	2.65
ØP	3.40	3.61	3.80
ØP1	7.19 REF		
Q	5.49	5.79	6.09
S	6.04	6.17	6.30
θ	10°		

NOTE:

1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling Dimensions = Millimeters
3. Dimensions D and E does not include MOLD FLASH
4. Thermal pad contour optional within dimensions D1 and E1
5. Lead finish uncontrolled in L1
6. ØP to have a max draft angle of 1.5° to the top with MAX. hole diameter of 3.91mm

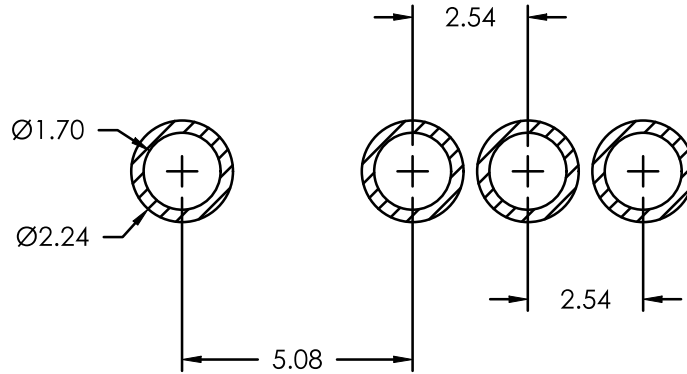
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DESCRIPTION:	TO247-4LH 15.94x23.45x5.02, 2.54P	PAGE 1 OF 2

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TO247-4LH 15.94x23.45x5.02, 2.54P  
CASE 340CV  
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RECOMMENDED PCB THROUGH HOLE



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.  
END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

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