Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, TO-263-7, 1200 V, 53 mohm

UF4C120053B7S

Description

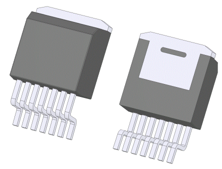
The UF4C120053B7S is a 1200 V, 53 mΩ G4 SiC FET. It is based on a unique “cascode” circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows use of off-the-shelf gate drivers hence requiring minimal re-design when replacing Si IGBTs, Si superjunction devices or SiC MOSFETs. Available in the space-saving TO-263-7 package which enables automated assembly, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- On-resistance $R_{DS(on)}$: 53 mΩ (Typ)
- Operating Temperature: 175 °C (Max)
- Excellent Reverse Recovery: Q_{rr} = 98 nC
- Low Body Diode V_{FSD}: 1.28 V
- Low Gate Charge: Q_G = 37.8 nC
- Threshold Voltage $V_{G(th)}$: 4.8 V (Typ) Allowing 0 to 15 V Drive
- Low Intrinsic Capacitance
- ESD Protected: HBM Class 2 and CDM Class C3
- TO-263-7 Package for Faster Switching, Clean Gate Waveforms
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

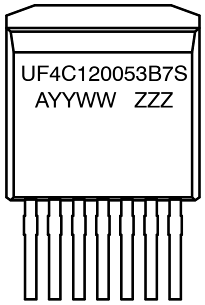
Typical Applications

- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Induction Heating



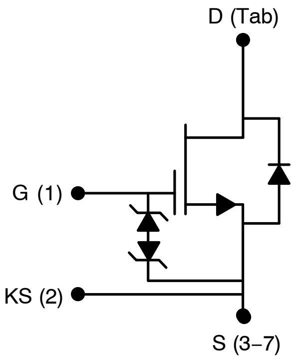
TO-263-7 10.18x9.08x4.43, 1.27P
CASE 418BA

MARKING DIAGRAM



UF4C120053B7S = Specific Device Code
A = Assembly Location
YY = Year
WW = Work Week
ZZZ = Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

April, 2025 − Rev. 2

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		1200	V
Gate-source Voltage	V_{GS}	DC	−20 to +20	V
		AC (f > 1 Hz)	−25 to +25	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25$ °C	34	A
		$T_C = 100$ °C	24.6	A
Pulsed Drain Current (Note 2)	I_{DM}	$T_C = 25$ °C	100	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	L = 15 mH, $I_{AS} = 2.7$ A	54.6	mJ
SiC FET dv/dt Ruggedness	dv/dt	$V_{DS} \leq 800$ V	150	V/ns
Power Dissipation	P_{tot}	$T_C = 25$ °C	250	W
Maximum Junction Temperature	$T_{J,\,max}$		175	°C
Operating and Storage Temperature	T_J, T_{STG}		−55 to 175	°C
Reflow Soldering Temperature	T_{solder}	Reflow MSL 1	245	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by $T_{J,\,max}$.
2. Pulse width t_p limited by $T_{J,\,max}$.
3. Starting $T_J = 25$ °C.

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		–	0.46	0.60	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = +25$ °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC						
Drain-source Breakdown Voltage	BV_{DS}	$V_{GS} = 0$ V, $I_D = 1$ mA	1200	–	–	V
Total Drain Leakage Current	I_{DSS}	$V_{DS} = 1200$ V, $V_{GS} = 0$ V, $T_J = 25$ °C	–	0.2	50	μA
		$V_{DS} = 1200$ V, $V_{GS} = 0$ V, $T_J = 175$°C	–	15	–	
Total Gate Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $T_J = 25$ °C, $V_{GS} = -20$ V / +20 V	–	6	20	μA
Drain-source On-resistance	$R_{DS(on)}$	$V_{GS} = 12$ V, $I_D = 20$ A, $T_J = 25$°C	–	53	67	mΩ
		$V_{GS} = 12$ V, $I_D = 20$ A, $T_J = 125$°C	–	112	–	
		$V_{GS} = 12$ V, $I_D = 20$ A, $T_J = 175$°C	–	159	–	
Gate Threshold Voltage	$V_{G(th)}$	$V_{DS} = 5$ V, $I_D = 10$ mA	4	4.8	6	V
Gate Resistance	R_G	f = 1 MHz, open drain	–	4.5	–	Ω
TYPICAL PERFORMANCE – REVERSE DIODE						
Diode Continuous Forward Current (Note 1)	I_S	$T_C = 25$ °C	–	–	34	A
Diode Pulse Current (Note 2)	$I_{S,\,pulse}$	$T_C = 25$ °C	–	–	100	A
Forward Voltage	V_{FSD}	$V_{GS} = 0$ V, $I_S = 10$ A, $T_J = 25$ °C	–	1.28	1.65	V
		$V_{GS} = 0$ V, $I_S = 10$ A, $T_J = 175$ °C	–	1.96	–	
Reverse Recovery Charge	Q_{rr}	$V_{DS} = 800$ V, $I_S = 25$ A, $V_{GS} = -5$ V, $R_G = 20$ Ω, di/dt = 1600 A/μs, $T_J = 25$ °C	–	98	–	nC
Reverse Recovery Time	t_{rr}		–	15.2	–	ns

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – REVERSE DIODE						
Reverse Recovery Charge	Q_{rr}	V_{DS} = 800 V, I_S = 25 A, V_{GS} = –5 V, R_G = 20 Ω, di/dt = 1600 A/μs, T_J = 150 °C	–	105	–	nC
Reverse Recovery Time	t_{rr}		–	19.6	–	ns
TYPICAL PERFORMANCE – DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz	–	1370	–	pF
Output Capacitance	C_{oss}		–	43.5	–	
Reverse Transfer Capacitance	C_{rss}		–	2.2	–	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	V_{DS} = 0 V to 800 V, V_{GS} = 0 V	–	54	–	pF
Effective Output Capacitance, Time Related	$C_{oss(tr)}$		–	100	–	
C_{OSS} Stored Energy	E_{oss}	V_{DS} = 800 V, V_{GS} = 0 V	–	17.3	–	μJ
Total Gate Charge	Q_G	V_{DS} = 800 V, I_D = 25 A, V_{GS} = 0 V to 15 V	–	37.8	–	nC
Gate-drain Charge	Q_{GD}		–	9.5	–	
Gate-source Charge	Q_{GS}		–	10	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 800 V, I_D = 25 A, Gate Driver = –5 V to +15 V, R_{G_ON} = 1 Ω, R_{G_OFF} = 20 Ω, Inductive Load, FWD: Same Device with V_{GS} = –5 V and R_G = 20 Ω, Snubber: R_S = 20 Ω, C_S = 100 pF, T_J = 25 °C (Note 4), (Note 5)	–	20	–	ns
Rise Time	t_r		–	32	–	
Turn-off Delay Time	$t_{d(off)}$		–	57	–	
Fall Time	t_f		–	12	–	
Turn-on Energy Including R_S Energy	E_{ON}		–	570	–	μJ
Turn-off Energy Including R_S Energy	E_{OFF}		–	57	–	
Total Switching Energy	E_{TOTAL}		–	627	–	
Snubber R_S Energy During Turn-on	E_{RS_ON}		–	5	–	
Snubber R_S Energy During Turn-off	E_{RS_OFF}		–	11	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 800 V, I_D = 25 A, Gate Driver = –5 V to +15 V, R_{G_ON} = 1 Ω, R_{G_OFF} = 20 Ω, Inductive Load, FWD: Same Device with V_{GS} = –5 V and R_G = 20 Ω, Snubber: R_S = 20 Ω, C_S = 100 pF, T_J = 150 °C (Note 4), (Note 5)	–	24	–	ns
Rise Time	t_r		–	33	–	
Turn-off Delay Time	$t_{d(off)}$		–	63	–	
Fall Time	t_f		–	13	–	
Turn-on Energy Including R_S Energy	E_{ON}		–	660	–	μJ
Turn-off Energy Including R_S Energy	E_{OFF}		–	75	–	
Total Switching Energy	E_{TOTAL}		–	735	–	
Snubber R_S Energy During Turn-on	E_{RS_ON}		–	5	–	
Snubber R_S Energy During Turn-off	E_{RS_OFF}		–	12	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Measured with the switching test circuit in Figure 26.
5. In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.

TYPICAL PERFORMANCE DIAGRAMS

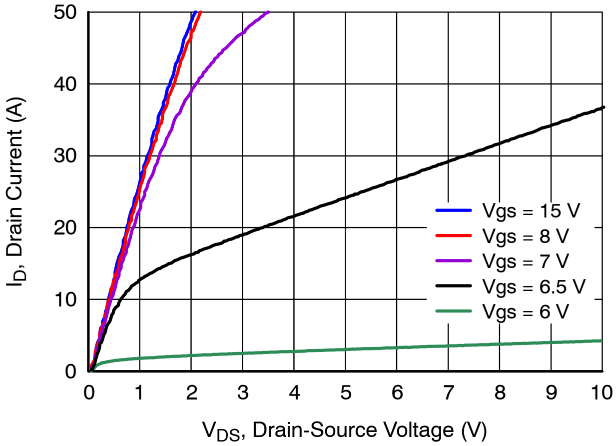


Figure 1. Typical Output Characteristics at T_J = –55 °C, t_p < 250 μs

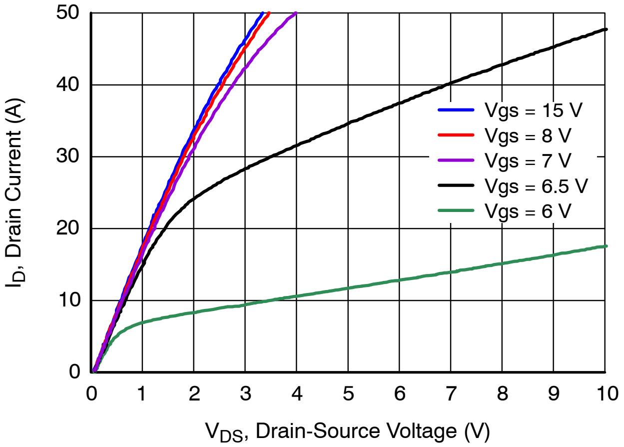


Figure 2. Typical Output Characteristics at T_J = 25 °C, t_p < 250 μs

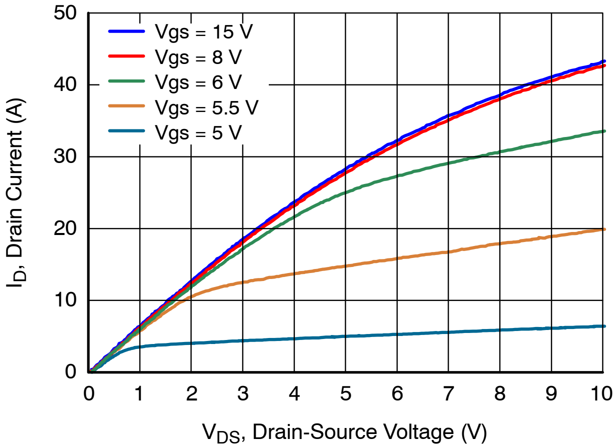


Figure 3. Typical Output Characteristics at T_J = 175 °C, t_p < 250 μs

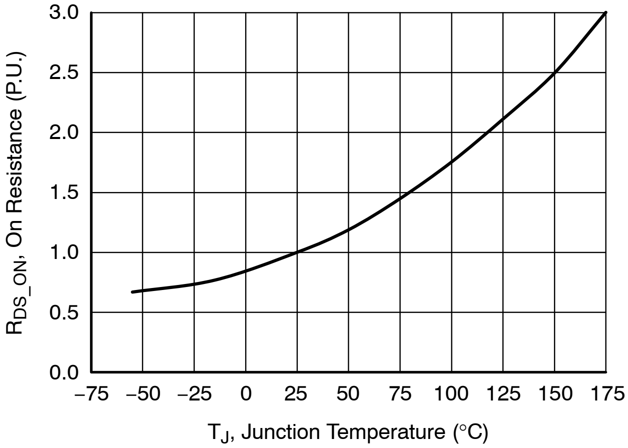


Figure 4. Normalized On-Resistance vs. Temperature at V_{GS} = 12 V and I_D = 25 A

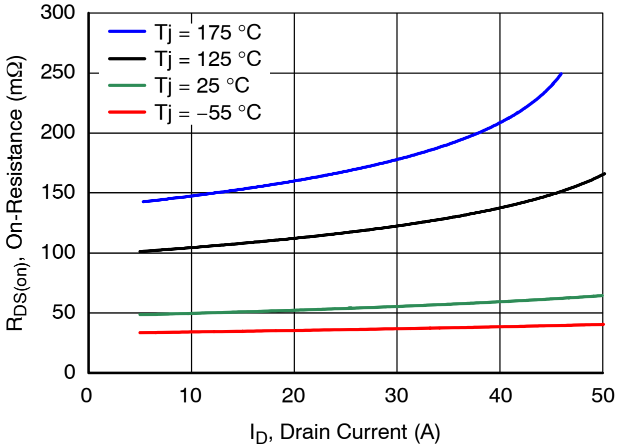


Figure 5. Typical Drain-Source On-Resistances at V_{GS} = 12 V

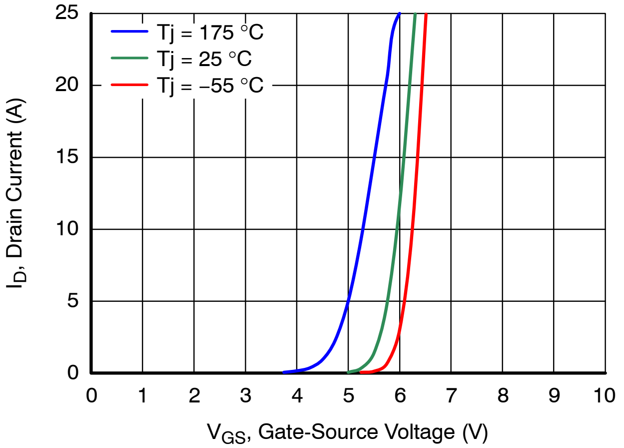


Figure 6. Typical Transfer Characteristics at V_{DS} = 5 V

TYPICAL PERFORMANCE DIAGRAMS (continued)

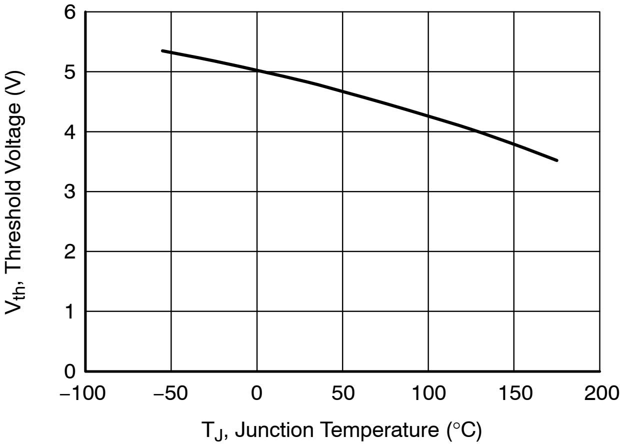


Figure 7. Threshold Voltage vs. Junction Temperature at V_{DS} = 5 V and I_D = 10 mA

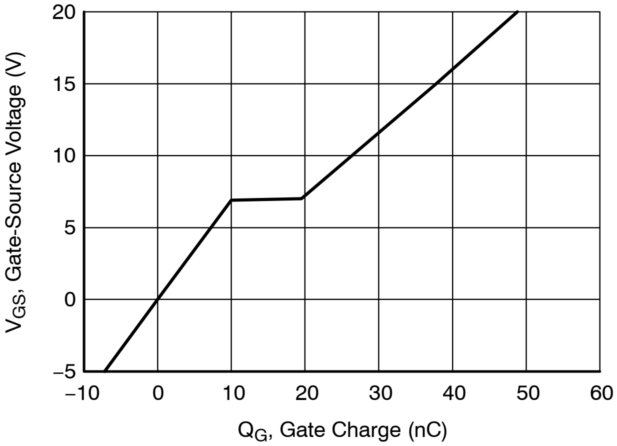


Figure 8. Typical Gate Charge at V_{DS} = 800 V and I_D = 25 A

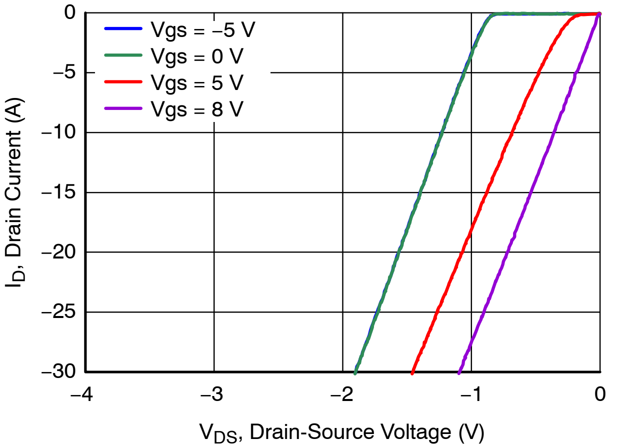


Figure 9. 3rd Quadrant Characteristics at T_J = −55 °C

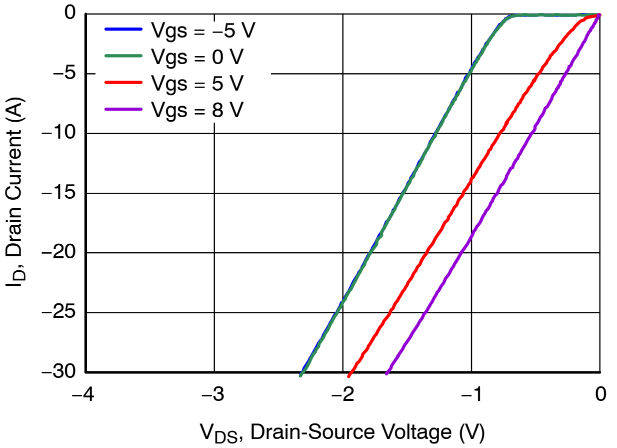


Figure 10. 3rd Quadrant Characteristics at T_J = 25 °C

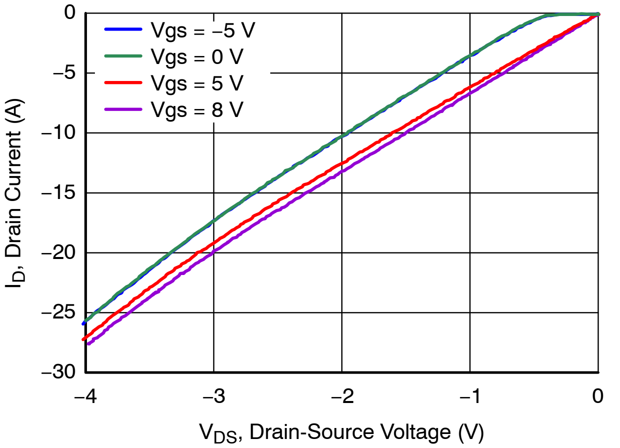


Figure 11. 3rd Quadrant Characteristics at T_J = 175 °C

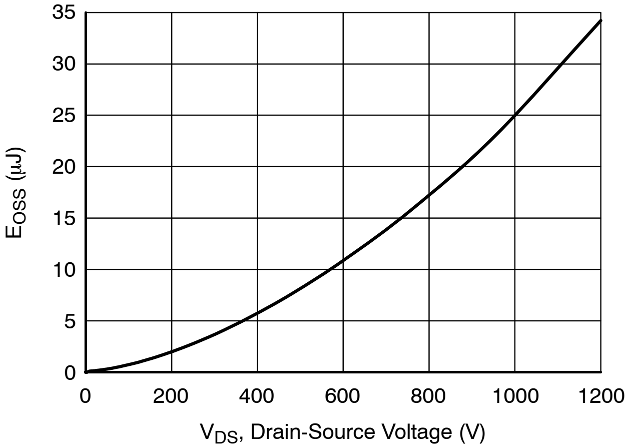


Figure 12. Typical Stored Energy in C_{OSS} at V_{GS} = 0 V

TYPICAL PERFORMANCE DIAGRAMS (continued)

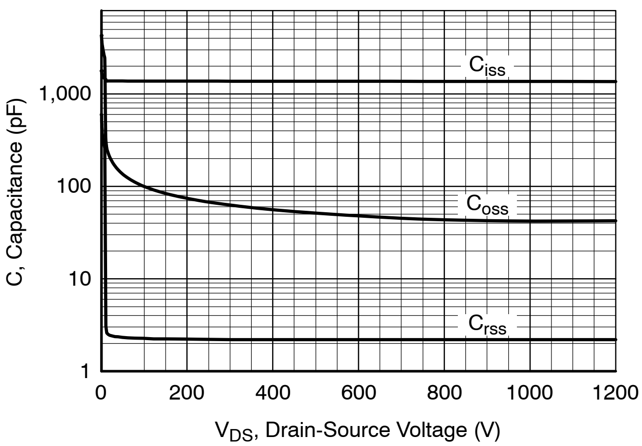


Figure 13. Typical Capacitances at f = 100 kHz and V_{GS} = 0 V

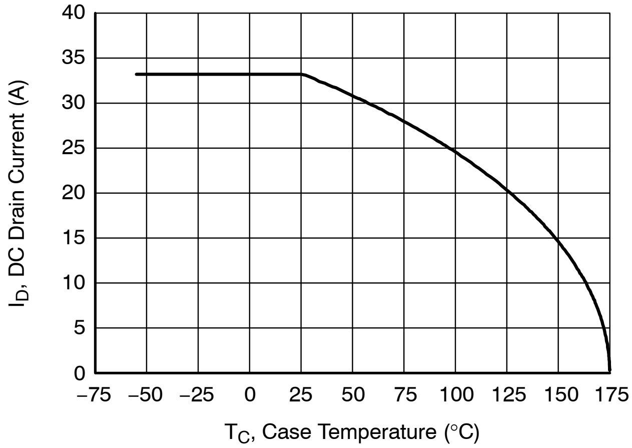


Figure 14. DC Drain Current Derating

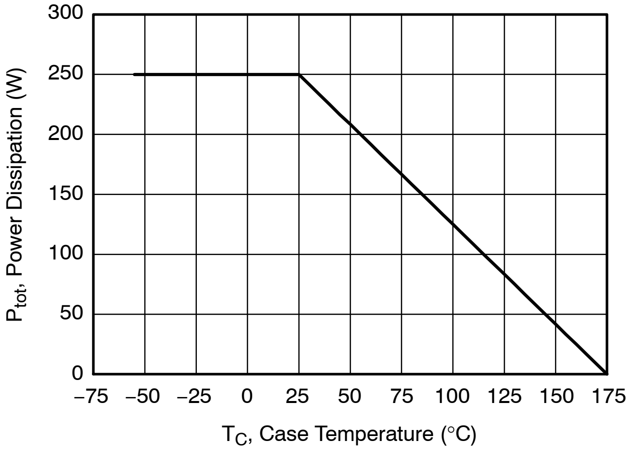


Figure 15. Total Power Dissipation

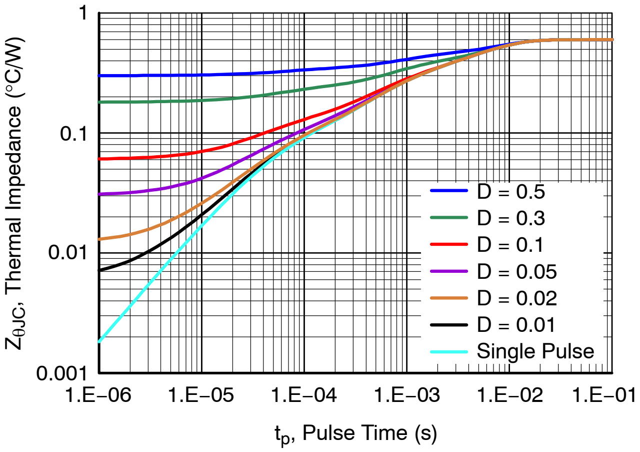


Figure 16. Maximum Transient Thermal Impedance

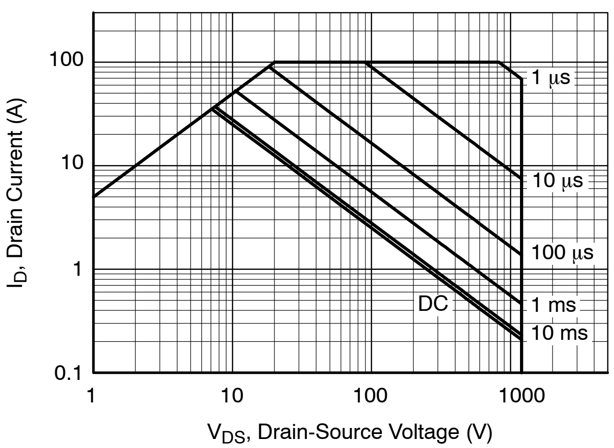


Figure 17. Safe Operation Area at T_C = 25 °C, D = 0, Parameter t_p

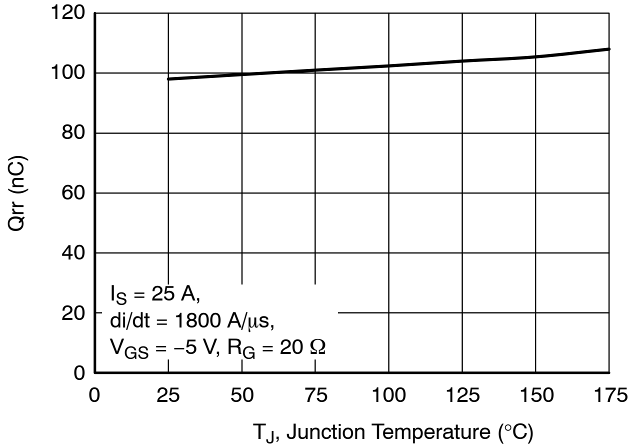


Figure 18. Reverse Recovery Charge Q_{rr} vs. Junction Temperature at V_{DS} = 800 V

TYPICAL PERFORMANCE DIAGRAMS (continued)

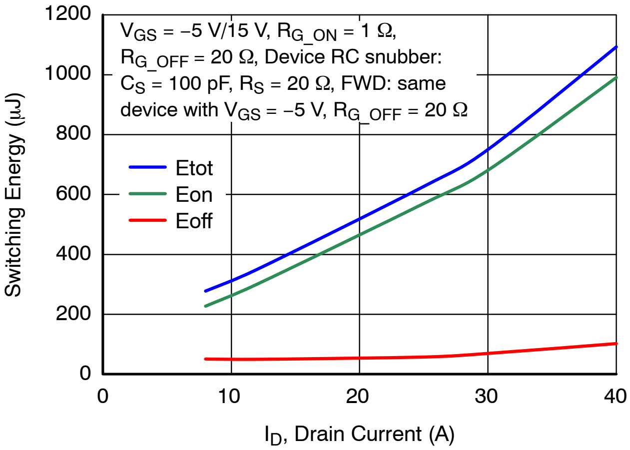


Figure 19. Clamped Inductive Switching Energy vs. Drain Current at V_{DS} = 800 V and T_J = 25 °C

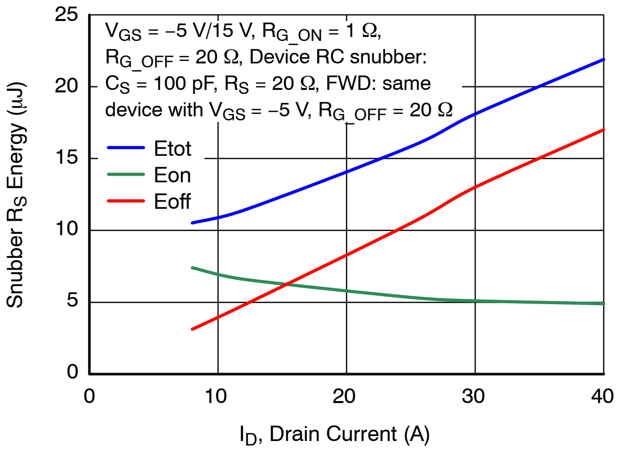


Figure 20. RC Snubber Energy Loss vs. $R_{G,EXT}$ at V_{DS} = 800 V, I_D = 25 A, and T_J = 25 °C

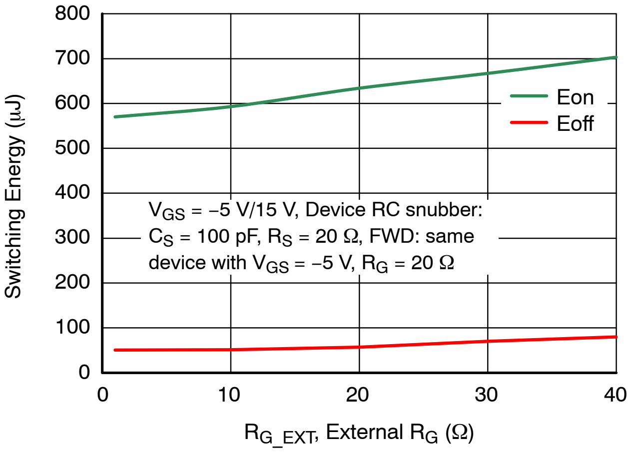


Figure 21. Clamped Inductive Switching Energies vs. $R_{G,EXT}$ at V_{DS} = 800 V, I_D = 25 A, and T_J = 25 °C

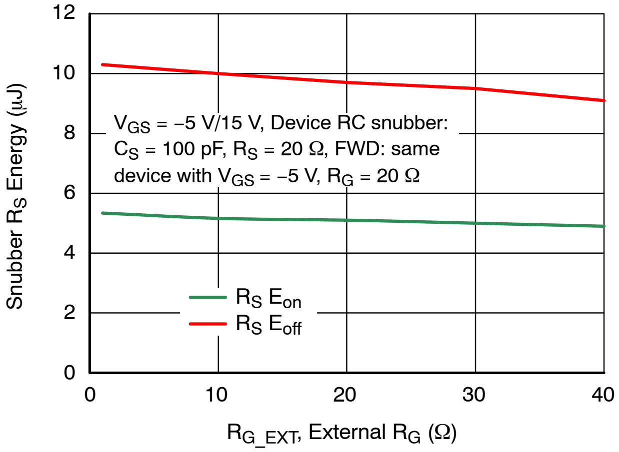


Figure 22. RC Snubber Energy Loss vs. $R_{G,EXT}$ at V_{DS} = 800 V, I_D = 25 A, and T_J = 25 °C

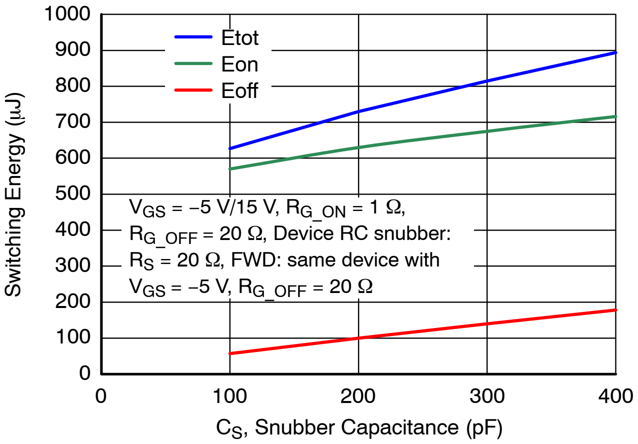


Figure 23. Clamped Inductive Switching Energies vs. Snubber Capacitance C_S at V_{DS} = 800 V I_D = 25 A, and T_J = 25 °C

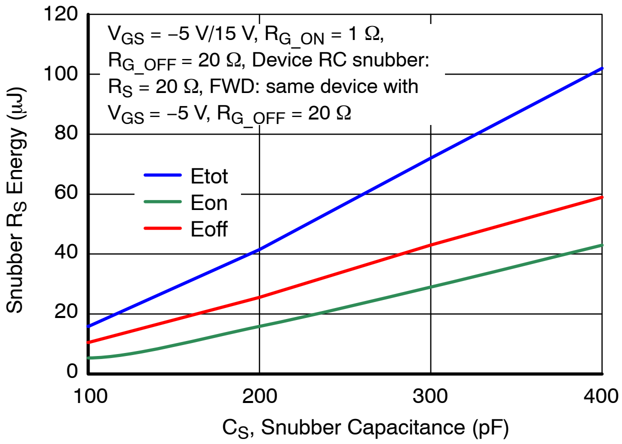


Figure 24. RC Snubber Energy Losses vs. Snubber Capacitance C_S at V_{DS} = 800 V, I_D = 25 A, and T_J = 25 °C

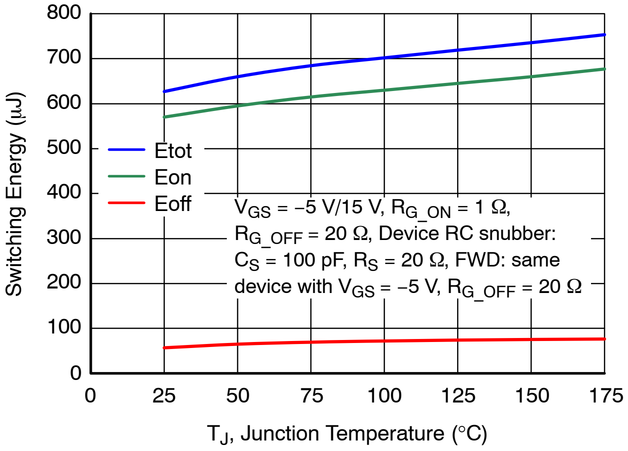


Figure 25. Clamped Inductive Switching Energy vs. Junction Temperature at V_{DS} = 800 V and I_D = 25 A

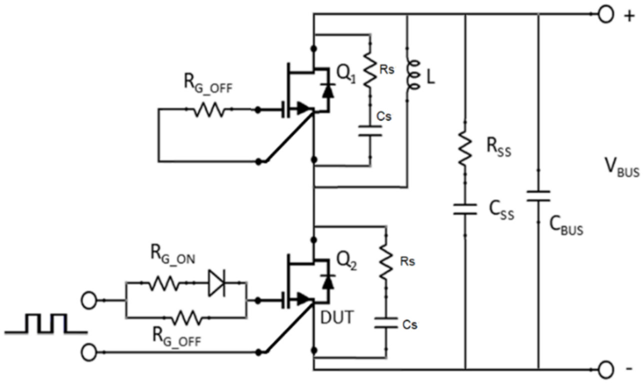


Figure 26. Schematic of the Half-bridge Mode Switching Test Circuit with Device R_C Snubbers (R_S =20 Ω, C_S = 100 pF) and a Bus RC Snubber (R_{SS} = 2.5 Ω, C_{SS}=100 nF)

APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.onsemi.com.

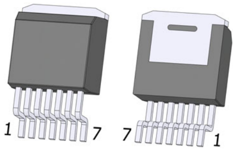
A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the **onsemi** website at www.onsemi.com

ORDERING INFORMATION

Part Number	Marking	Package	Shipping†
UF4C120053B7S	UF4C120053B7S	TO-263-7	800 / Tape & Reel

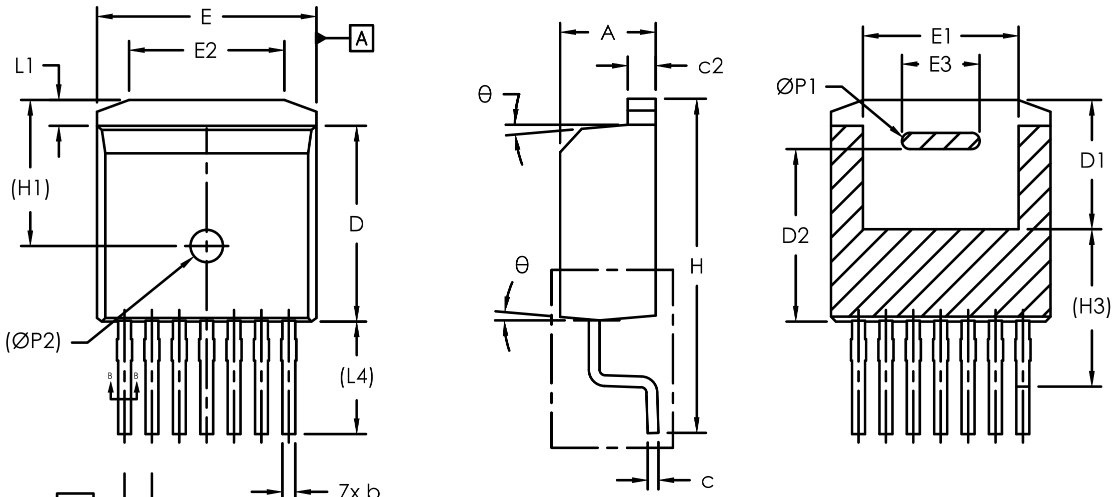
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

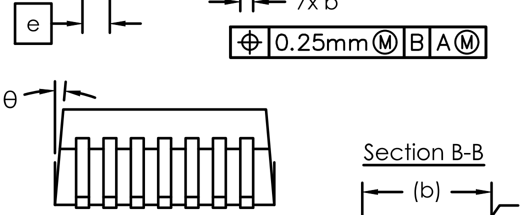
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

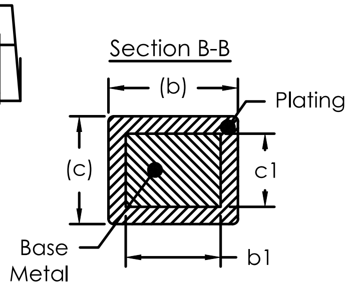


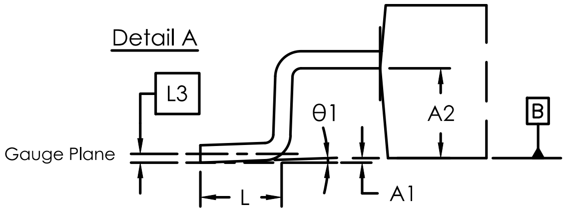
TO−263−7 10.18x9.08x4.43, 1.27P
CASE 418BA
ISSUE B

DATE 17 APR 2025









SYM	MILLIMETERS		
	Min	Nom	Max
A	4.30	4.43	4.56
A1	0.00	0.13	0.25
A2	2.45	2.60	2.75
b	0.50	0.60	0.70
b1	0.50	-	-
c	0.40	0.50	0.60
c1	0.40	-	-
c2	1.20	1.30	1.40
D	8.93	9.08	9.23
D1	5.85	6.00	6.15
D2	7.90	8.00	8.10
e	1.27 BSC		
E	10.08	10.18	10.28
E1	6.82	7.22	7.62
E2	6.50	7.55	8.60
E3	3.50	3.60	3.70
H	15.00	15.50	16.00
H1	6.78 REF		
H3	7.30 REF.		
L	1.90	2.20	2.50
L1	0.98	1.20	1.42
L3	0.25 BSC		
L4	5.22 REF		
ØP1	0.65	0.75	0.85
ØP2	1.50 REF		
θ	5°		
θ1	3°		

Notes:
1. Dimensioning and Tolerancing as per ASME Y14.5M, 2018.
2. Controlling Dimension : Millimeters
3. Package body sides exclude mold flash and gate burrs.
4. Dimension L is measured on gauge plane.
5. Dimension c1 and b1 applies to base metal only.

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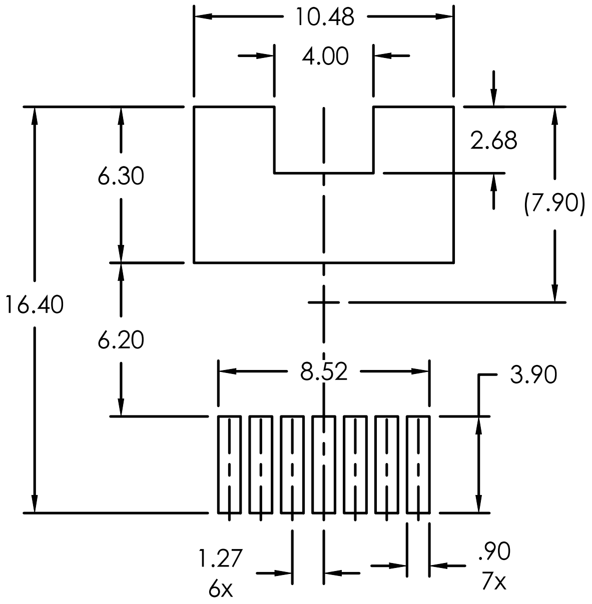
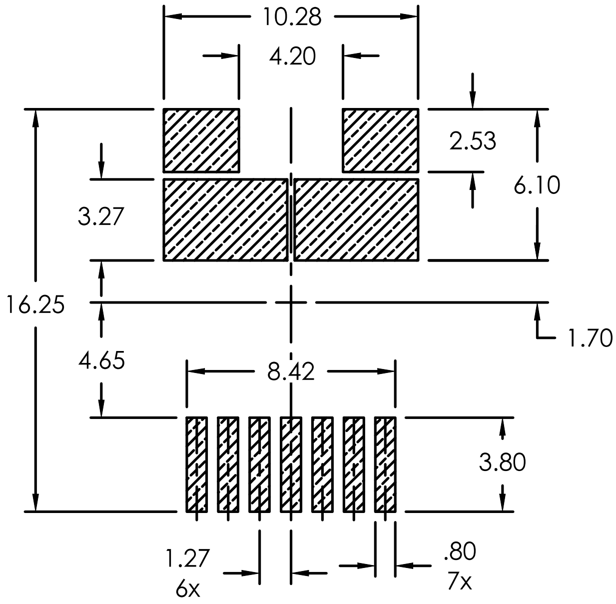
TO−263−7 10.18x9.08x4.43, 1.27P
CASE 418BA
ISSUE B

DATE 17 APR 2025

RECOMMENDED PCB FOOTPRINT

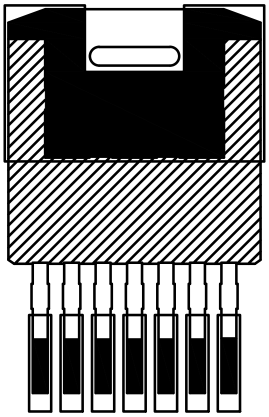


RECOMMENDED STENCIL APERTURE



NOTE: LAND PATTERN AND STENCIL APERTURE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE. END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

PCB FOOTPRINT with PACKAGE OVERLAY



■ AREA IN CONTACT WITH THE PACKAGE

▨ MOLD COMPOUND

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