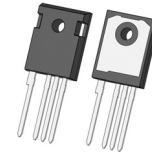


# Silicon Carbide (SiC) JFET – EliteSiC, Power N-Channel, TO247-4, 1200 V, 7.1 mohm

## UF3N120007K4S



TO247-4  
CASE 340AN

### Description

onsemi's UF3N120007K4S is a 1200 V, 7.1 mΩ High-Performance Gen 3 Normally-On SiC JFET Transistor. This device exhibits Ultra-low On resistance ( $R_{DS(ON)}$ ) in a TO247-4 Package, making it an ideal fit to address the Challenging Thermal Constraints of Solid-state Circuit Breakers and Relay Applications. Additionally, the JFET is a Robust Device Technology Capable of the High-Energy Switching Required in Circuit Protection Applications.

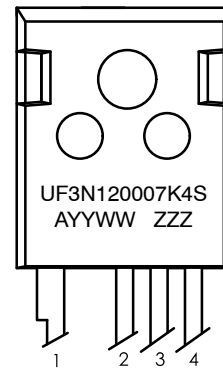
### Features

- Single Digit On-Resistance
- Operating Temperature: 175 °C (Max)
- High Pulse Current Capability
- Excellent Device Robustness
- Silver-Sintered Die Attach for Excellent Thermal Resistance
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

### Typical Applications

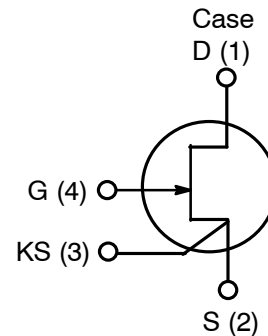
- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control
- Induction Heating

### MARKING DIAGRAM



UF3N120007K4S = Specific Device Code  
A = Assembly Location  
YY = Year  
WW = Work Week  
ZZZ = Lot ID

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# UF3N120007K4S

## MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-Source Voltage	$V_{DS}$		1200	V
Gate-Source Voltage	$V_{GS}$	DC	-30 to +3	V
		AC (Note 1)	-30 to +30	
Continuous Drain Current (Note 2)	$I_D$	$T_C < 112\text{ }^\circ\text{C}$	120	A
Pulsed Drain Current (Note 3)	$I_{DM}$	$T_C = 25\text{ }^\circ\text{C}$	550	A
Power Dissipation	$P_{TOT}$	$T_C = 25\text{ }^\circ\text{C}$	789	W
Maximum Junction Temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{STG}$		-55 to 175	$^\circ\text{C}$
Max. Lead Temperature for Soldering, 1/8" from Case for 5 seconds	$T_L$		250	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- +30 V AC Rating Applies for Turn-on Pulses <200 ns applied with external  $R_G > 1\Omega$ .
- Limited by Bondwires
- Pulse width  $t_p$  limited by  $T_{J,max}$

## THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Value			
			Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		-	0.15	0.19	$^\circ\text{C/W}$

# UF3N120007K4S

## ELECTRICAL CHARACTERISTICS ( $T_J = +25\text{ }^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>TYPICAL PERFORMANCE – STATIC</b>						
Drain-Source Breakdown Voltage	$BV_{DS}$	$V_{GS} = -20\text{ V}, I_D = 1\text{ mA}$	1200	–	–	V
Total Drain Leakage Current	$I_{DSS}$	$V_{DS} = 1200\text{ V}, V_{GS} = -20\text{ V}, T_J = 25\text{ }^\circ\text{C}$	–	20	300	$\mu\text{A}$
		$V_{DS} = 1200\text{ V}, V_{GS} = -20\text{ V}, T_J = 175\text{ }^\circ\text{C}$	–	100	–	
Total Gate Leakage Current	$I_{GSS}$	$V_{GS} = -20\text{ V}, T_J = 25\text{ }^\circ\text{C}$	–	15	300	$\mu\text{A}$
		$V_{GS} = -20\text{ V}, T_J = 175\text{ }^\circ\text{C}$	–	55	–	$\mu\text{A}$
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 2\text{ V}, I_D = 100\text{ A}, T_J = 25\text{ }^\circ\text{C}$	–	7.1	–	$\text{m}\Omega$
		$V_{GS} = 0\text{ V}, I_D = 100\text{ A}, T_J = 25\text{ }^\circ\text{C}$	–	8.6	11	
		$V_{GS} = 2\text{ V}, I_D = 100\text{ A}, T_J = 175\text{ }^\circ\text{C}$	–	15.5	–	
		$V_{GS} = 0\text{ V}, I_D = 100\text{ A}, T_J = 175\text{ }^\circ\text{C}$	–	17.8	–	
Gate Threshold Voltage	$V_{G(th)}$	$V_{DS} = 5\text{ V}, I_D = 320\text{ mA}$	–9.3	–7	–4.7	V
Gate Resistance	$R_G$	$f = 1\text{ MHz}, \text{Open Drain}$	–	0.54	–	$\Omega$

## TYPICAL PERFORMANCE – DYNAMIC

Input Capacitance	$C_{iss}$	$V_{DS} = 800\text{ V}, V_{GS} = -20\text{ V}, f = 100\text{ kHz}$	–	8110	–	$\text{pF}$
Output Capacitance	$C_{oss}$		–	368	–	
Reverse Transfer Capacitance	$C_{rss}$		–	358	–	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	$V_{DS} = 0\text{ V to } 800\text{ V}, V_{GS} = -20\text{ V}$	–	403	–	$\text{pF}$
$C_{OSS}$ Stored Energy	$E_{OSS}$	$V_{DS} = 800\text{ V}, V_{GS} = -20\text{ V}$	–	130	–	$\mu\text{J}$
Total Gate Charge	$Q_G$	$V_{DS} = 800\text{ V}, I_D = 100\text{ A}, V_{GS} = -18\text{ V to } 0\text{ V}$	–	830	–	$\text{nC}$
Gate-Drain Charge	$Q_{GD}$		–	520	–	
Gate-Source Charge	$Q_{GS}$		–	120	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE DIAGRAM

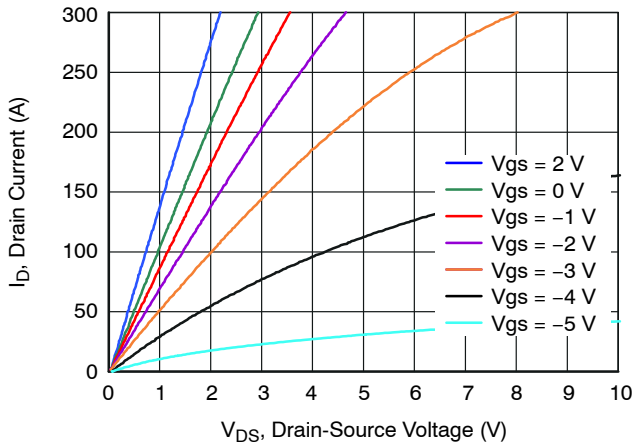


Figure 1. Typical Output Characteristics at  $T_J = -55\text{ }^\circ\text{C}$ ,  $t_p < 250\text{ }\mu\text{s}$

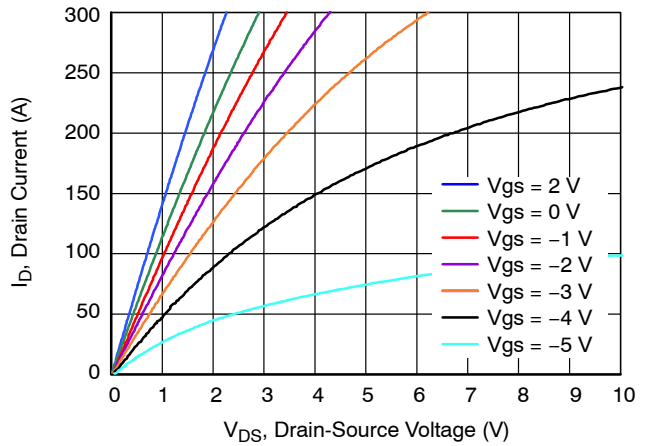


Figure 2. Typical Output Characteristics at  $T_J = 25\text{ }^\circ\text{C}$ ,  $t_p < 250\text{ }\mu\text{s}$

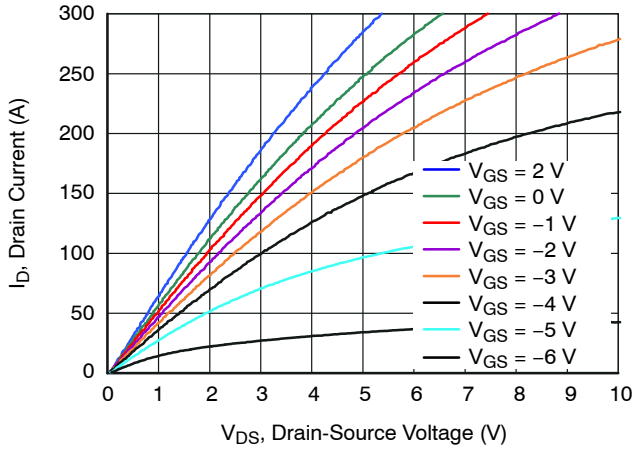


Figure 3. Typical Output Characteristics at  $T_J = 175\text{ }^\circ\text{C}$ ,  $t_p < 250\text{ }\mu\text{s}$

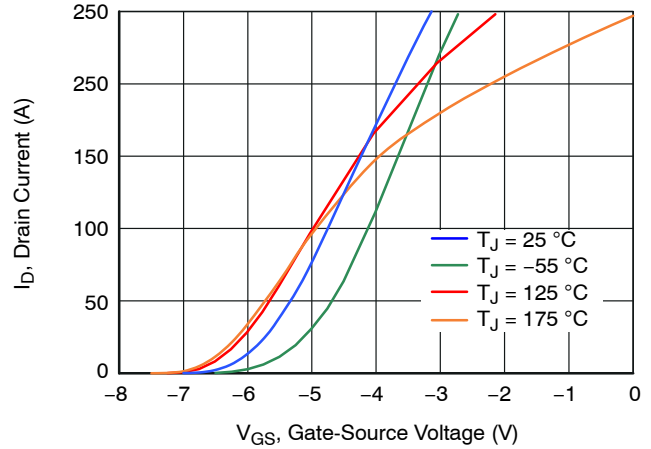


Figure 4. Typical Transfer Characteristics at  $V_{DS} = 5\text{ V}$

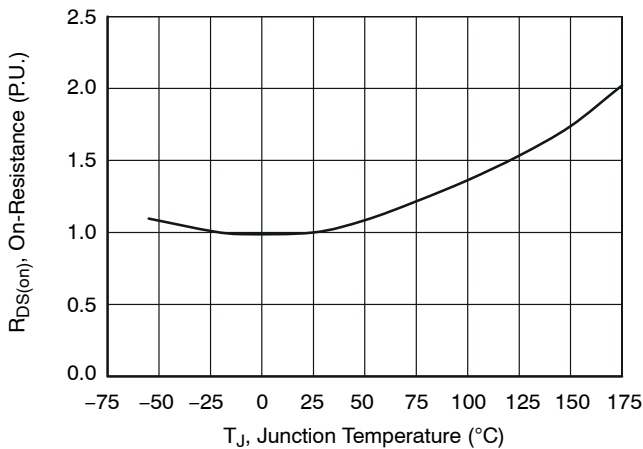


Figure 5. Normalized On-Resistance Vs. Temperature at  $V_{GS} = 0\text{ V}$  and  $I_D = 100\text{ A}$

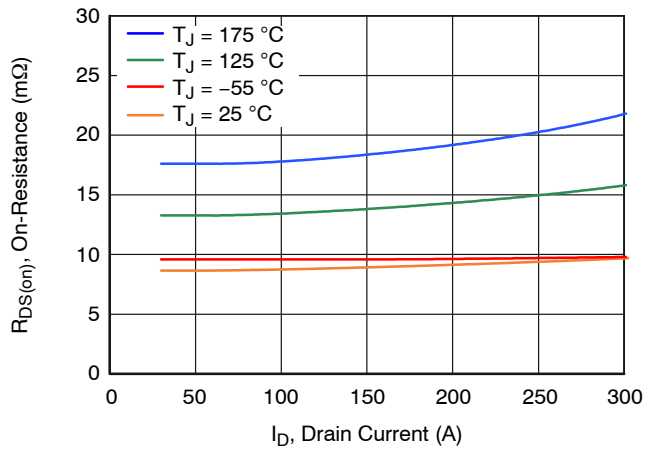


Figure 6. Typical Drain-Source On-Resistance  $V_{GS} = 0\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

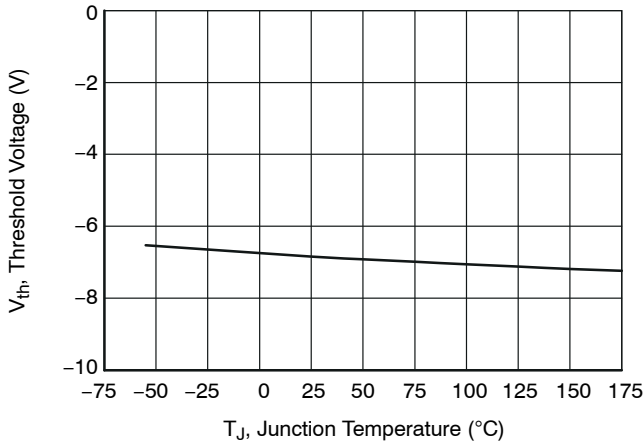


Figure 7. Threshold Voltage vs. Junction Temperature at  $V_{DS} = 5\text{ V}$  and  $I_D = 320\text{ mA}$

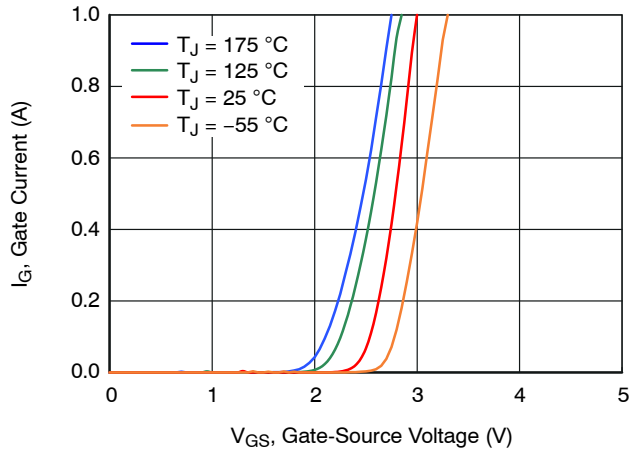


Figure 8. Typical Gate Forward Current at  $V_{DS} = 0\text{ V}$

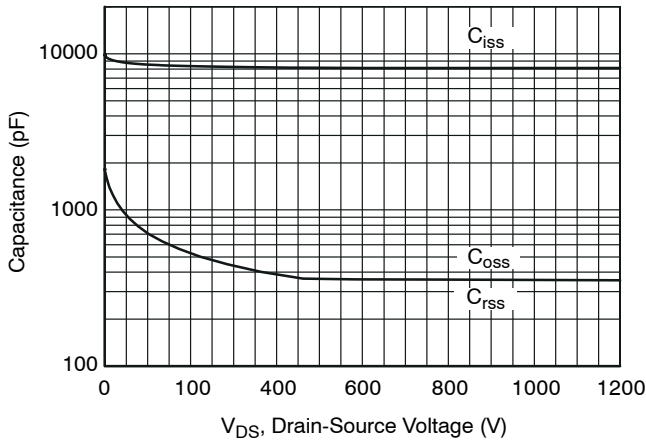


Figure 9. Typical Capacitances at  $f = 100\text{ KHz}$  and  $V_{GS} = -20\text{ V}$

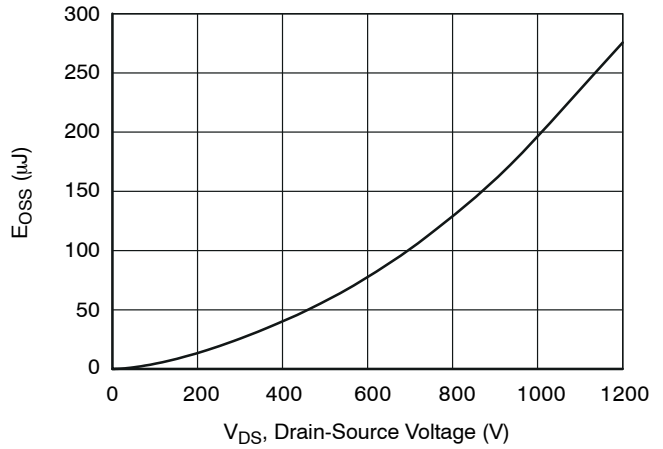


Figure 10. Typical Stored Energy in  $C_{OSS}$  at  $V_{GS} = -20\text{ V}$

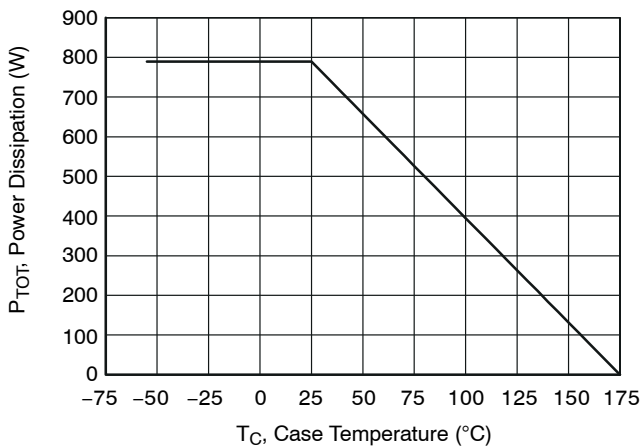


Figure 11. Total Power Dissipation

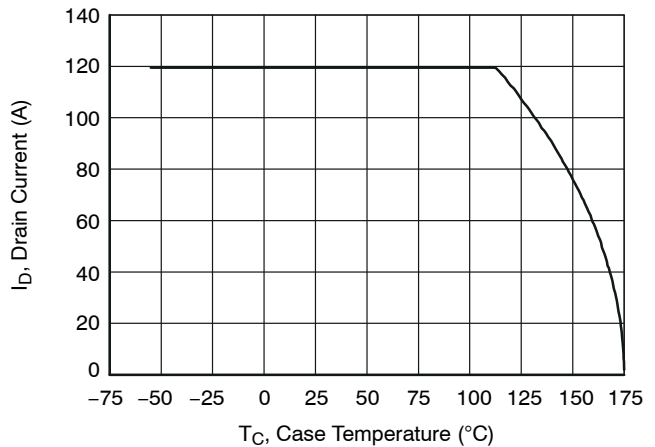
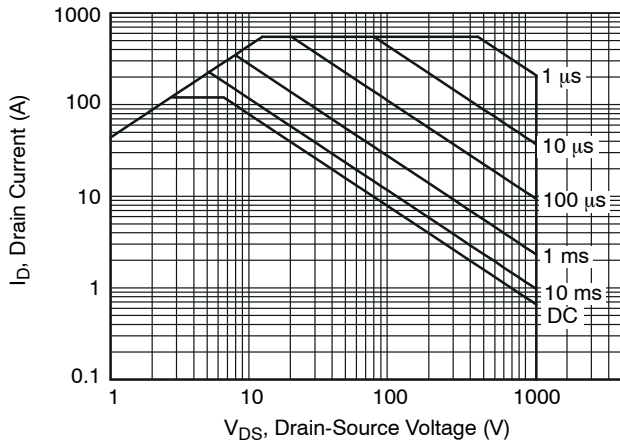


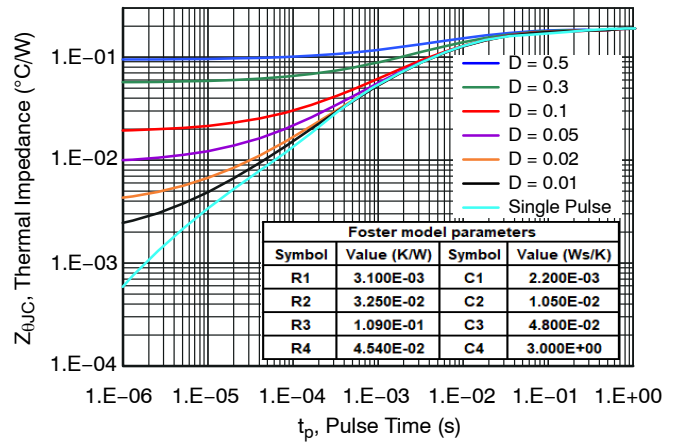
Figure 12. DC Drain Current Derating

# UF3N120007K4S

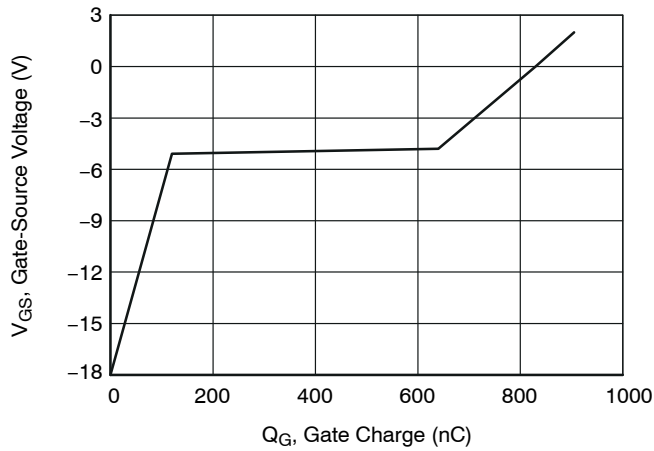
## TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)



**Figure 13. Safe Operation Area at  $T_C = 25\text{ }^\circ\text{C}$ , Parameter  $t_p$**



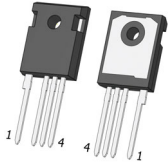
**Figure 14. Maximum Transient Thermal Impedance**



**Figure 15. Typical Gate Charge at  $V_{DS} = 800\text{ V}$  and  $I_D = 100\text{ A}$**

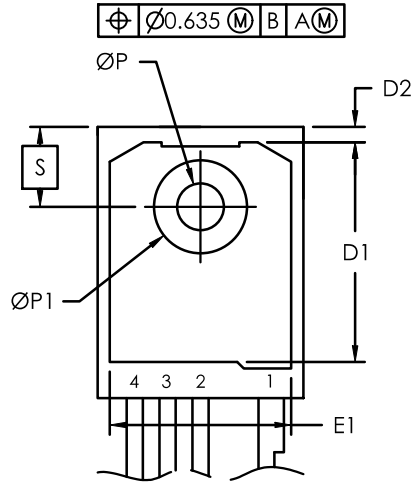
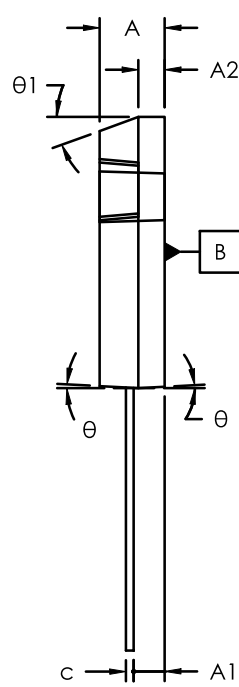
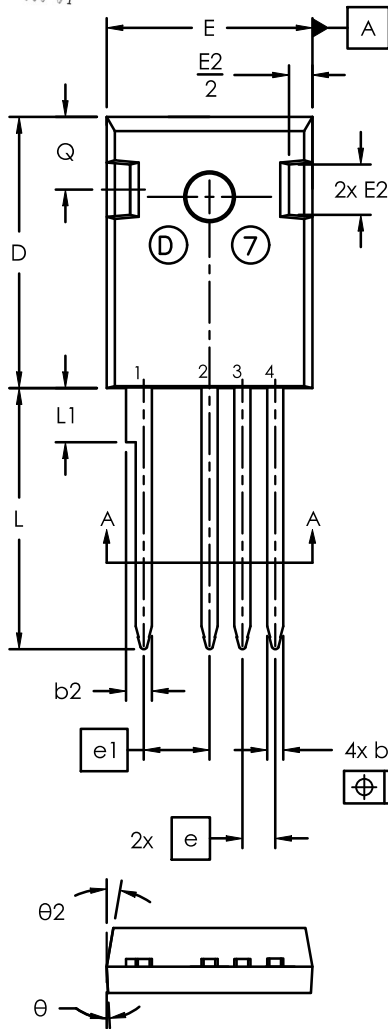
### ORDERING INFORMATION

Part Number	Marking	Package	Shipping
UF3N120007K4S	UF3N120007K4S	TO247-4 (Pb-Free, Halogen Free)	600 Units / Tube



TO247-4 15.90x20.96x5.03, 5.44P  
CASE 340AN  
ISSUE E

DATE 20 JUN 2025



$\text{Ø} \ 0.254 \text{ (M) B A (M)}$

SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
c	0.38	0.60	0.89
D	20.80	20.96	21.46
D1	13.08	—	—
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	2.54 BSC		
e1	5.08 BSC		
E1	13.46	—	—
E2	3.43	3.89	5.20
L	19.81	20.17	20.32
L1	—	—	4.50
ØP	3.40	3.60	3.80
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.17 BSC		
θ	3°		
θ1	20°		
θ2	10°		

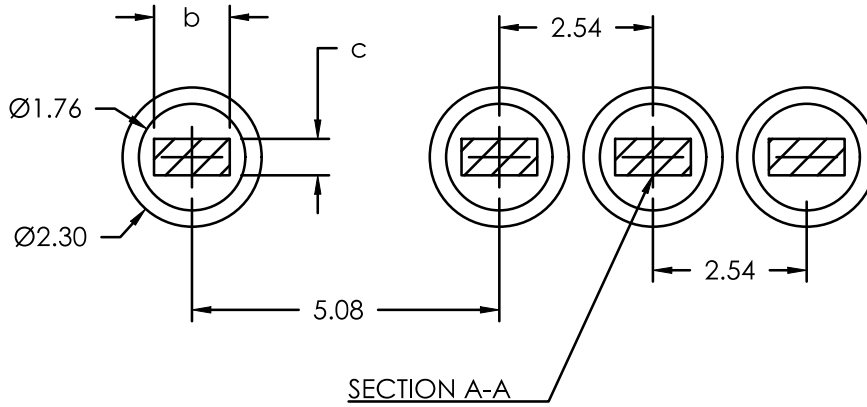
NOTE:

1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.
5. Through Hole diameter value = End Hole diameter
6. PCB Through Hole pattern as per IPC-2221/IPC-2222

<b>DOCUMENT NUMBER:</b>	<b>98AON86067F</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TO247-4 15.90x20.96x5.03, 5.44P</b>	<b>PAGE 1 OF 2</b>

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

RECOMMENDED PCB THROUGH HOLE



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.  
END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

<b>DOCUMENT NUMBER:</b>	<b>98AON86067F</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TO247-4 15.90x20.96x5.03, 5.44P</b>	<b>PAGE 2 OF 2</b>

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)