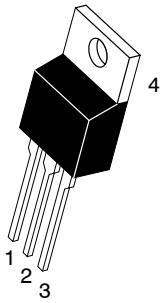
Plastic Medium-Power Complementary Silicon Transistors

TIP120, TIP121, TIP122 (NPN); TIP125, TIP126, TIP127 (PNP)

Designed for general−purpose amplifier and low−speed switching applications.



1. Base
2. Collector
3. Emitter
4. Collector

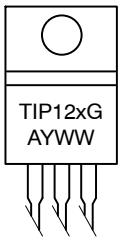
TO−220AB
CASE 221A
STYLE 1

DARLINGTON
5 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60−80−100 VOLTS, 65 WATTS

Features

- High DC Current Gain −
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector−Emitter Sustaining Voltage − @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) − TIP120, TIP125
  = 80 Vdc (Min) − TIP121, TIP126
  = 100 Vdc (Min) − TIP122, TIP127
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- Pb−Free Packages are Available*

MARKING DIAGRAM



TIP12x	= Device Code
x	= 0, 1, 2, 5, 6, or 7
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

© Semiconductor Components Industries, LLC, 2014

MAXIMUM RATINGS

Symbol	Rating	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
V_{CEO}	Collector−Emitter Voltage	60	80	100	Vdc
V_{CB}	Collector−Base Voltage	60	80	100	Vdc
V_{EB}	Emitter−Base Voltage		5.0		Vdc
I_C	Collector Current − Continuous − Peak		5.0 8.0		Adc
I_B	Base Current		120		mAdc
P_D	Total Power Dissipation @ T_C = 25°C Derate above 25°C		65 0.52		W W/°C
P_D	Total Power Dissipation @ T_A = 25°C Derate above 25°C		2.0 0.016		W W/°C
E	Unclamped Inductive Load Energy (Note 1)		50		mJ
T_J, T_{stg}	Operating and Storage Junction, Temperature Range		−65 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	1.92	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	62.5	°C/W

1. I_C = 1 A, L = 100 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Characteristic		Min	Max	Unit
OFF CHARACTERISTICS					
$V_{CEO(sus)}$	Collector−Emitter Sustaining Voltage (Note 2) (I_C = 100 mAdc, I_B = 0)	 TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	 60 80 100	 − − −	Vdc
I_{CEO}	Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	 − − −	 0.5 0.5 0.5	mAdc
I_{CBO}	Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	 TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	 − − −	 0.2 0.2 0.2	mAdc
I_{EBO}	Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		−	2.0	mAdc
ON CHARACTERISTICS (Note 2)					
h_{FE}	DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		1000 1000	− −	−
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc) (I_C = 5.0 Adc, I_B = 20 mAdc)		 − −	 2.0 4.0	Vdc
$V_{BE(on)}$	Base−Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		−	2.5	Vdc
DYNAMIC CHARACTERISTICS					
h_{fe}	Small−Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		4.0	−	−
C_{ob}	Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz	TIP125, TIP126, TIP127 TIP120, TIP121, TIP122	− −	300 200	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

Share Feedback
Your Opinion Matters

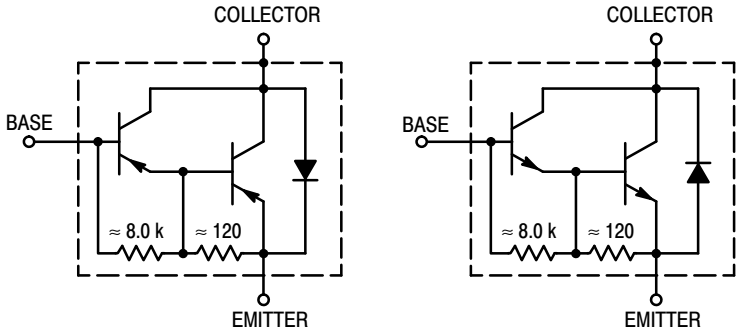


Figure 1. Darlington Circuit Schematic

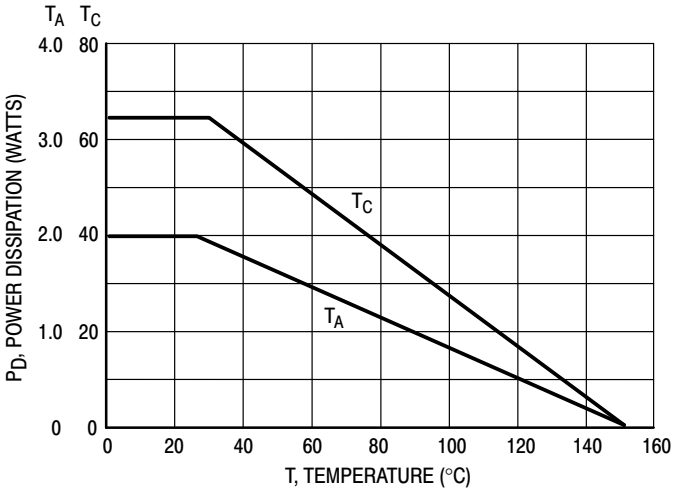


Figure 2. Power Derating

Share Feedback
Your Opinion Matters

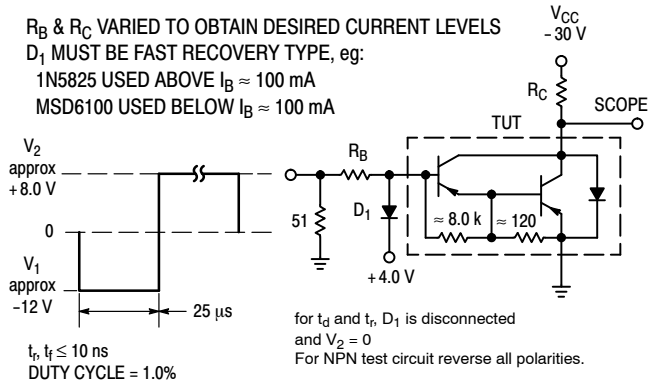


Figure 3. Switching Times Test Circuit

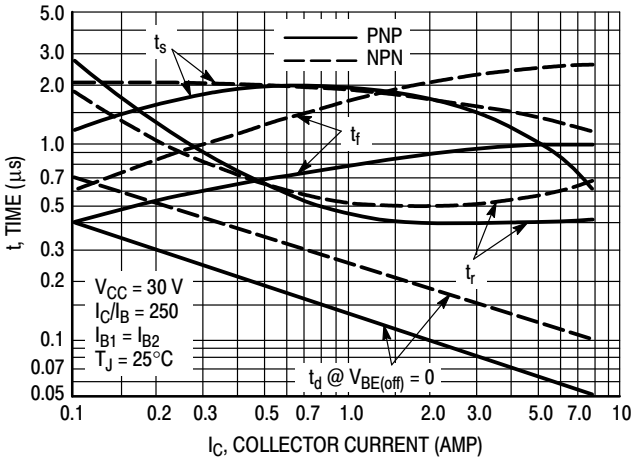


Figure 4. Switching Times

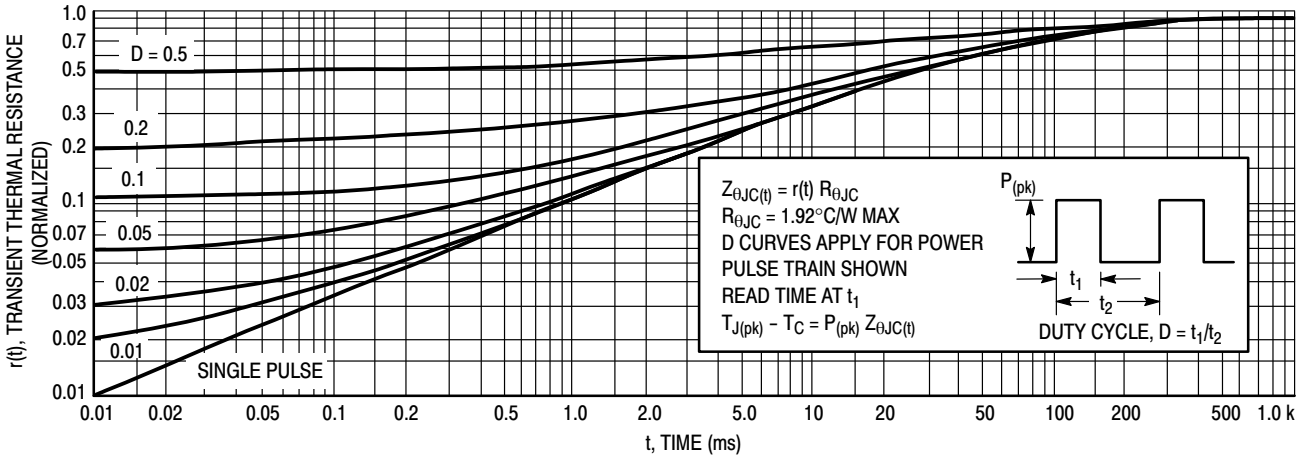


Figure 5. Thermal Response

Share Feedback
Your Opinion Matters

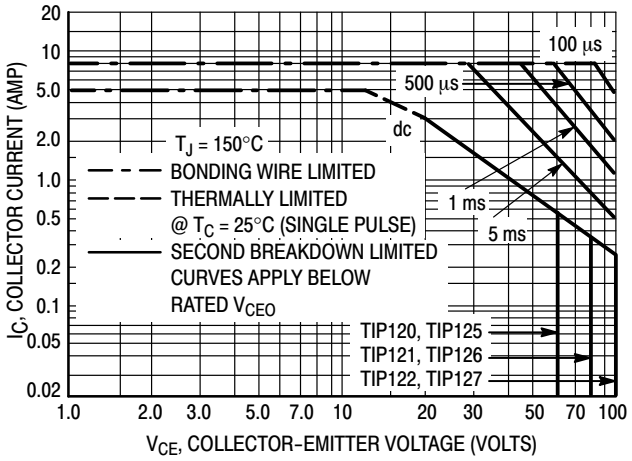


Figure 6. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

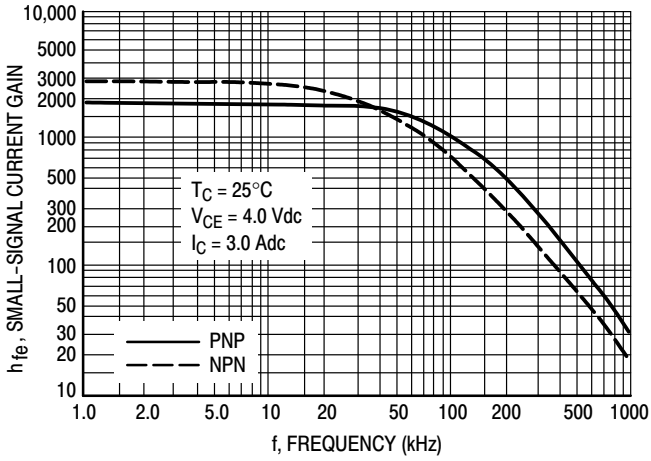


Figure 7. Small−Signal Current Gain

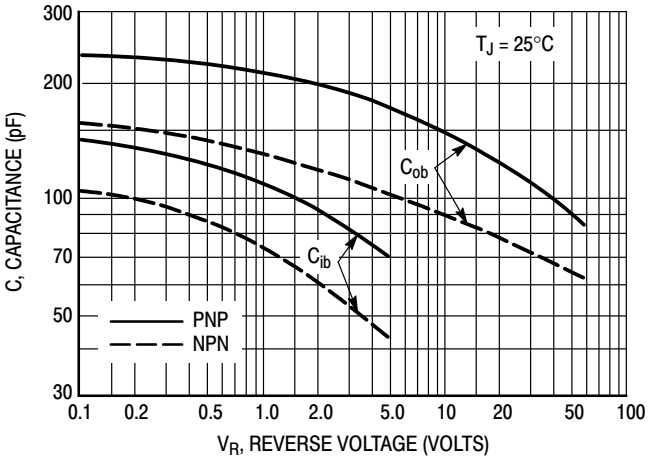
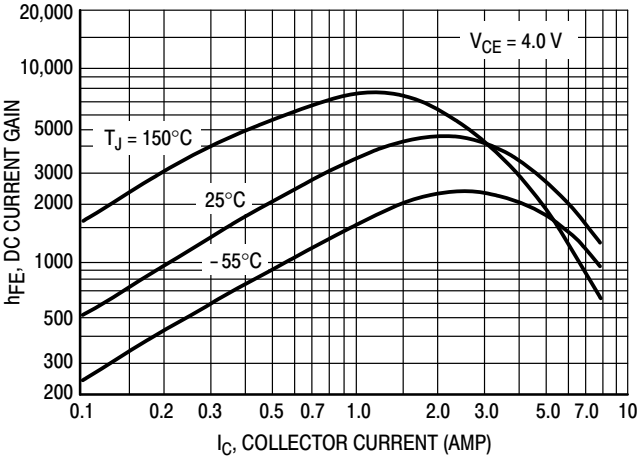


Figure 8. Capacitance

Share Feedback
Your Opinion Matters

NPN
TIP120, TIP121, TIP122



PNP
TIP125, TIP126, TIP127

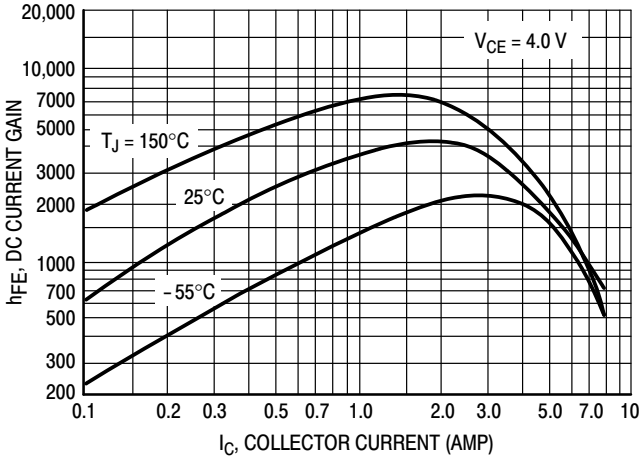
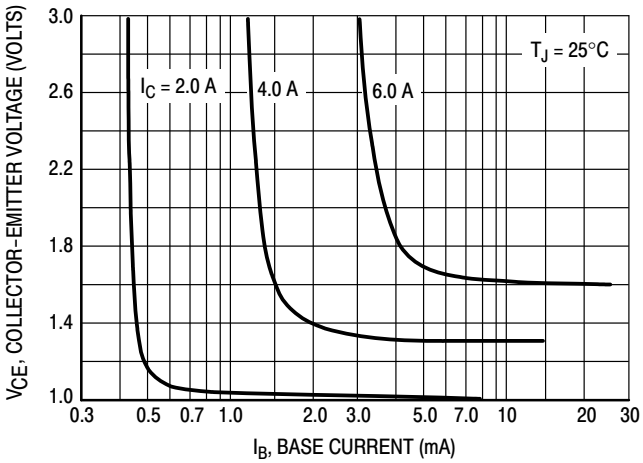


Figure 9. DC Current Gain



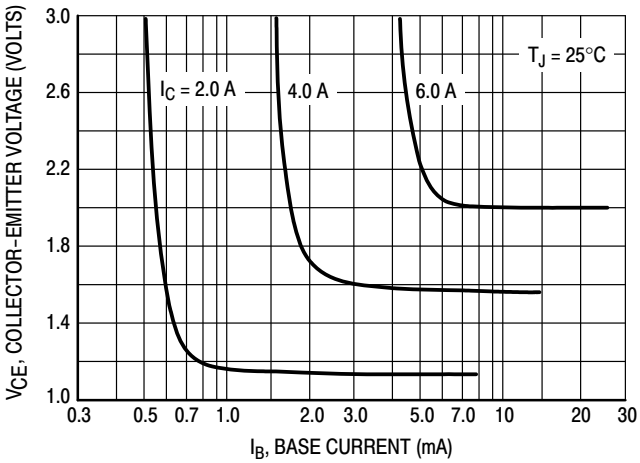
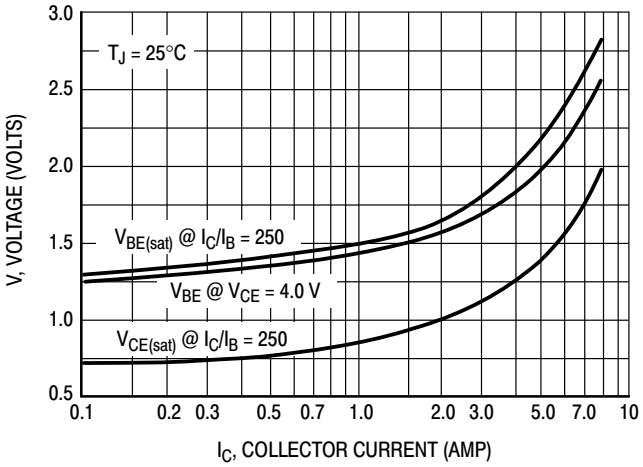


Figure 10. Collector Saturation Region



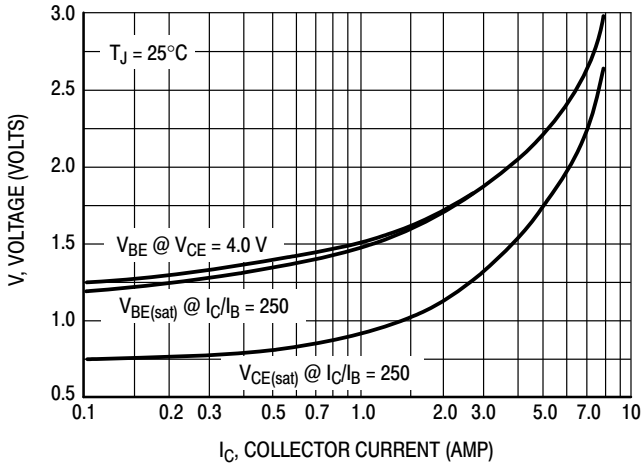


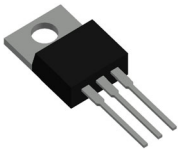
Figure 11. “On” Voltages

Share Feedback
Your Opinion Matters

ORDERING INFORMATION

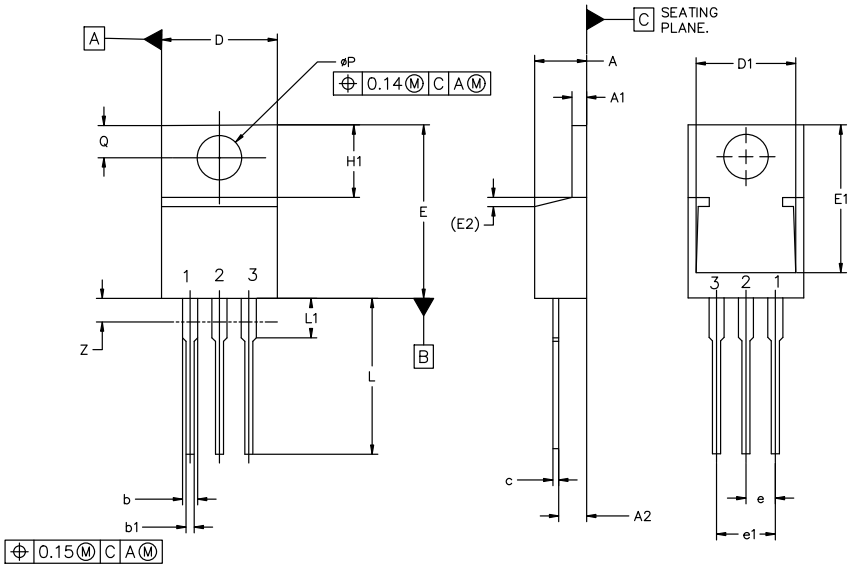
Device	Package	Shipping
TIP120	TO−220	50 Units / Rail
TIP120G	TO−220 (Pb−Free)	50 Units / Rail
TIP121	TO−220	50 Units / Rail
TIP121G	TO−220 (Pb−Free)	50 Units / Rail
TIP122	TO−220	50 Units / Rail
TIP122G	TO−220 (Pb−Free)	50 Units / Rail
TIP125	TO−220	50 Units / Rail
TIP125G	TO−220 (Pb−Free)	50 Units / Rail
TIP126	TO−220	50 Units / Rail
TIP126G	TO−220 (Pb−Free)	50 Units / Rail
TIP127	TO−220	50 Units / Rail
TIP127G	TO−220 (Pb−Free)	50 Units / Rail

Share Feedback
Your Opinion Matters



TO−220−3 10.10x15.12x4.45, 2.54P
CASE 221A
ISSUE AL

DATE 05 FEB 2025



MILLIMETERS			
DIM	MIN	NOM	MAX
A	4.07	4.45	4.83
A1	1.15	1.28	1.41
A2	2.04	2.42	2.79
b	1.15	1.34	1.52
b1	0.64	0.80	0.96
c	0.36	0.49	0.61
D	9.66	10.10	10.53
D1	8.43	8.63	8.83
E	14.48	15.12	15.75
E1	12.58	12.78	12.98
E2	1.27 REF		

MILLIMETERS			
DIM	MIN	NOM	MAX
e	2.42	2.54	2.66
e1	4.83	5.08	5.33
H1	5.97	6.22	6.47
L	12.70	13.49	14.27
L1	2.80	3.45	4.10
Q	2.54	2.79	3.04
øP	3.60	3.85	4.09
Z	–.––	–.––	3.48

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

DOCUMENT NUMBER:	**98ASB42148B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO−220−3 10.10x15.12x4.45, 2.54P**	**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, onsemi, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales