Low-Voltage Multiplexer/Demultiplexer, Bus Switch

Preliminary Document

T30LMSW3B3257 / T30LMSW3B3253 / T30LMSW3B3125 / T30LMSW3B3126

The T30LMSW3B3257 device is a 4-bit 1-of-2 highspeed FET multiplexer/demultiplexer. The select (S) input controls the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable ($\overline{OE}$) input is high.

The T30LMSW3B3253 device is a dual 1-of-4 highspeed FET multiplexer and demultiplexer. The select (S0, S1) inputs control the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable ($\overline{OE}$) input is high.

The T30LMSW3B3125 and T30LMSW3B3126 devices are quadruple FET bus switches featuring independent line switches. Each switch of the T30LMSW3B3125 is disabled when the associated output-enable ($\overline{OE}$) input is high. Each switch of the T30LMSW3B3126 is disabled when the associated output-enable (OE) input is low.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the devices when the devices are powered down. The devices have isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor while OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Features

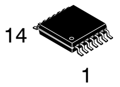
- 5 Ω Switch Connection Between 2 Ports
- Rail to Rail Switching on Data Ports
- I_{off} Supports Partial Power Down Mode Operation
- Break-Before-Make circuitry for 3257 and 3253
- 2000 V HBM ESD Protection (JESD22)

Typical Applications

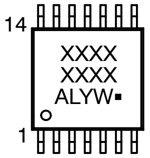
- Internet of Things
- Wireless Headphones
- Muxing/Demuxing
- Datacenters and Enterprise Computing
- Building Automation

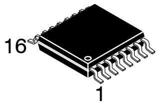
This Preliminary document is for informational purposes only. **onsemi** may update or withdraw it without notice. Content and referenced products are under development and subject to change.

MARKING DIAGRAMS

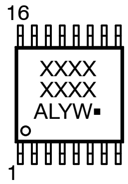


TSSOP-14
DT SUFFIX
CASE 948G





TSSOP-16
DT SUFFIX
CASE 948F



XXXXXX	= Specific Device Code
A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
▪	= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

May, 2026 – Rev. P4

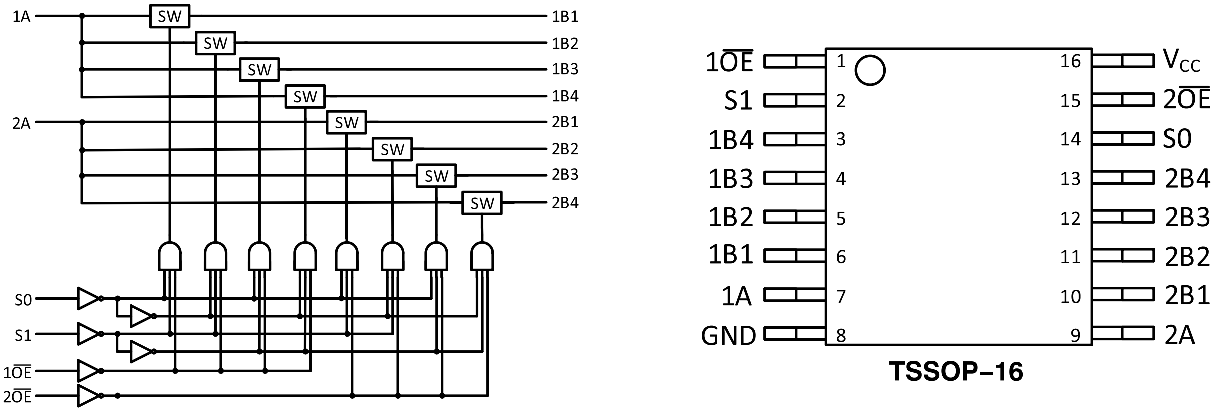


Figure 1. T30LMSW3B3253 Logic Diagram and Pin Assignment

T30LMSW3B3253 FUNCTION TABLE

Inputs			Function
OE	S1	S0	
L	L	L	A = B1
L	L	H	A = B2
L	H	L	A = B3
L	H	H	A = B4
H	X	X	Disconnect

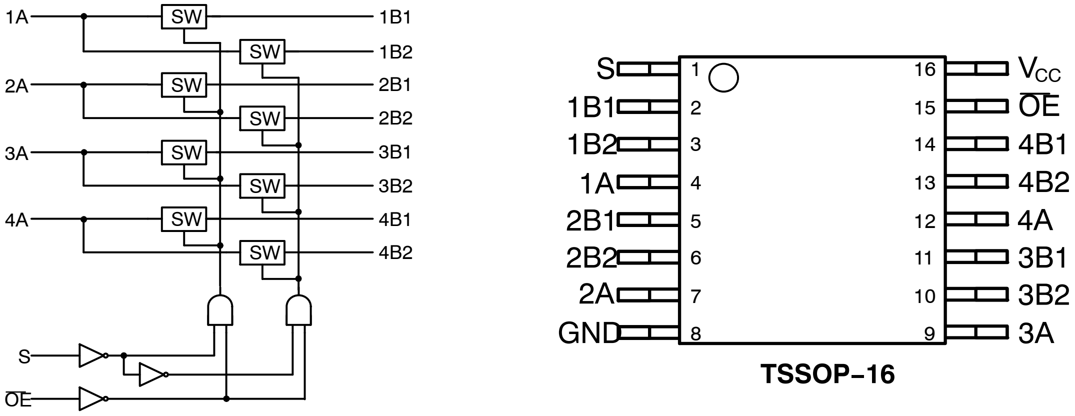


Figure 2. T30LMSW3B3257 Logic Diagram and Pin Assignment

T30LMSW3B3257 FUNCTION TABLE

Inputs		Function
OE	S	
L	L	A = B1
L	H	A = B2
H	X	Disconnect

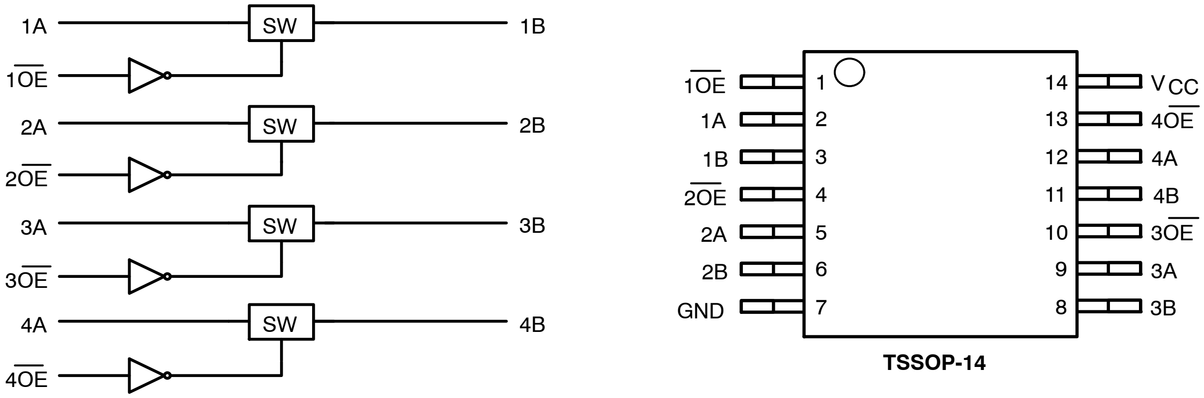


Figure 3. T30LMSW3B3125 Logic Diagram and Pin Assignment

T30LMSW3B3125 FUNCTION TABLE

$\overline{OE}$	Function
L	A = B
H	Disconnect

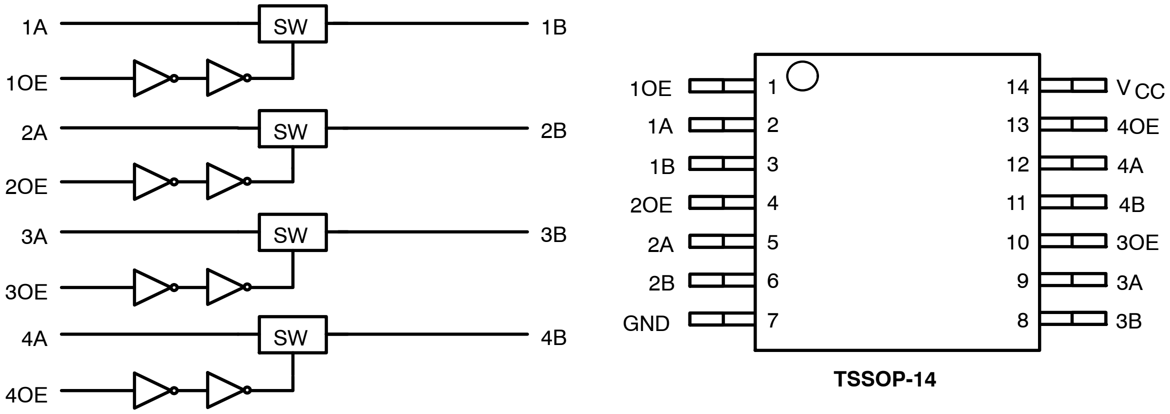


Figure 4. T30LMSW3B3126 Logic Diagram and Pin Assignment

T30LMSW3B3126 FUNCTION TABLE

OE	Function
L	Disconnect
H	A = B

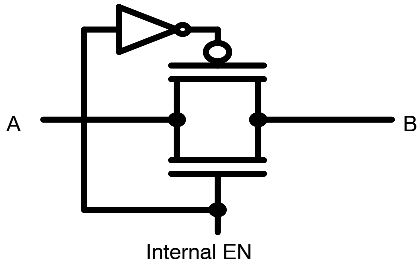


Figure 5. Individual FET Switch Simplified Schematic

MAXIMUM RATINGS

Symbol	Parameter	Condition	Value	Unit
V_{CC}	Supply Voltage		−0.5 to +4.3	V
V_I	Input Voltage (Note 1)		−0.5 to +4.3	V
	Continuous Channel Current		128	mA
I_{IK}	Input Clamp Current	$V_{I/O}$ < GND	−50	mA
I_{CC}	DC Supply Current Per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_J	Junction Temperature		+150	°C
T_{STG}	Storage Temperature		−65 to +150	°C
θ_{JA}	Thermal Resistance (Note 2) TSSOP-16 TSSOP-14		159 150	°C/W
P_D	Power Dissipation in Still Air TSSOP−16 TSSOP-14		787 833	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34		UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model		 4 2	kV
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 25 °C (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2 ounce copper trace no air flow per JESD51-7.
3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	1.65	3.6	V
V_I	Control Pin Input Voltage	GND	3.6	V
$V_{I/O}$	I/O Pin Voltage	GND	V_{CCA}	V
T_A	Operating Temperature Range	−40	+125	°C
$\Delta t/\Delta V$	Control Input Transition Rise or Fall Rate	0	200	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

				T_A = –40 °C to +85 °C			T_A = –40 °C to +125 °C		
Symbol	**Parameter**	**Test Conditions**	**V_{CCA} (V)**	**Min**	**Typ (Note 5)**	**Max**	**Min**	**Max**	**Unit**
V_{IH}	Input HIGH Voltage		1.65–1.95	0.7 * V_{CC}	–	–	0.7 * V_{CC}	–	V
			2.3–2.7	1.7	–	–	1.7	–	
			2.7–3.6	2.0	–	–	2.0	–	
V_{IL}	Input LOW Voltage		1.65–1.95	–	–	0.3 * V_{CC}	–	0.3 * V_{CC}	V
			2.3–2.7	–	–	0.7	–	0.7	
			2.7–3.6	–	–	0.8	–	0.8	
V_{IK}	Clamp Diode Voltage	I_I = –18 mA	3.0	–	–	–1.2	–	–1.2	V
I_I	Input Leakage	V_I = V_{CC} or GND	3.6	–	–	±0.5	–	±0.5	μA
I_{off}	Power Off Leakage	V_I or V_O = GND to 3.6 V	0	–	–	1.0	–	1.0	μA
I_{CC}	Supply Current	V_I = V_{CC} or GND, I_O = 0	3.6	–	–	1.0	–	1.0	μA
ΔI_{CC}	Additional Supply Current	Control Pins; One input at 3 V, Other inputs at V_{CC} or GND	3.6	–	–	100	–	100	μA
C_I	Control Input Capacitance	V_I = 3 V or GND		–	3	–	–	–	pF
$C_{IO(off)}$	Switch Off Capacitance (T30LMSW3B3257)	$\overline{OE}$ = V_{CC}; A		–	10.5	–	–	–	pF
		V_I = 3 V or GND B		–	6.5	–	–	–	
	Switch Off Capacitance (T30LMSW3B3253)	$\overline{OE}$ = V_{CC}; A		–	20.5	–	–	–	
		V_I = 3 V or GND B		–	6.5	–	–	–	
	Switch Off Capacitance (T30LMSW3B3125 / T30LMSW3B3126)	$\overline{OE}$ = V_{CC} or OE = GND;		–	7.0	–	–	–	
		V_I = 3 V or GND							
R_{ON}	ON Resistance	V_I = 0 V; I_I = 24 mA	1.65–1.95	–	6	10	–	10	Ω
		V_I = 1.05 V; I_I = 15 mA		–	26	50	–	50	
		V_I = 0 V; I_I = 64 mA	2.3–2.7	–	4	7	–	7	
		I_I = 24 mA		–	4	7	–	7	
		V_I = 1.7 V; I_I = 15 mA		–	10	20	–	20	
		V_I = 0 V; I_I = 64 mA	3.0–3.6	–	4	6	–	6	
		I_I = 24 mA		–	4	6	–	6	
		V_I = 2.4 V; I_I = 15 mA		–	8	12	–	12	

5. All typical values are at nominal value of V_{CC} range and T_A = 25 °C.

AC ELECTRICAL CHARACTERISTICS (T30LMSW3B3257/T30LMSW3B3253)

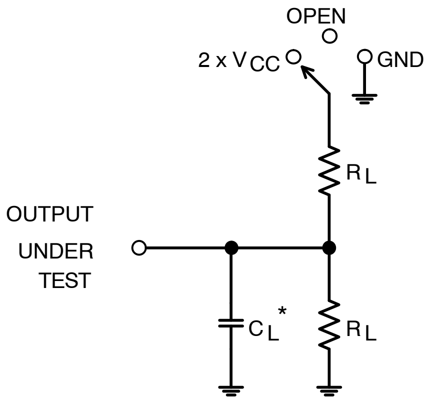
Symbol	Parameter	Test Conditions	V_{CCA} (V)	T_A = −40 °C to +85 °C			T_A = −40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	
t_{PD}	Propagation Delay (Note 6) A to B or B to A		1.65–1.95	–	–	0.15	–	0.15	ns
			2.3–2.7	–	–	0.15	–	0.15	
			3.0–3.6	–	–	0.25	–	0.25	
t_{EN}	Enable Time S to A or B		1.65–1.95	–	–	8.8	–	8.8	ns
			2.3–2.7	–	–	6.1	–	6.1	
			3.0–3.6	–	–	5.3	–	5.3	
	Enable Time $\overline{OE}$ to A or B		1.65–1.95	–	–	8.6	–	8.6	
			2.3–2.7	–	–	5.6	–	5.6	
			3.0–3.6	–	–	5	–	5	
t_{DIS}	Disable Time S to A or B		1.65–1.95	–	–	5.5	–	5.5	ns
			2.3–2.7	–	–	4.8	–	4.8	
			3.0–3.6	–	–	4.5	–	4.5	
	Disable Time $\overline{OE}$ to A or B		1.65–1.95	–	–	6.5	–	6.5	
			2.3–2.7	–	–	5.5	–	5.5	
			3.0–3.6	–	–	5.5	–	5.5	

AC ELECTRICAL CHARACTERISTICS (T30LMSW3B3125 / T30LMSW3B3126)

Symbol	Parameter	Test Conditions	V_{CCA} (V)	T_A = −40 °C to +85 °C			T_A = −40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	
t_{PD}	Propagation Delay (Note 6) A to B or B to A		1.65–1.95	–	–	0.15	–	0.15	ns
			2.3–2.7	–	–	0.15	–	0.15	
			3.0–3.6	–	–	0.25	–	0.25	
t_{EN}	Enable Time $\overline{OE}$ to A or B		1.65–1.95	–	–	8.6	–	8.6	ns
			2.3–2.7	–	–	5.6	–	5.6	
			3.0–3.6	–	–	5	–	5	
t_{DIS}	Disable Time $\overline{OE}$ to A or B		1.65–1.95	–	–	6.5	–	6.5	ns
			2.3–2.7	–	–	5.5	–	5.5	
			3.0–3.6	–	–	5.5	–	5.5	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

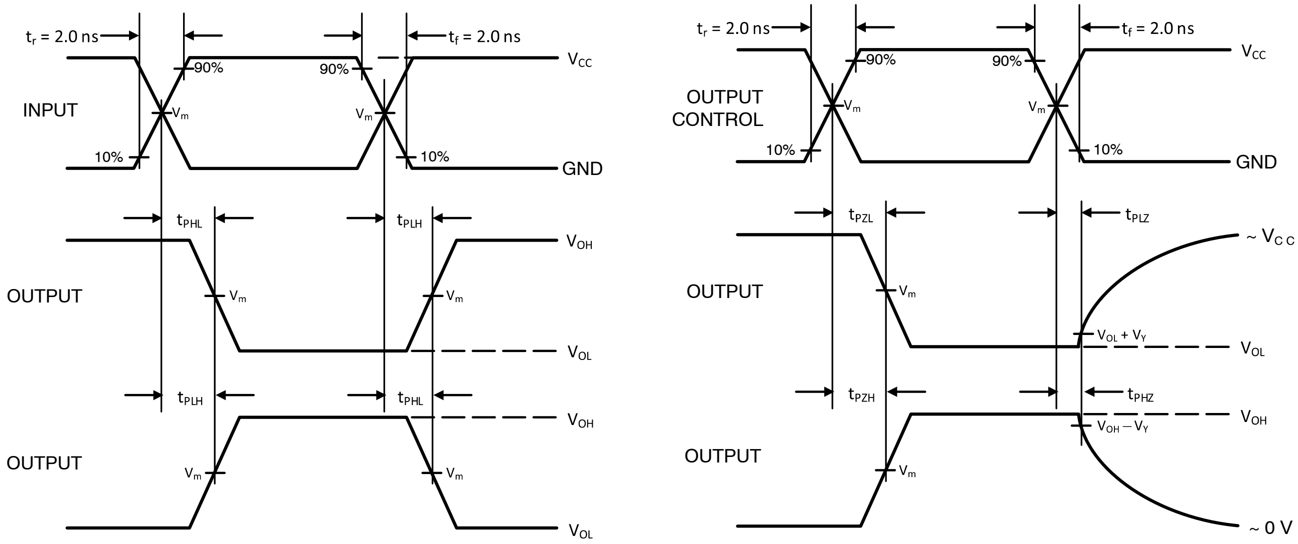
6. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	2 x VCC
t_{PHZ} / t_{PZH}	GND

C_L includes load and jig capacitance
Pulse generator Z_O = 50 Ω
Input f = 10 MHz; t_W = 500 ns

Figure 6. AC Test Circuit



V_{CC}, V	C_L, pF	R_L, Ω	V_m, V	V_Y, V
1.65 V to 1.95 V	15	500	$V_{CC}/2$	0.1
2.3 V to 2.7 V	30	500	$V_{CC}/2$	0.15
3.0 V to 3.6 V	50	500	$V_{CC}/2$	0.3

Figure 7. AC Waveforms

ORDERING INFORMATION

Device	Marking	Pin 1 Quadrant	Package	Shipping†
T30LMSW3B3257DTR2G	T3SW 3257	1	TSSOP-16	2500 / Tape & Reel
T30LMSW3B3253DTR2G	T3SW 3253	1	TSSOP-16	2500 / Tape & Reel
T30LMSW3B3125DTR2G	T3SW 3125	1	TSSOP-14	2500 / Tape & Reel
T30LMSW3B3126DTR2G	T3SW 3126	1	TSSOP-14	2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Pin 1 Orientation in Tape and Reel

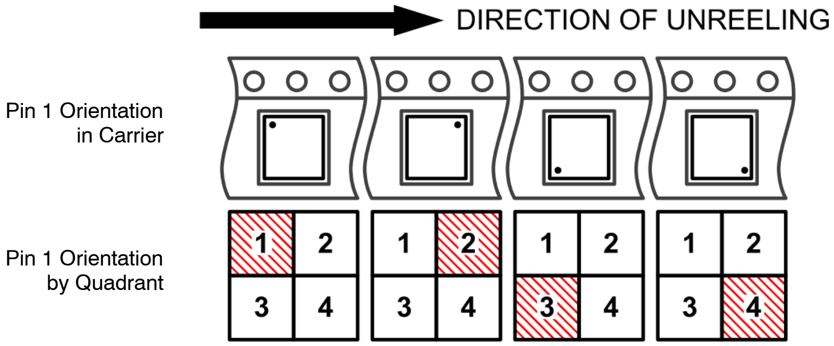


Figure 8.

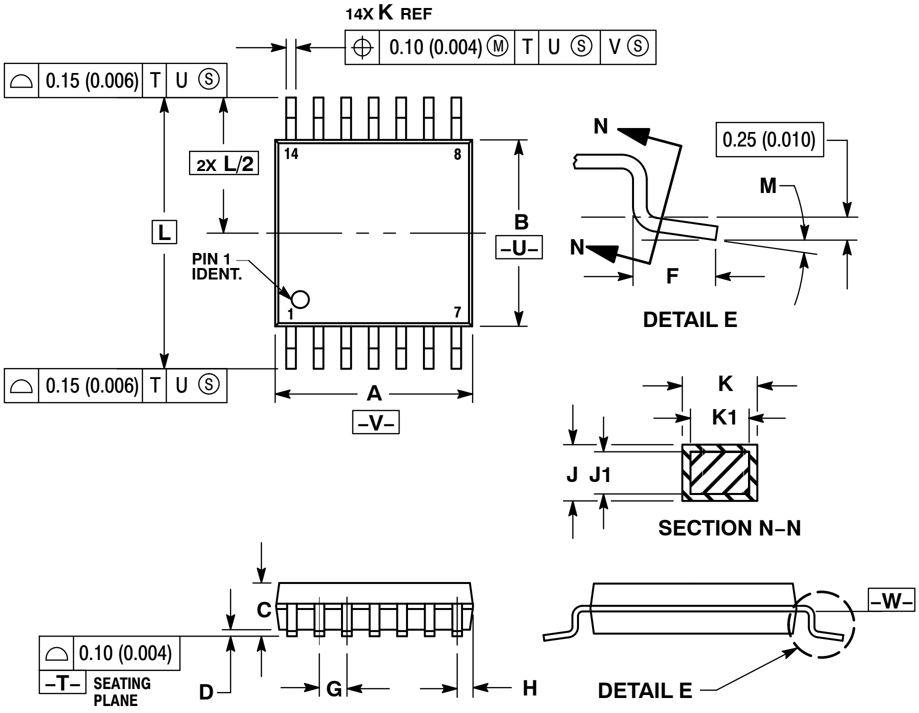
REVISION HISTORY

Revision	Description of Changes	Date
P3	Revision to correct two marking diagrams only.	11/28/2025
P4	Corrected several values on pages 4−6 and added package marking information to OPNs.	5/12/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

PACKAGE DIMENSIONS

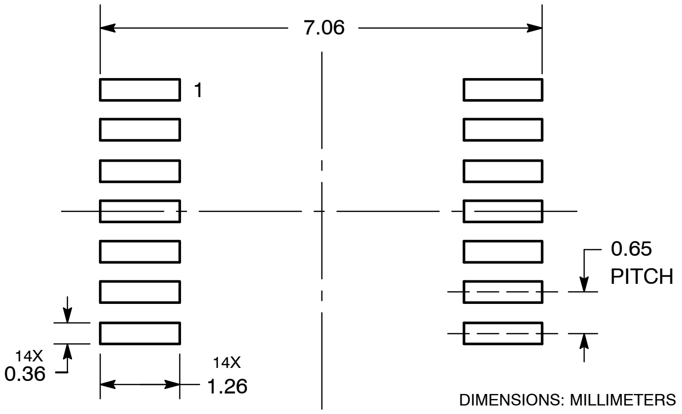
TSSOP−14 WB
CASE 948G
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

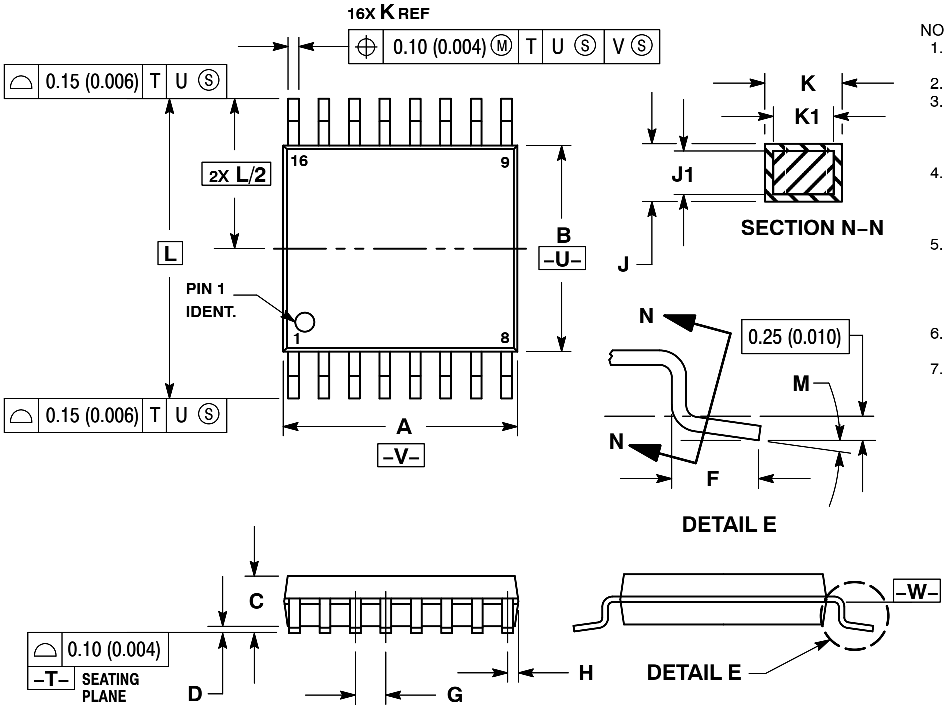
RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

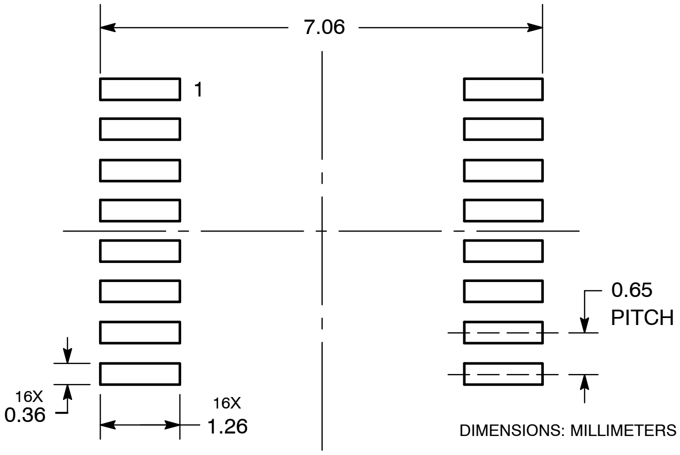
TSSOP−16 WB
CASE 948F
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

onsemi, onsemi, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

◊