

ESD Protection - In-Vehicle Networks

Automotive Qualified Low Capacitance High Speed Data Network Protection

SZESD9901

The SZESD9901 protects sensitive automotive electronics from ESD, Surge, and other harmful transient events. This device is designed for compliance to OPEN Alliance 100/1000 BASE-T1 Ethernet, and other high speed data networks. Device is suitable for ESD protection on the connector side of the transceiver PHY.

Features

- High Trigger Voltage ≥ 100 V
- X2DFN 1.0 x 0.6 mm Package
- Wettable Flank Package for Optimal Automated Optical Inspection (AOI)
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Open Alliance 100/1000 BASE-T1 Ethernet
- In Vehicle Networking (IVN)
- High Speed Data Networks

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature – Maximum (10 Seconds)	T_L	260	$^\circ\text{C}$
Human Body Model (HBM) IEC 61000-4-2 Contact (ESD) IEC 61000-4-2 Air (ESD) ISO 10605 150 pF / 330 Ω Contact* ISO 10605 330 pF / 330 Ω Contact ISO 10605 330 pF / 2 k Ω Contact ISO 10605 150 pF / 2 k Ω Contact * minimum number of discharges > 1000	ESD	± 8 ± 30 ± 30 ± 30 ± 30 ± 30 ± 30	kV
Maximum Peak Pulse Current 8/20 μs	I_{pp}	2.2	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Complies with the Following Standards:

- ISO7637-2, Jumpstart, Load Dump
- Open Alliance 100/1000 BASE-T1 Ethernet
- ISO7637-3, Pulse 2a 85 V, 3a 3b 150 V

MARKING DIAGRAM



X2DFNW2
CASE 711BG



DA = Specific Device Code
M = Date Code

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping [†]
SZESD9901MX2WT5G	X2DFNW2 (Pb-Free)	8,000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

ELECTRICAL CHARACTERISTICS

(T_A = 25 °C unless otherwise noted)

Symbol	Parameter
V _{RWM}	Working Peak Voltage
I _R	Maximum Reverse Leakage Current @ V _{RWM}
V _{trigger}	Trigger Voltage @ I _T
I _T	Test Current
V _{HOLD}	Holding Reverse Voltage
I _{HOLD}	Holding Reverse Current
R _{DYN}	Dynamic Resistance
I _{PP}	Maximum Peak Pulse Current
V _C	Clamping Voltage @ I _{PP} V _C = V _{HOLD} + (I _{PP} * R _{DYN})

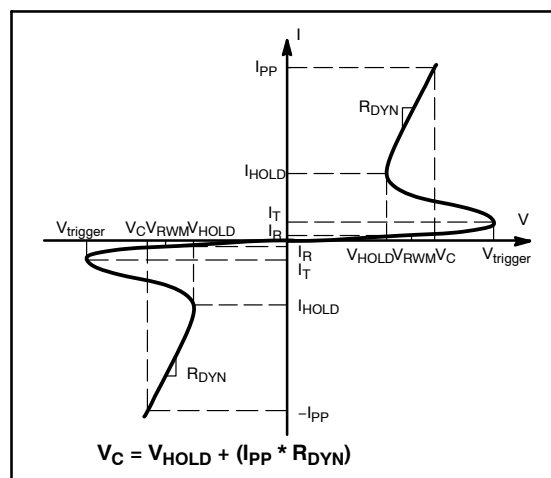


Figure 1. Bi-Directional

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{RWM}	Reverse Working Voltage	I/O Pin to GND			25	V
I _R	Reverse Leakage Current	V _{RWM} = 25 V		1	200	nA
V _{HOLD}	Reverse Holding Voltage	I/O Pin to GND	25	30		V
I _{HOLD}	Holding Reverse Current	I/O Pin to GND		4		A
V _C	Clamping Voltage TLP	ITLP = 4 A ITLP = 8 A ITLP = 16 A ITLP = 20 A		31 34 37 39		V
V _{trigger}	ESD Trigger Voltage (Note 2)	I _T = 1 mA, I/O Pin to GND	100			V
C _{Jio-gnd}	Channel Capacitance	V _R = 0 V, f = 1 MHz		2.3	2.6	pF
R _{DYN}	Dynamic Resistance (Note 2)	I/O to GND, GND to I/O		0.4		Ω
I _L	Insertion Loss	f = 1 GHz f = 5 GHz		9 5		dB
R _L	Return Loss	f = 1 GHz f = 5 GHz		12 6		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- For test procedure see Figure 16 and application note AND8307/D.
- ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
TLP conditions: Z₀ = 50 Ω, t_p = 100 ns, t_r = 1 ns, averaging window: t₁ = 70 ns to t₂ = 90 ns.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

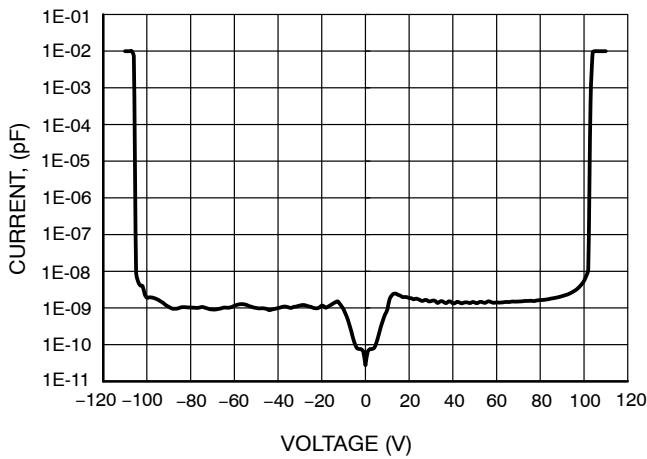


Figure 2. IV Characteristics

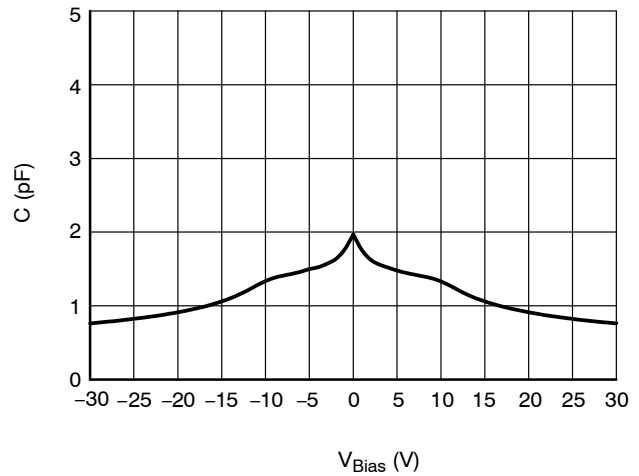


Figure 3. CV Characteristics

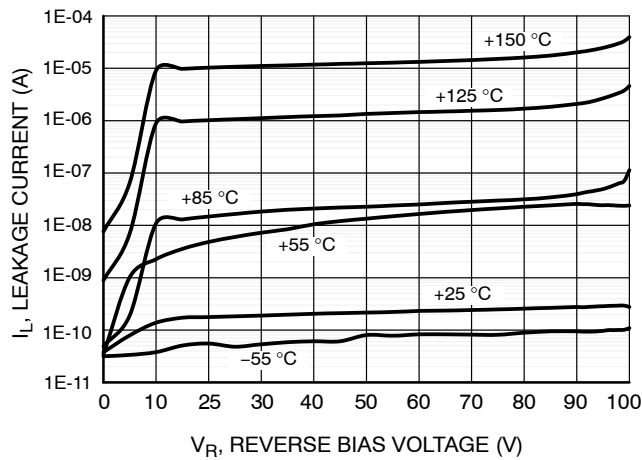


Figure 4. IR vs. Temperature Characteristics

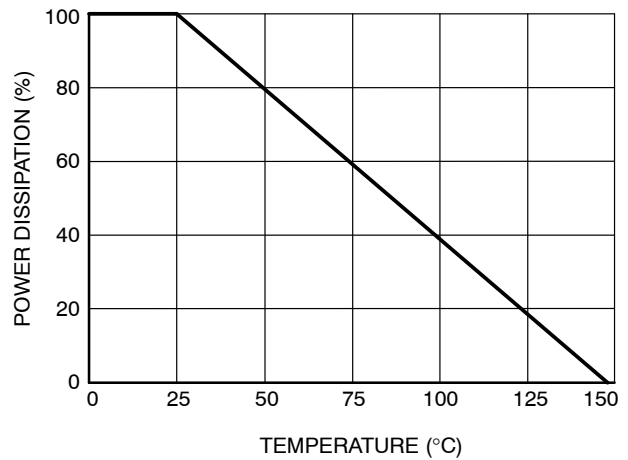


Figure 5. Steady State Power Derating

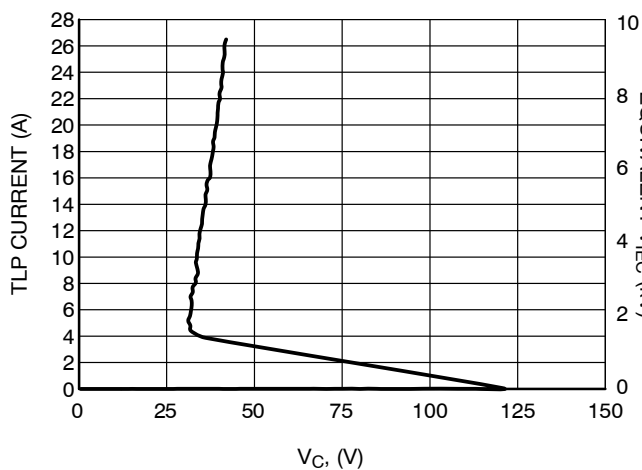


Figure 6. Positive TLP IV Curve

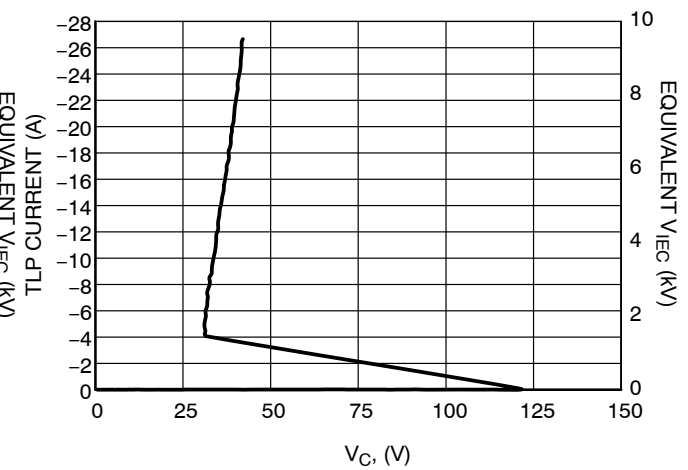


Figure 7. Negative TLP IV Curve

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

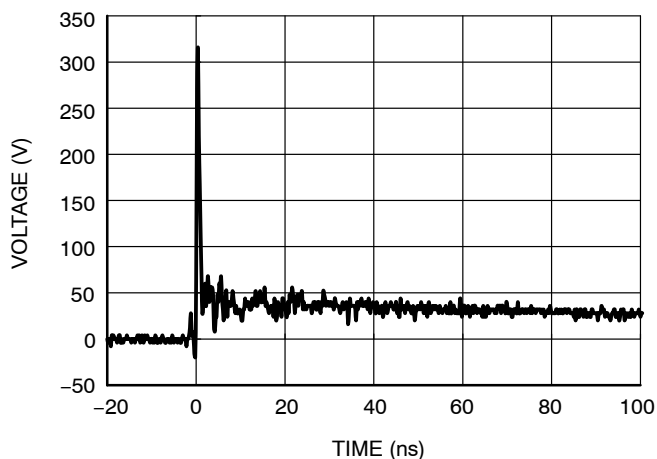


Figure 8. IEC61000-4-2 +8 kV Contact

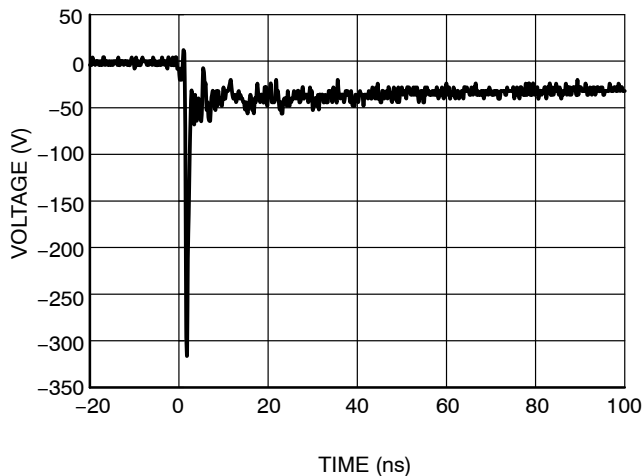


Figure 9. IEC61000-4-2 -8 kV Contact

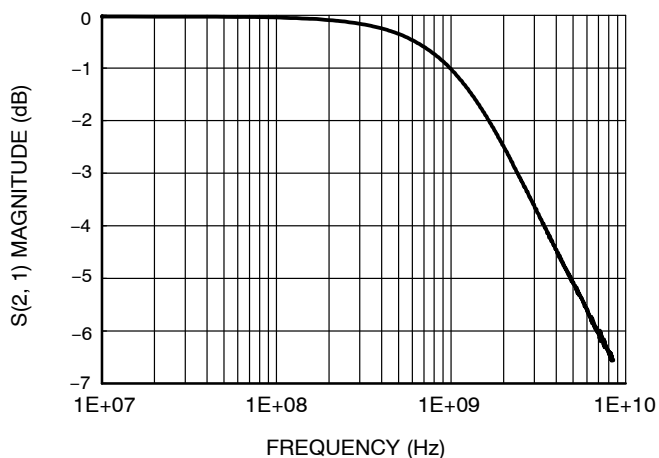


Figure 10. Typical Insertion Loss

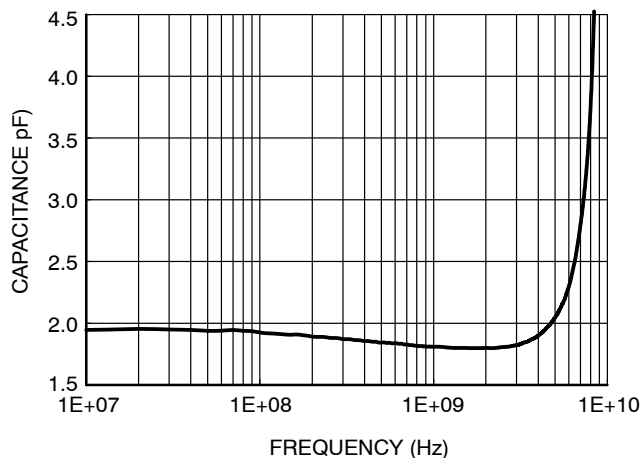


Figure 11. Typical Capacitance vs. Frequency

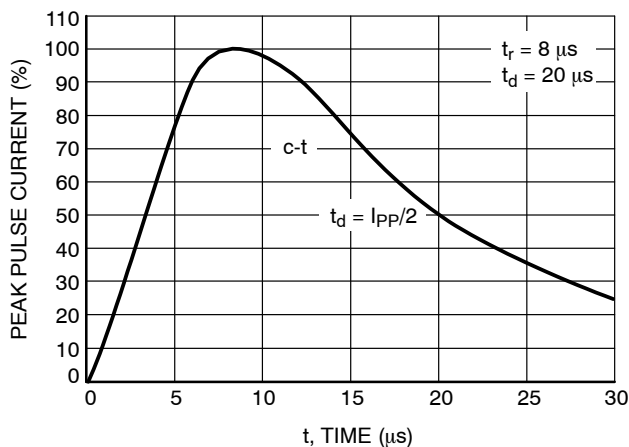


Figure 12. Pulse Waveform (8/20 μs)

Latch-Up Considerations

onsemi's 8000 series of ESD protection devices utilize a snap-back, SCR type structure. By using this technology, the potential for a latch-up condition was taken into account by performing load line analyses of common high speed serial interfaces. Example load lines for latch-up free applications and applications with the potential for latch-up are shown below with a generic IV characteristic of a snapback, SCR type structured device overlaid on each. In the latch-up free load line case, the IV characteristic of the snapback protection device intersects the load-line in one unique point (V_{OP} , I_{OP}). This is the only stable operating point of the

circuit and the system is therefore latch-up free. In the non-latch up free load line case, the IV characteristic of the snapback protection device intersects the load-line in two points (V_{OPA} , I_{OPA}) and (V_{OPB} , I_{OPB}). Therefore in this case, the potential for latch-up exists if the system settles at (V_{OPB} , I_{OPB}) after a transient. Because of this, SZESD9901 should not be used for HDMI applications – ESD8104 or ESD8040 have been designed to be acceptable for HDMI applications without latch-up. Please refer to Application Note AND9116/D for a more in-depth explanation of latch-up considerations using ESD8000 series devices.

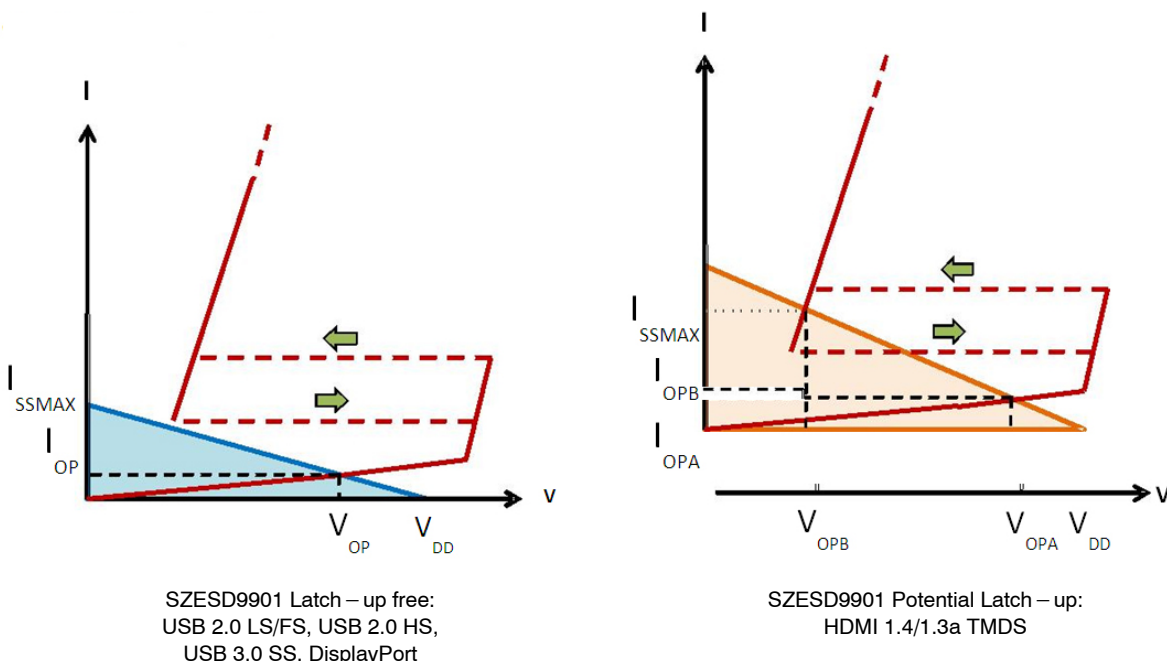


Figure 13. Example Load Lines for Latch-up Free Applications and Applications with the Potential for Latch-up

Table 1. SUMMARY OF SCR REQUIREMENTS FOR LATCH-UP FREE APPLICATIONS

Application	VBR (min) (V)	IH (min) (mA)	VH (min) (V)	onsemi ESD8000 Series Recommended PN
HDMI 1.4/1.3a TMDS	3.465	54.78	1.0	ESD8104, ESD8040
USB 2.0 LS/FS	3.301	1.76	1.0	ESD8004, ESD8551
USB 2.0 HS	0.482	N/A	1.0	ESD8004, ESD8551
USB 3.0 SS	2.800	N/A	1.0	ESD8004, ESD8006, ESD8551
DisplayPort	3.600	25.00	1.0	ESD8004, ESD8006, ESD8551

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how creates these screenshots and how to interpret them please refer to AND8307/D.

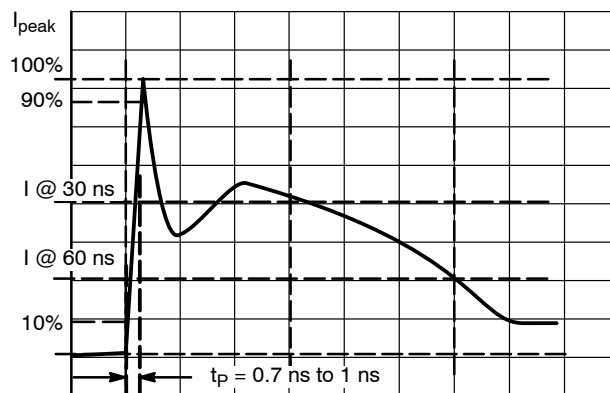


Figure 14. IEC61000-4-2 Current Waveform

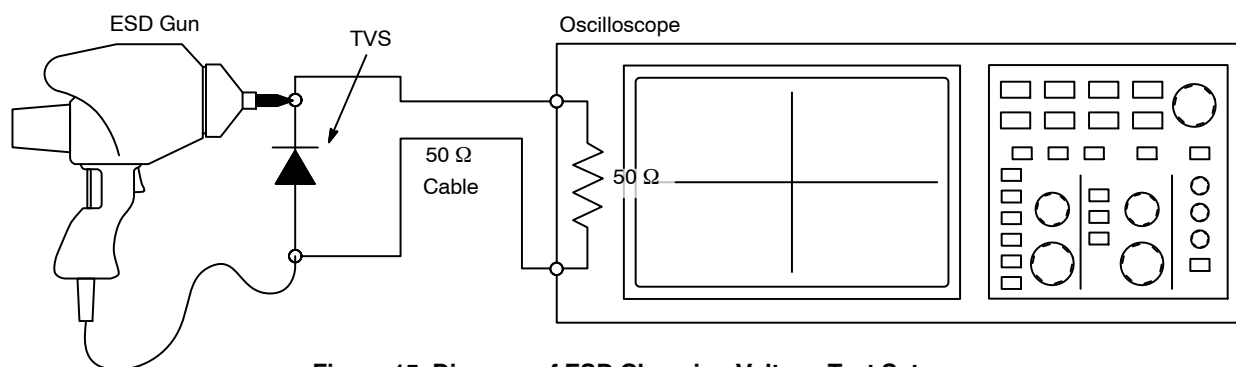


Figure 15. Diagram of ESD Clamping Voltage Test Setup

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

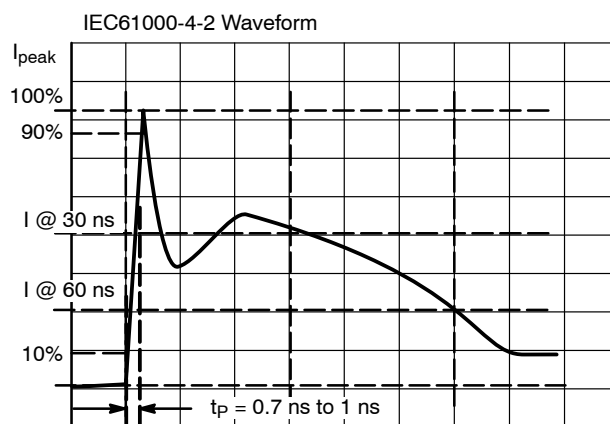


Figure 16. IEC61000-4-2 Spec

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 17. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 18 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

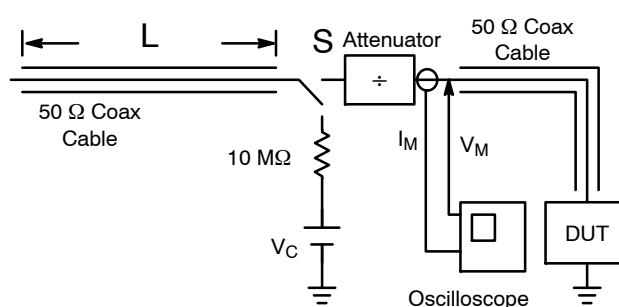


Figure 17. Simplified Schematic of a Typical TLP System

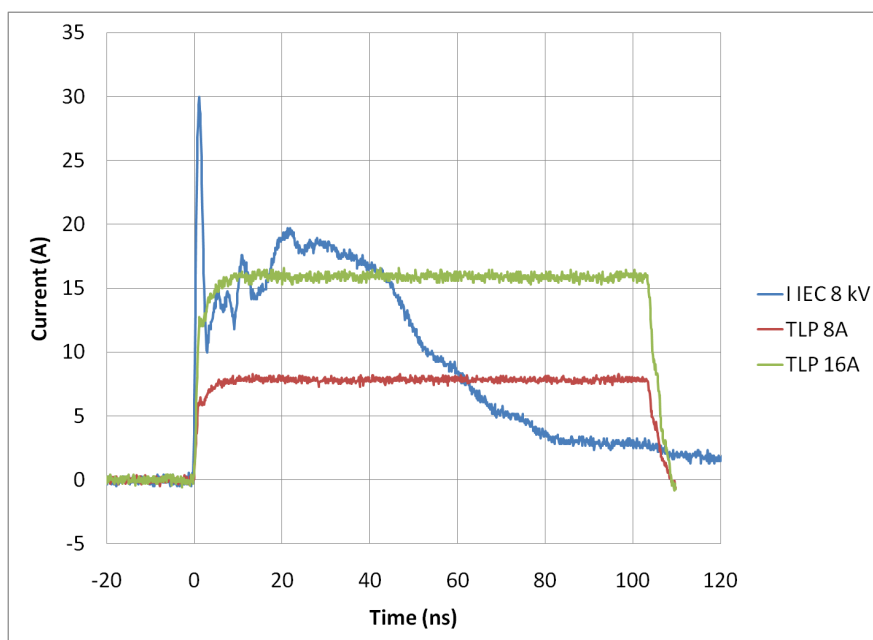


Figure 18. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

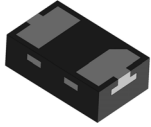
SZESD9901

REVISION HISTORY

Revision	Description of Changes	Date
2	Updated datasheet with new information to ensure standardized format and up-to-date data.	5/6/2026

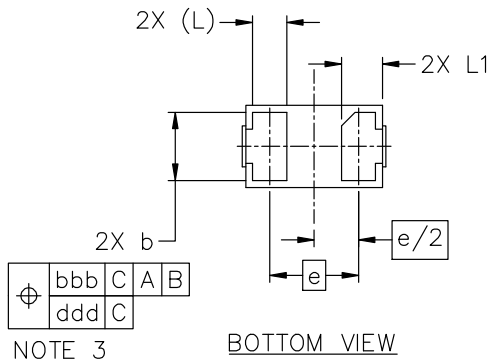
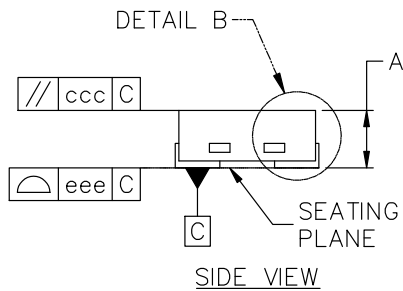
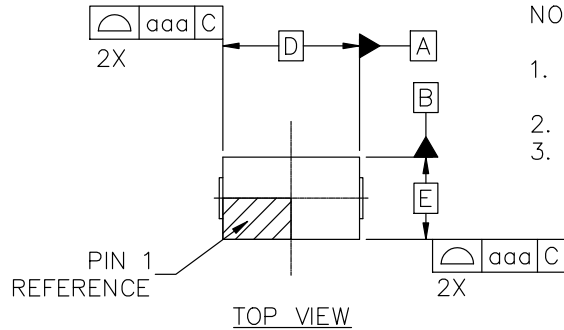
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.





X2DFNW-2 1.00x0.60x0.37, 0.65P
CASE 711BG
ISSUE F

DATE 06 NOV 2025



NOTE 3

**GENERIC
MARKING DIAGRAM***

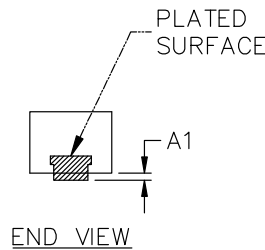
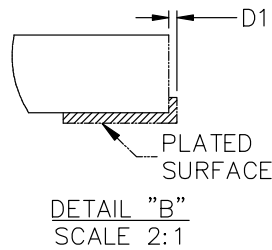


XX = Specific Device Code
M = Date Code

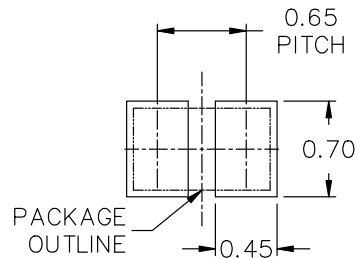
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
A1	~	~	0.05
b	0.45	0.50	0.55
D	1.00 BSC		
D1	~	~	0.05
E	0.60 BSC		
e	0.65 BSC		
L	0.22 REF		
L1	0.24	0.28	0.34
TOLERANCE FORM & POSITION			
aaa	0.05		
bbb	0.10		
ccc	0.05		
ddd	0.05		
eee	0.05		



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	X2DFNW-2 1.00x0.60x0.37, 0.65P	PAGE 1 OF 1

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