

MOSFET - Power, Single N-Channel, STD Gate, SO8FL

40 V, 1.3 mΩ, 195 A

NVMFWS1D3N04XM

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (5 x 6 mm) with Compact Design
- AECQ101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

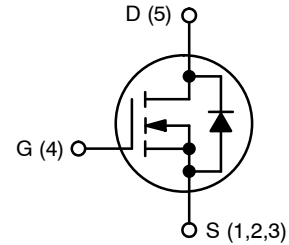
- Motor Drive
- Battery Protection
- Synchronous Rectification

MAXIMUM RATINGS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise stated)

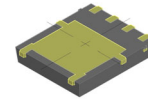
Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	40	V
Gate-to-Source Voltage	DC V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C = 25\text{ }^\circ\text{C}$	195
		$T_C = 100\text{ }^\circ\text{C}$	138
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	90
Continuous Drain Current $R_{\theta JA}$	I_{DA}	$T_A = 25\text{ }^\circ\text{C}$	40
		$T_A = 100\text{ }^\circ\text{C}$	28
Pulsed Drain Current	$T_C = 25\text{ }^\circ\text{C}$, $t_p = 10\text{ }\mu\text{s}$	I_{DM}	900
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	74.5	A
Single Pulse Avalanche Energy ($I_{PK} = 11.1\text{ A}$)	E_{AS}	306	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

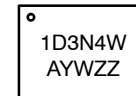
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
40 V	1.3 mΩ @ $V_{GS} = 10\text{ V}$	195 A



N-CHANNEL MOSFET



**DFNW5 (SO-8FL)
CASE 507BA**



1D3N4W = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMFWS1D3N04XM

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction-to-Ambient (Notes 1, 2)	$R_{\theta JA}$	40.1	

- Surface mounted on FR4 board using 650 mm², 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25\text{ }^\circ\text{C}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to 25 °C		15		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, T_J = 25\text{ }^\circ\text{C}$			10	μA
		$V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$			100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 25\text{ }^\circ\text{C}$		1.17	1.3	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 100\text{ } \mu\text{A}, T_J = 25\text{ }^\circ\text{C}$	2.5		3.5	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 100\text{ } \mu\text{A}$		-7.23		mV/°C
Forward Trans-conductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 20\text{ A}$		105		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		2459		pF
Output Capacitance	C_{OSS}			1578		
Reverse Transfer Capacitance	C_{RSS}			23.3		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DD} = 32\text{ V}; I_D = 50\text{ A}$		38.6		nC
Threshold Gate Charge	$Q_{G(TH)}$			7.2		
Gate-to-Source Charge	Q_{GS}			11.3		
Gate-to-Drain Charge	Q_{GD}			7.4		
Gate Resistance	R_G	$f = 1\text{ MHz}$		0.72		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 32\text{ V},$ $I_D = 50\text{ A}, R_G = 0\text{ } \Omega$		19.1		ns
Rise Time	t_r			6.2		
Turn-Off Delay Time	$t_{d(OFF)}$			30.4		
Fall Time	t_f			5.2		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 20\text{ A}, T_J = 25\text{ }^\circ\text{C}$		0.8		V
		$V_{GS} = 0\text{ V}, I_S = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.65		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_S = 50\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 32\text{ V}$		46		ns
Charge Time	t_a			22		
Discharge Time	t_b			24		
Reverse Recovery Charge	Q_{RR}			55		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

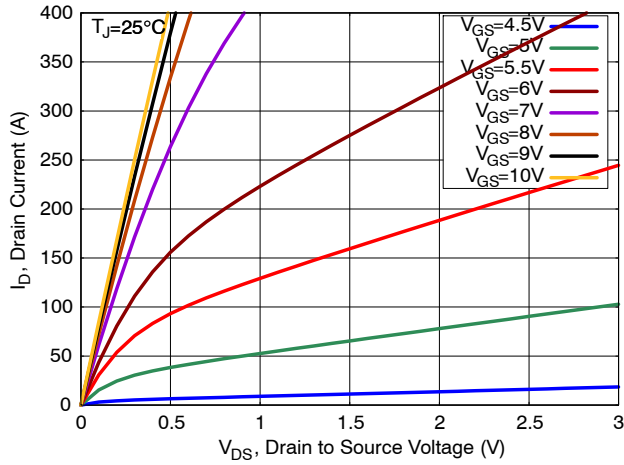


Figure 1. On-Region Characteristics

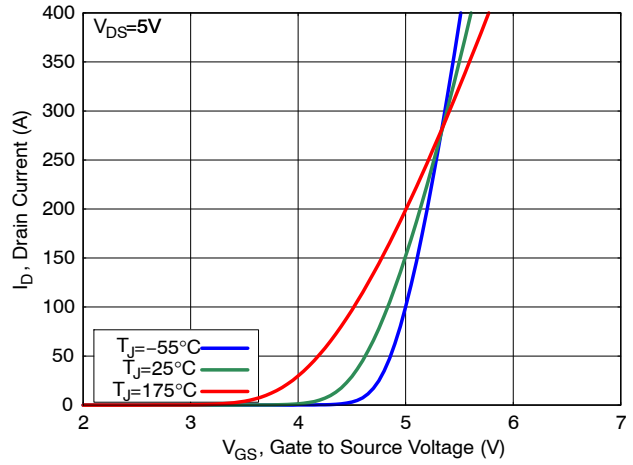


Figure 2. Transfer Characteristics

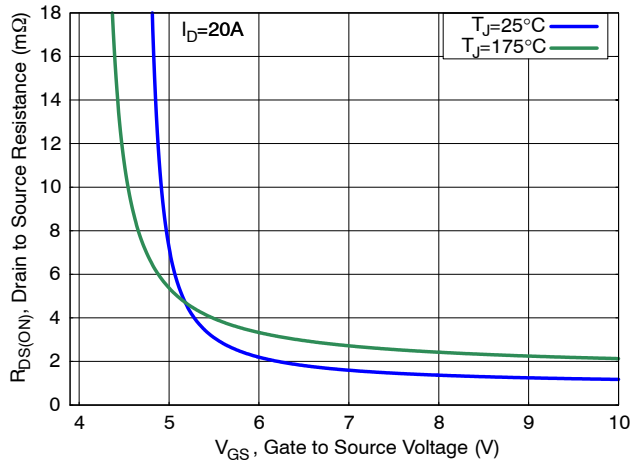


Figure 3. On-Resistance vs. V_{GS}

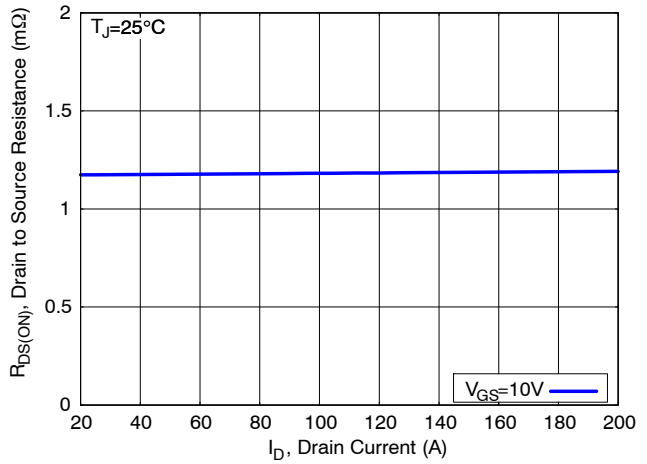


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

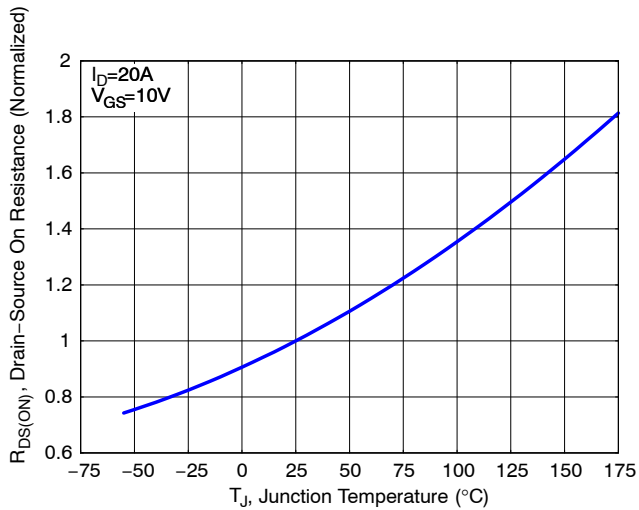


Figure 5. On-Resistance Variation with Temperature

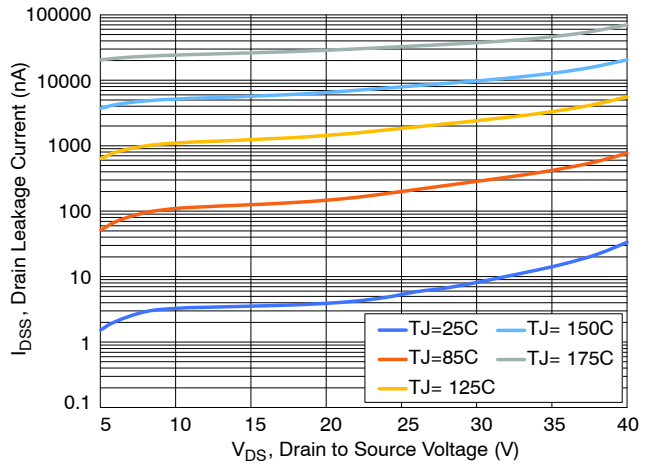


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

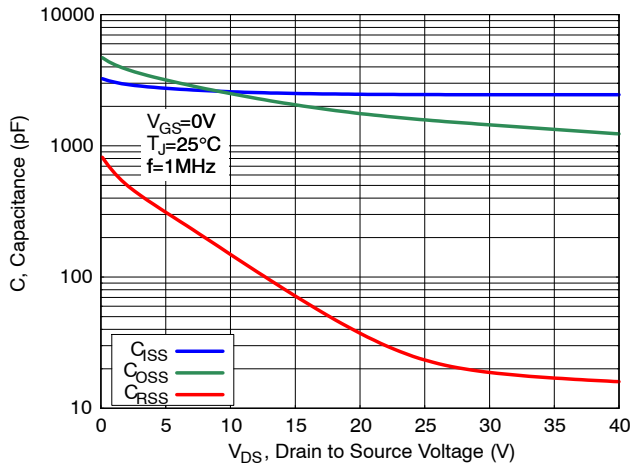


Figure 7. Capacitance Characteristics

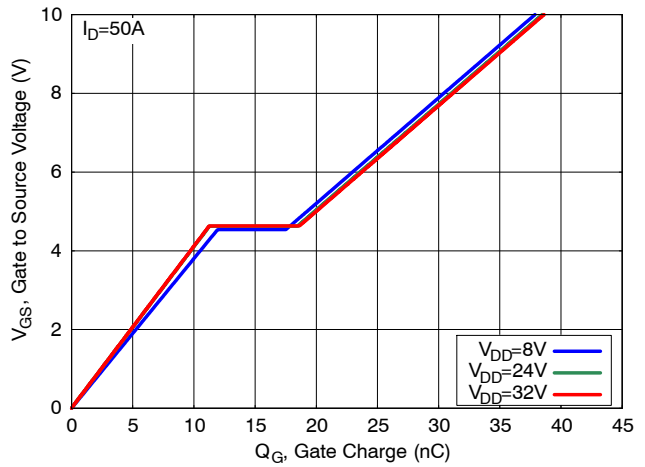


Figure 8. Gate-to-Source Voltage vs. Total Charge

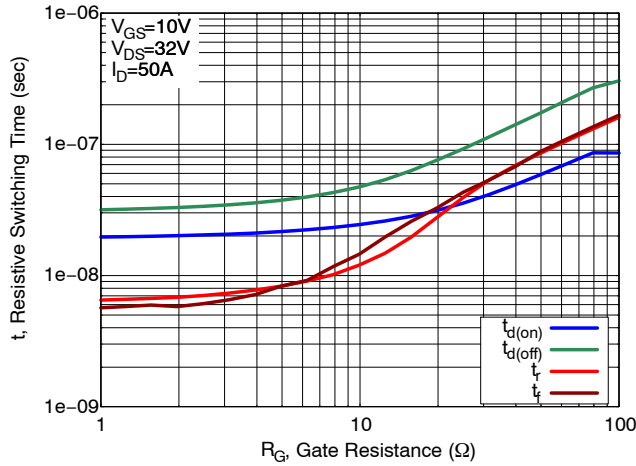


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

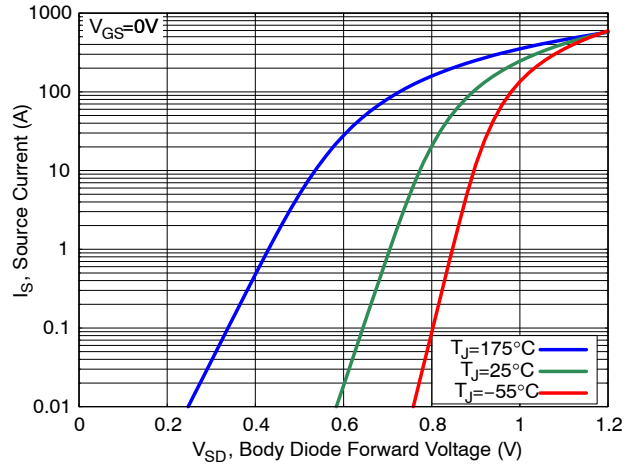


Figure 10. Diode Forward Voltage vs. Current

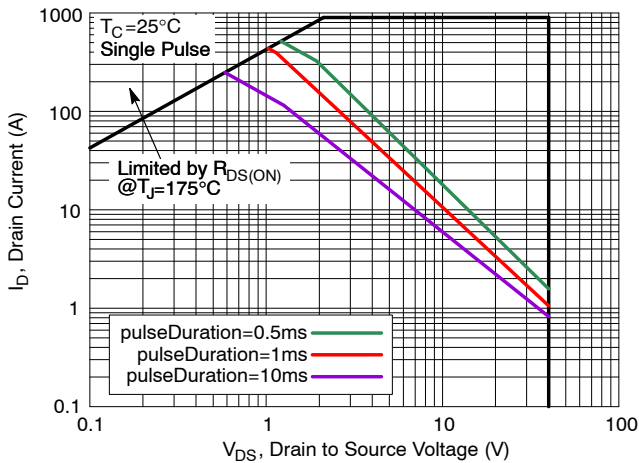


Figure 11. Safe Operating Area (SOA)

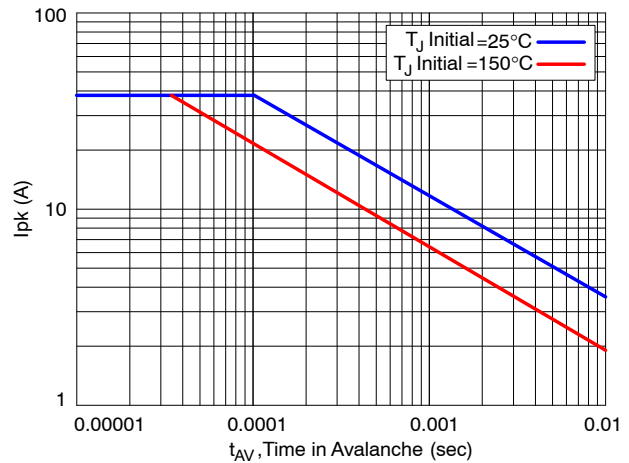


Figure 12. Avalanche Current vs Pulse Time (UIS)

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TYPICAL CHARACTERISTICS

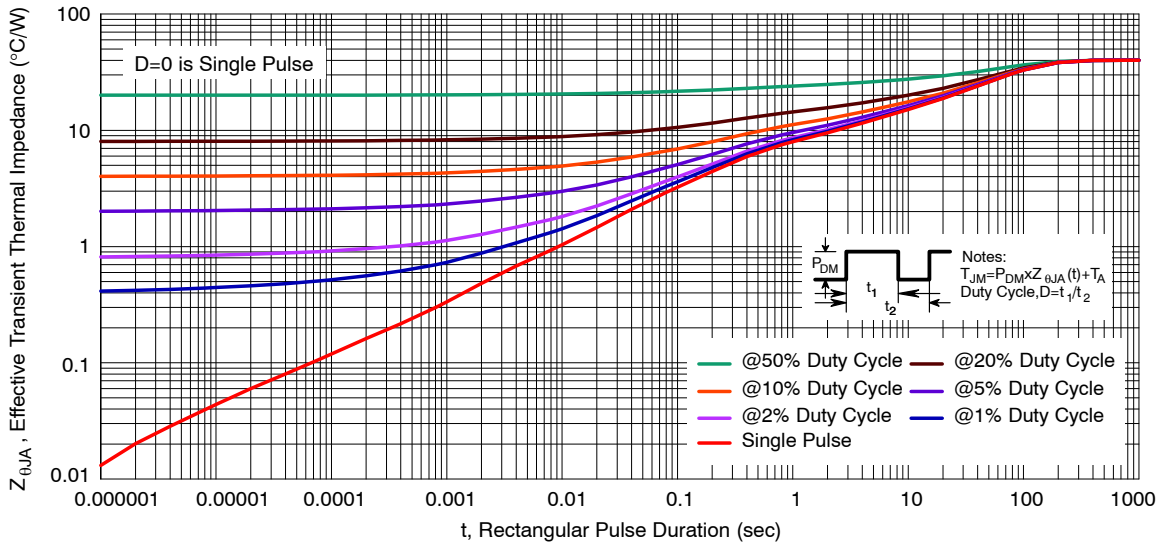


Figure 13. Transient Thermal Response

ORDERING INFORMATION

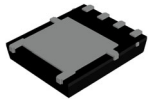
Device	Marking	Package	Shipping†
NVMFWS1D3N04XMT1G	1D3N4W	DFNW5 (Pb-Free)	1500 / Tape & Reel
NVMFWS1D3N04XMET1G	1D3N4W	DFNW5 (Pb-Free)	1500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

REVISION HISTORY

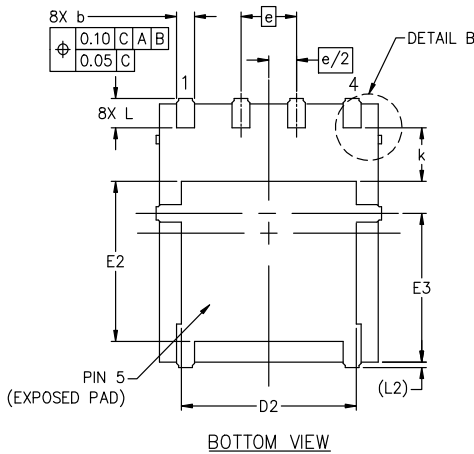
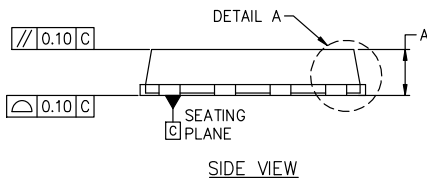
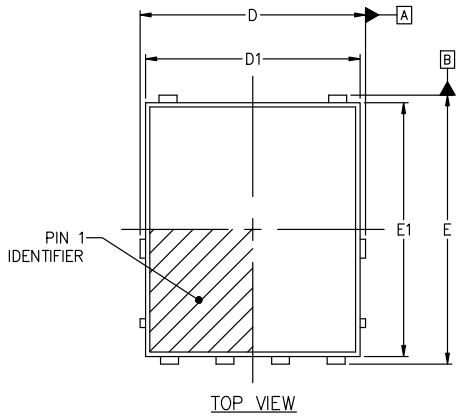
Revision	Description of Changes	Date
4	Added one new OPN.	4/23/2026

* Please note that this document has been previously updated prior to the inclusion of this revision history table and that the changes tracked only reflect what has occurred on the noted approval dates.



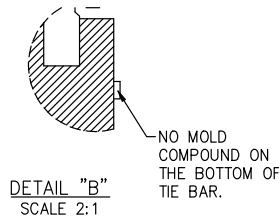
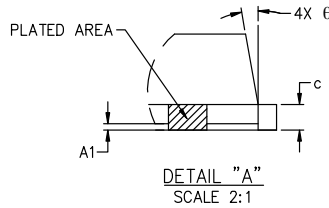
**DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BA
ISSUE C**

DATE 19 SEP 2024

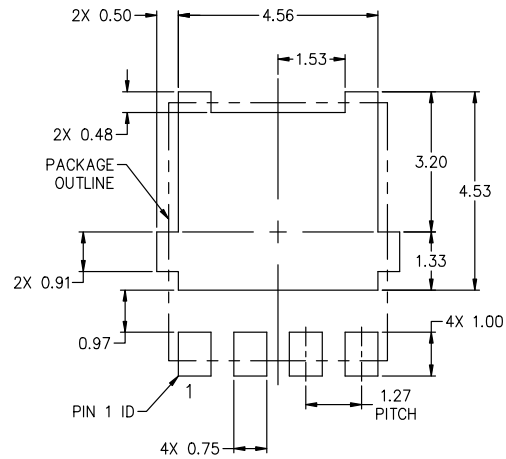


NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
theta	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT*
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DFNW5 4.90x5.90x1.00, 1.27P	PAGE 1 OF 1

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