

# Silicon Carbide (SiC) MOSFET - EliteSiC, 960 mohm, 1700 V, M1, TO-247-3L

## NVHL1000N170M1

### Features

- Typ.  $R_{DS(on)}$  = 960 m $\Omega$  @  $V_{GS} = 20$  V
- Ultra Low Gate Charge ( $Q_{G(tot)} = 14$  nC)
- High Speed Switching with Low Capacitance ( $C_{oss} = 11$  pF)
- 100% Avalanche Tested
- AEC-Q101 Qualified and PPAP Capable
- This Device is Halide Free and RoHS Compliant with exemption 7a, Pb-Free 2LI (on second level interconnection)

### Typical Applications

- Flyback Converter

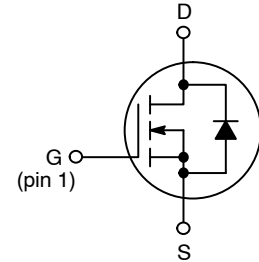
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	1700	V
Gate-to-Source Voltage	$V_{GS}$	-15/+25	V
Recommended Operation Values of Gate-to-Source Voltage	$T_C < 175^\circ\text{C}$ $V_{GSop}$	-5/+20	V
Continuous Drain Current (Note 1)	Steady State $T_C = 25^\circ\text{C}$ $I_D$	4.2	A
Power Dissipation (Note 1)	$P_D$	48	W
Continuous Drain Current (Note 1)	Steady State $T_C = 100^\circ\text{C}$ $I_D$	3	A
Power Dissipation (Note 1)	$P_D$	24	W
Pulsed Drain Current (Note 2)	$T_C = 25^\circ\text{C}$ $I_{DM}$	14	A
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	9.5	A
Single Pulse Drain-to-Source Avalanche Energy (Note 3)	$E_{AS}$	24	mJ
Maximum Lead Temperature for Soldering (1/25" from case for 10 s)	$T_L$	270	$^\circ\text{C}$

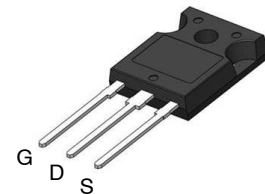
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Repetitive rating, limited by max junction temperature.
3.  $E_{AS}$  of 24 mJ is based on starting  $T_J = 25^\circ\text{C}$ ;  $L = 1$  mH,  $I_{AS} = 6.9$  A,  $V_{DD} = 120$  V,  $V_{GS} = 20$  V.

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	$I_D$ MAX
1700 V	960 m $\Omega$ @ 20 V	4.2 A



N-CHANNEL MOSFET



TO-247-3LD  
CASE 340CX

### MARKING DIAGRAM



A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Lot Traceability  
HL1000N170M1 = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping
NVHL1000N170M1	TO-247-3L	30 Units / Tube

# NVHL1000N170M1

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case – Steady State (Note 1)	$R_{\theta JC}$	3.1	°C/W

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	1700			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 1\text{ mA}$ , referenced to $25^\circ\text{C}$ (Note 4)		0.5		V/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 1700\text{ V}$	$T_J = 25^\circ\text{C}$		100	$\mu\text{A}$
			$T_J = 175^\circ\text{C}$		1	mA
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = +25/-15\text{ V}, V_{DS} = 0\text{ V}$			$\pm 1$	$\mu\text{A}$

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 640\text{ }\mu\text{A}$	1.8	3.2	4.3	V
Recommended Gate Voltage	$V_{GOP}$		-5		+20	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 20\text{ V}, I_D = 2\text{ A}, T_J = 25^\circ\text{C}$ $V_{GS} = 20\text{ V}, I_D = 2\text{ A}, T_J = 175^\circ\text{C}$ (Note 4)		960	1430	m $\Omega$
				1800		
Forward Transconductance	$g_{FS}$	$V_{DS} = 10\text{ V}, I_D = 2\text{ A}$ (Note 4)		0.6		S

### CHARGES, CAPACITANCES & GATE RESISTANCE (Note 4)

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 1000\text{ V}$		150		pF
Output Capacitance	$C_{OSS}$			11		
Reverse Transfer Capacitance	$C_{RSS}$			0.6		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -5/20\text{ V}, V_{DS} = 800\text{ V}, I_D = 2\text{ A}$		14		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.5		
Gate-to-Source Charge	$Q_{GS}$			2.6		
Gate-to-Drain Charge	$Q_{GD}$			7.5		
Gate-Resistance	$R_G$		$f = 1\text{ MHz}$		5.7	

### SWITCHING CHARACTERISTICS (Notes 4, 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -5/20\text{ V}, V_{DS} = 800\text{ V}, I_D = 2\text{ A}, R_G = 25\text{ }\Omega$ inductive load $L = 300\text{ }\mu\text{H}$		5.6		ns
Rise Time	$t_r$			30		
Turn-Off Delay Time	$t_{d(OFF)}$			11		
Fall Time	$t_f$			84		$\mu\text{J}$
Turn-On Switching Loss	$E_{ON}$			120		
Turn-Off Switching Loss	$E_{OFF}$			11		
Total Switching Loss	$E_{tot}$			131		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Continuous Drain-Source Diode Forward Current (Note 1)	$I_{SD}$	$V_{GS} = -5\text{ V}, T_J = 25^\circ\text{C}$		9.5		A
Pulsed Drain-Source Diode Forward Current (Note 2)	$I_{SDM}$			48		
Forward Diode Voltage	$V_{SD}$	$V_{GS} = -5\text{ V}, I_{SD} = 2\text{ A}, T_J = 25^\circ\text{C}$		4.2		V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = -5/20\text{ V}, I_{SD} = 2\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}$ (Note 4)		5.9		ns
Reverse Recovery Charge	$Q_{RR}$			11		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Defined by design, not subject to production test.

5.  $E_{ON}/E_{OFF}$  result is with body diode.

TYPICAL CHARACTERISTICS

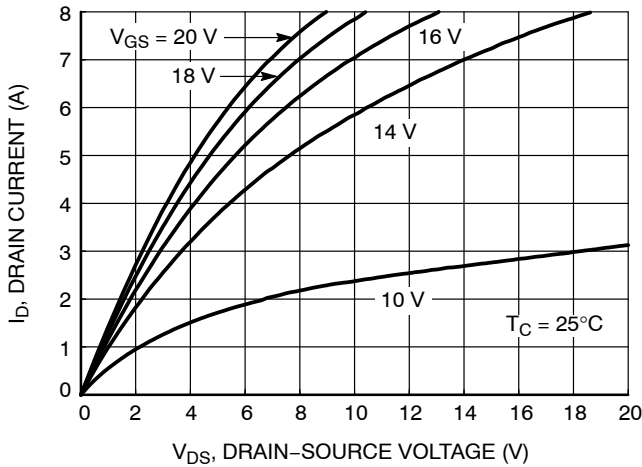


Figure 1. On-Region Characteristics

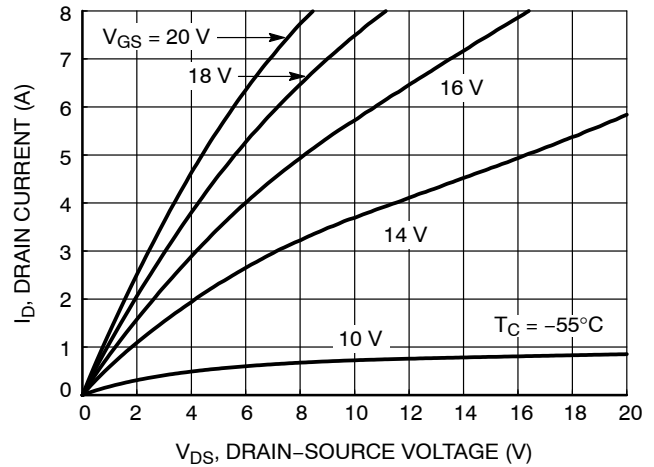


Figure 2. On-Region Characteristics

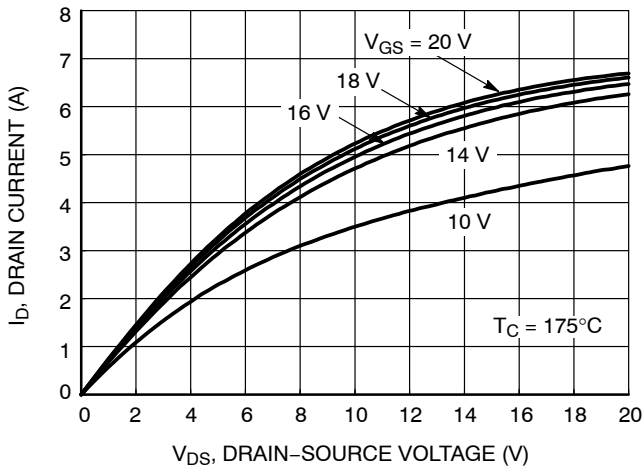


Figure 3. On-Region Characteristics

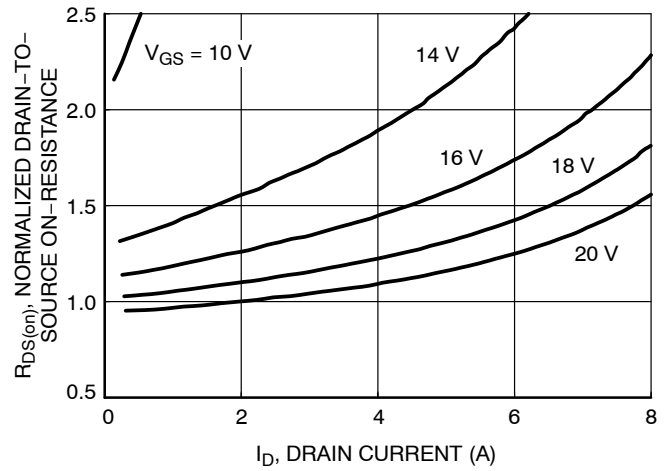


Figure 4. Normalized On-Resistance vs. Drain Current and Gate Voltage

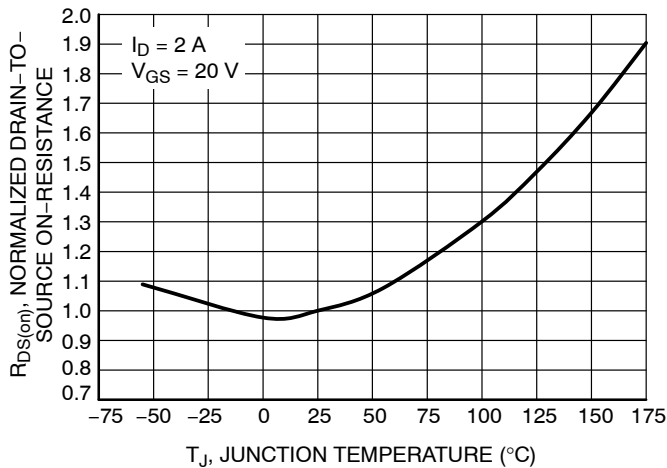


Figure 5. Normalized On-Resistance Variation with Temperature

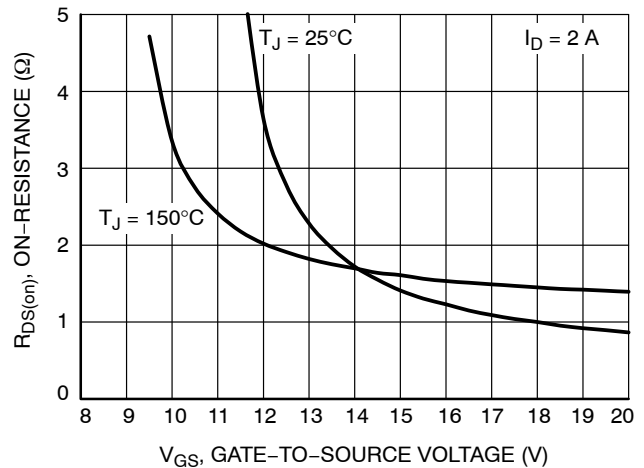


Figure 6. On-Resistance vs. Gate-to-Source Voltage

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## TYPICAL CHARACTERISTICS

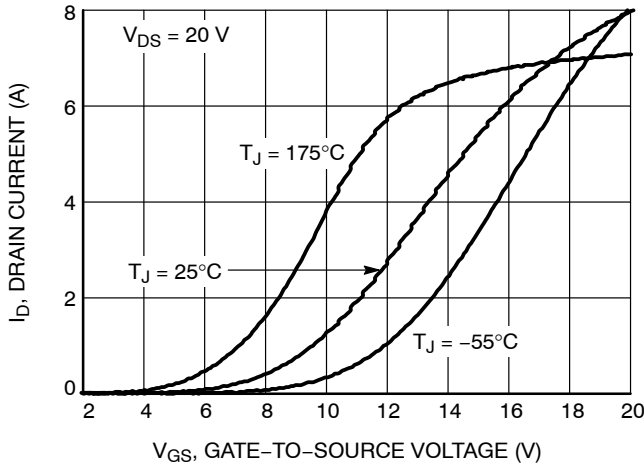


Figure 7. Transfer Characteristics

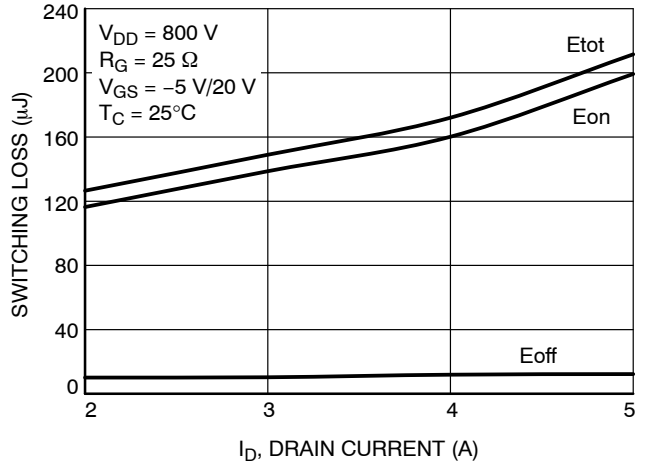


Figure 8. Switching Loss vs. Drain Current

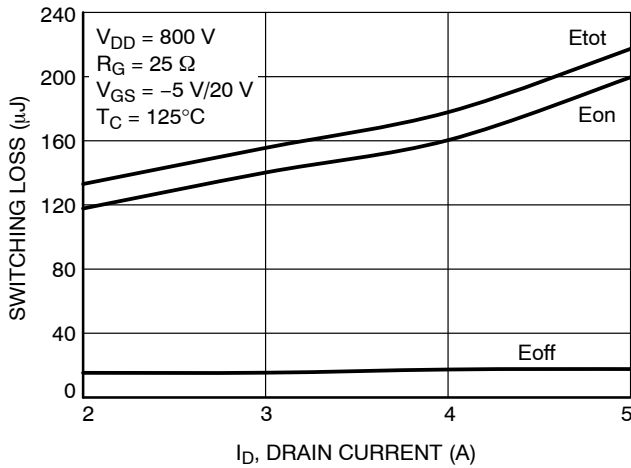


Figure 9. Switching Loss vs. Drain Current

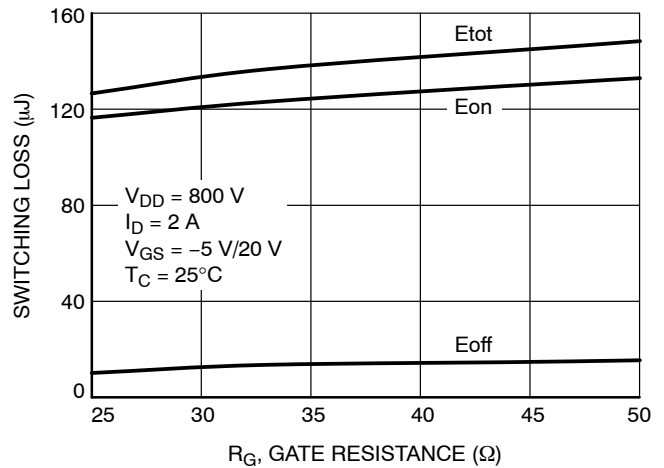


Figure 10. Switching Loss vs. Gate Resistance

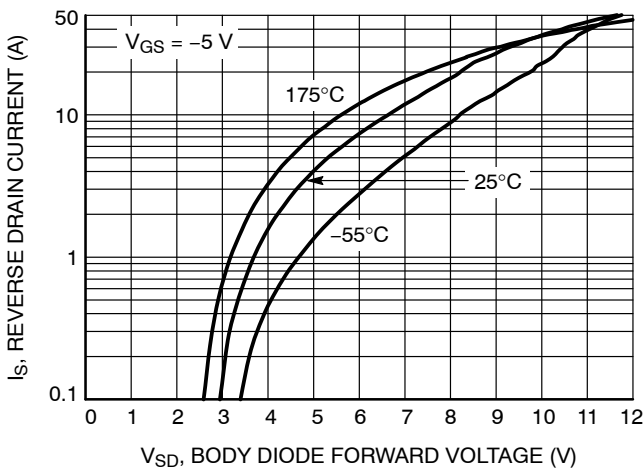


Figure 11. Reverse Drain Current vs. Body Diode Forward Voltage

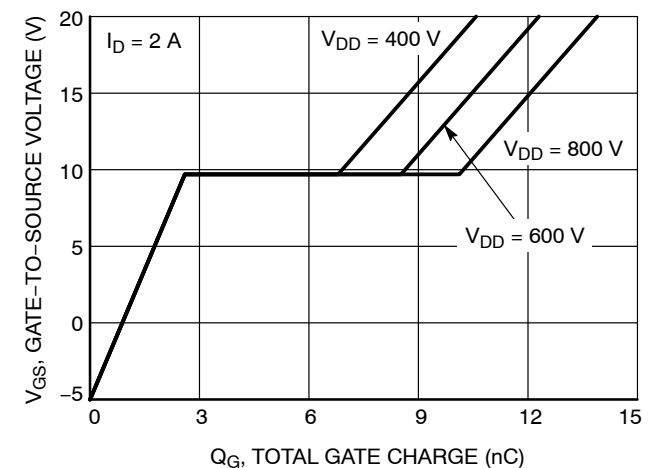
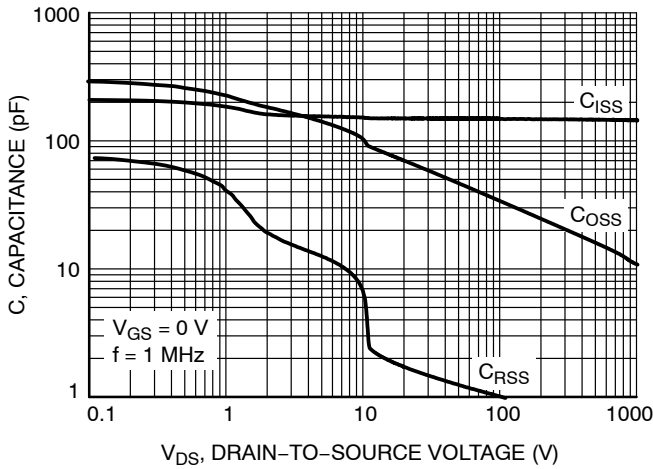


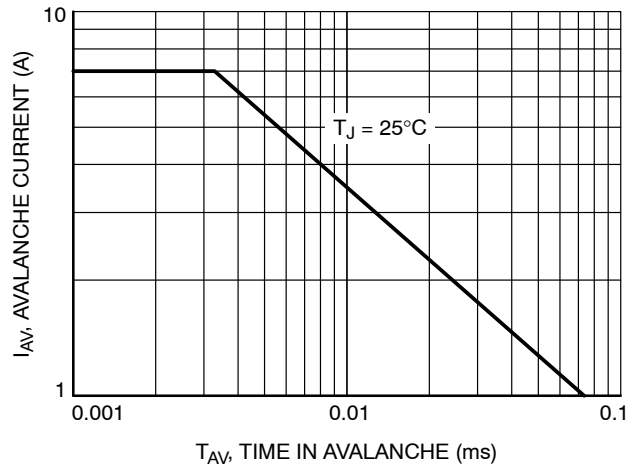
Figure 12. Gate-to-Source Voltage vs. Total Gate Charge

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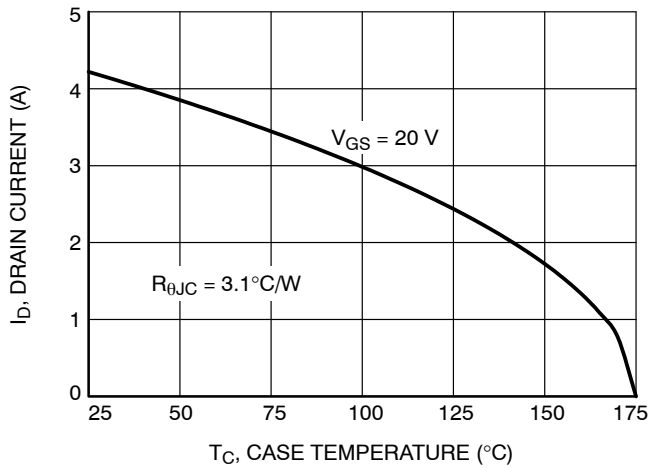
## TYPICAL CHARACTERISTICS



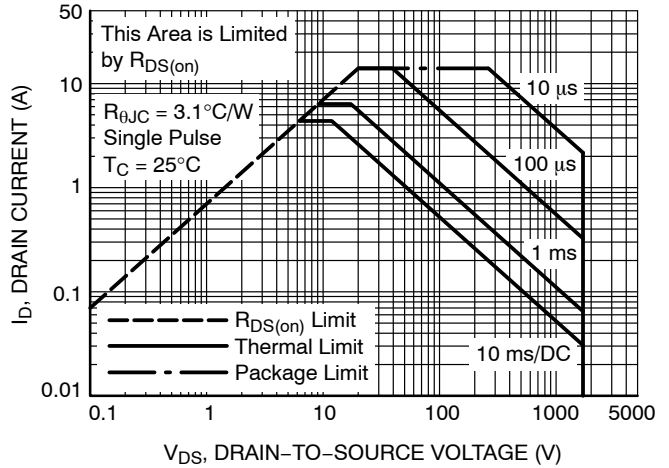
**Figure 13. Capacitance vs. Drain-to-Source Voltage**



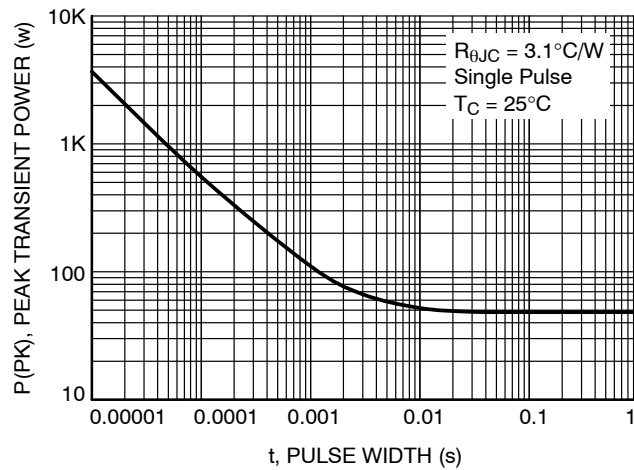
**Figure 14. Unclamped Inductive Switching Capability**



**Figure 15. Maximum Continuous Drain Current vs. Case Temperature**

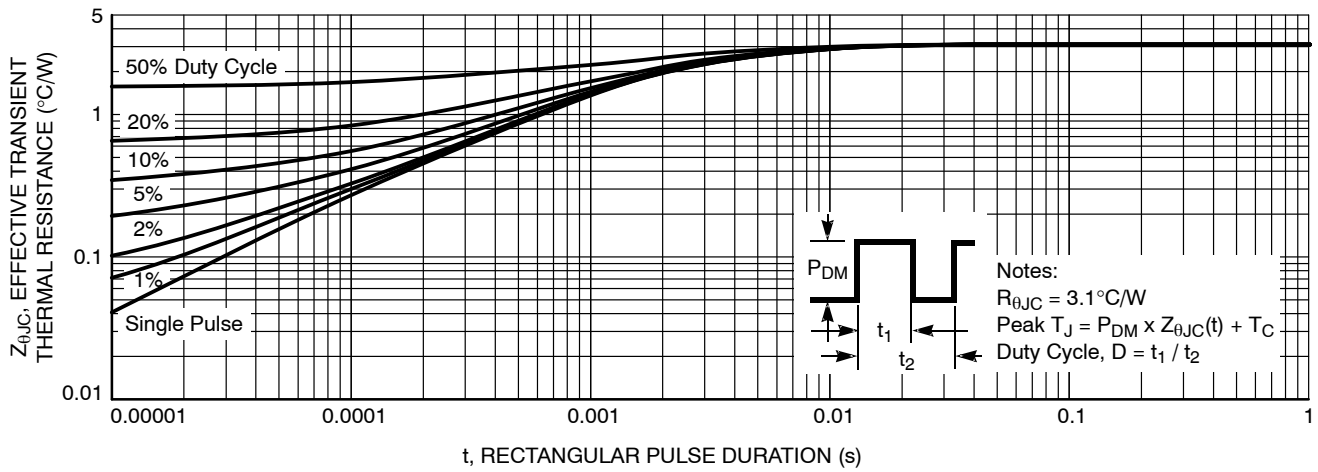


**Figure 16. Maximum Rated Forward Biased Safe Operating Area**



**Figure 17. Single Pulse Maximum Power Dissipation**

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**Figure 18. Transient Thermal Impedance**

## ESD RATINGS

ESD Test	Classification	Standard
ESD-HBM	0B (125 V to <250 V)	ANSI/ESDA/JEDEC JS-001
ESD-CDM	C3 (>1000 V)	ANSI/ESDA/JEDEC JS-002

# MECHANICAL CASE OUTLINE

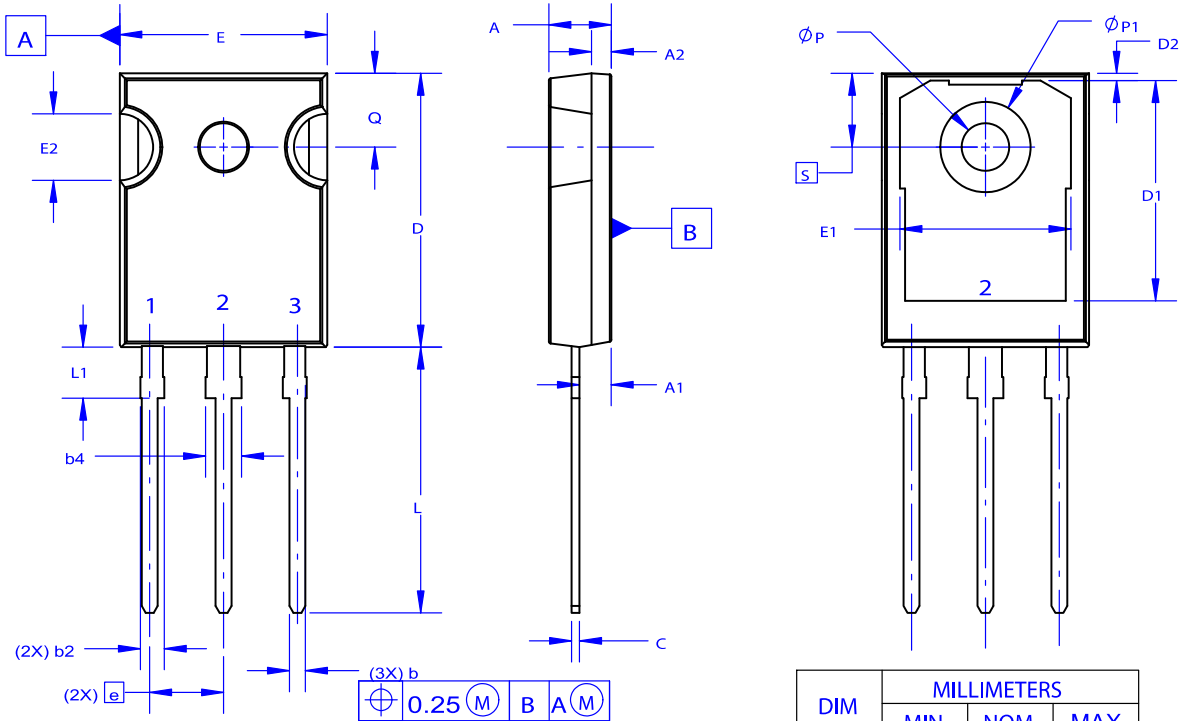
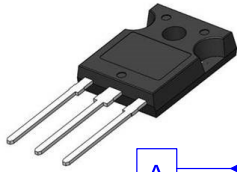
## PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-3LD  
CASE 340CX  
ISSUE A

DATE 06 JUL 2020



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.60	6.80	7.00

### GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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