

MOSFET – Power, N-Channel, SUPERFET® III, Automotive, Easy-Drive

650 V, 65 A, 40 mΩ

NVHL040N65S3

Description

SUPERFET III MOSFET is onsemi's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET Easy drive series helps manage EMI issues and allows for easier design implementation.

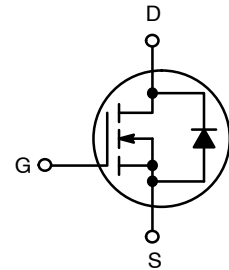
Features

- AEC-Q101 Qualified
- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 35.4\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 136\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 1154\text{ pF}$)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

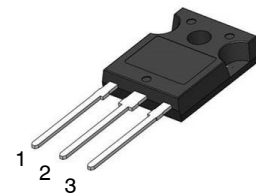
Applications

- Automotive On Board Charger
- Automotive DC/DC Converter for HEV

V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	40 mΩ @ 10 V	65 A

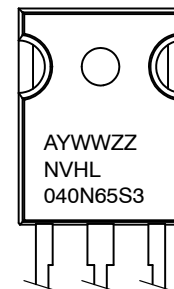


POWER MOSFET



TO-247-3LD
CASE 340CX

MARKING DIAGRAM



A	= Assembly Site
YWW	= Date Code (Year & Week)
ZZ	= Assembly Lot Number
NVHL040N65S3	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

NVHL040N65S3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V _{DSS}	Drain to Source Voltage		650	V
V _{GSS}	Gate to Source Voltage	– DC	±30	V
		– AC (f > 1 Hz)	±30	
I _D	Drain Current	– Continuous (T _C = 25 °C)	65	A
		– Continuous (T _C = 100 °C)	41	
I _{DM}	Drain Current	– Pulsed (Note 1)	162.5	A
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		358	mJ
I _{AS}	Avalanche Current (Note 2)		8.1	A
E _{AR}	Repetitive Avalanche Energy (Note 1)		4.17	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P _D	Power Dissipation	(T _C = 25 °C)	417	W
		– Derate Above 25 °C	3.33	
T _J , T _{STG}	Operating and Storage Temperature Range		–55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse width limited by maximum junction temperature.

2. I_{AS} = 8.1 A, R_G = 25 Ω, starting T_J = 25 °C.

3. I_{SD} ≤ 32.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25 °C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.3	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40	

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25 °C	650	–	–	V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150 °C	700	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25 °C	–	0.64	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 520 V, T _C = 125 °C	–	4.5	–	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 1.7 mA	2.5	–	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 32.5 A	–	35.4	40	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 32.5 A	–	46	–	S



NVHL040N65S3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	–	4740	–	pF
C_{oss}	Output Capacitance		–	120	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to }400\text{ V}, V_{GS} = 0\text{ V}$	–	1154	–	pF
$C_{oss(er.)}$	Energy Related Output Capacitance	$V_{DS} = 0\text{ V to }400\text{ V}, V_{GS} = 0\text{ V}$	–	171	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DS} = 400\text{ V}, I_D = 32.5\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	–	136	–	nC
Q_{gs}	Gate to Source Gate Charge		–	33	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	59	–	nC
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	–	0.7	–	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 32.5\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 3.3\text{ }\Omega$ (Note 4)	–	35	–	ns
t_r	Turn-On Rise Time		–	51	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	95	–	ns
t_f	Turn-Off Fall Time		–	30	–	ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain to Source Diode Forward Current		–	–	65	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	162.5	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 32.5 A	–	–	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 32.5 A, dI _F /dt = 100 A/μs	–	534	–	ns
Q _{rr}	Reverse Recovery Charge		–	13.6	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NVHL040N65S3	NVHL040N65S3	TO-247 G03	Tube	N/A	N/A	30 Units



TYPICAL PERFORMANCE CHARACTERISTICS

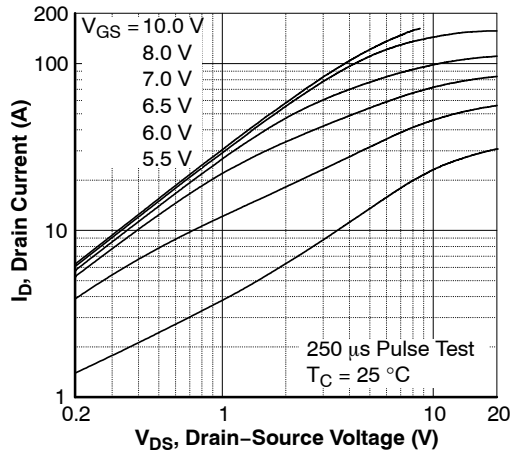


Figure 1. On-Region Characteristics 25°C

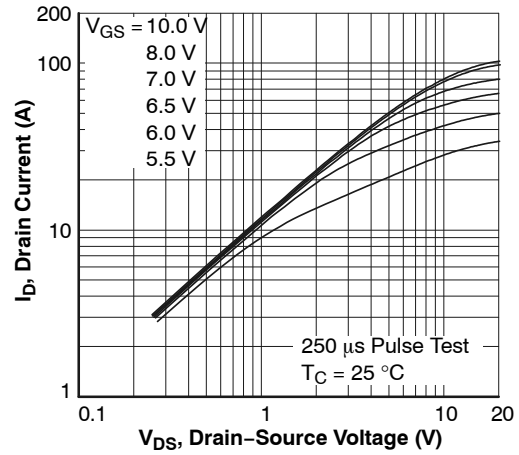


Figure 2. On-Region Characteristics 150°C

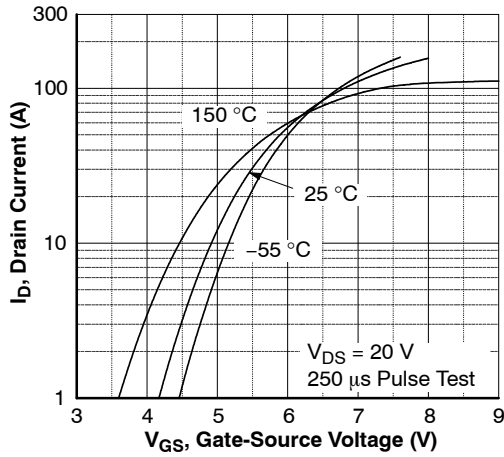


Figure 3. Transfer Characteristics

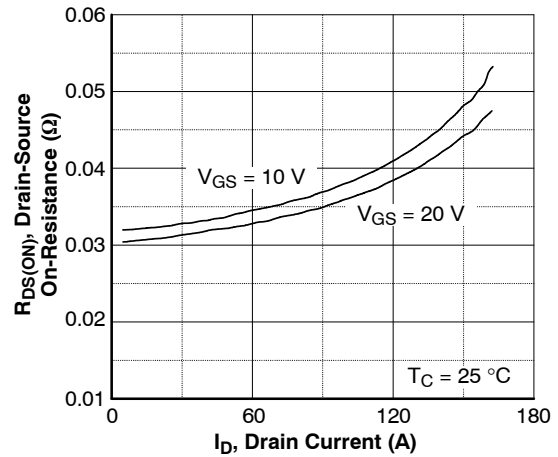


Figure 4. On-Resistance Variation vs. Drain Current and Gate Voltage

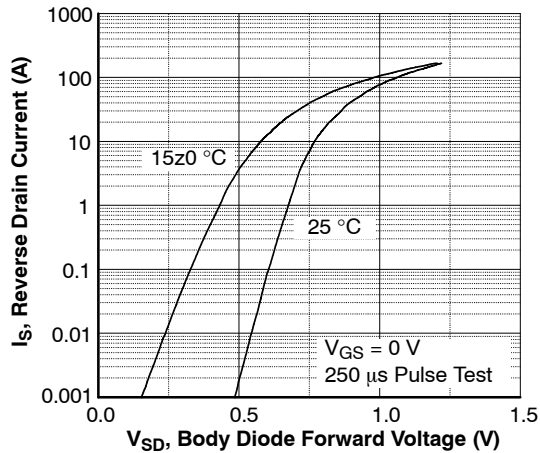


Figure 5. Body Diode Forward Voltage Variation vs. Source Current and Temperature

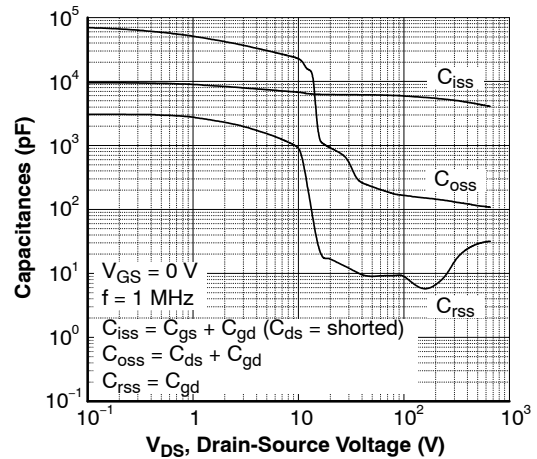


Figure 6. Capacitance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

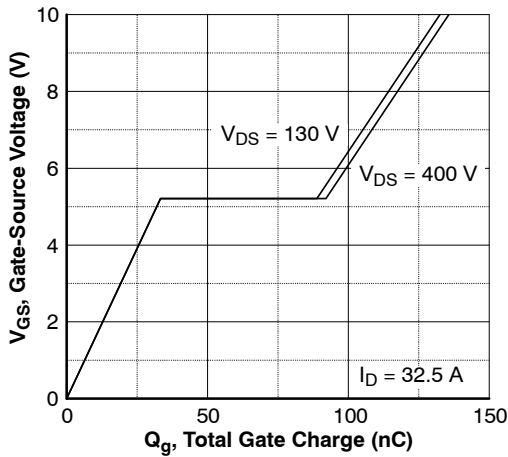


Figure 7. Gate Charge Characteristics

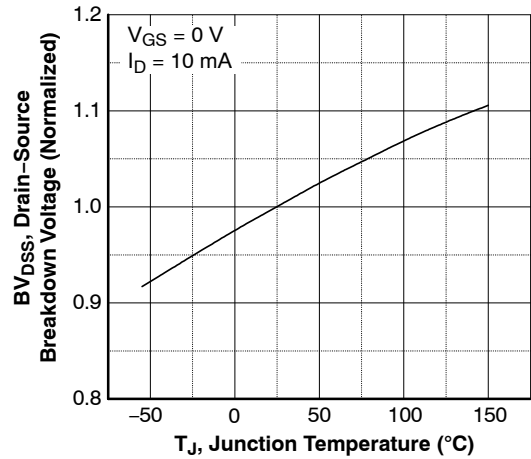


Figure 8. Breakdown Voltage Variation vs. Temperature

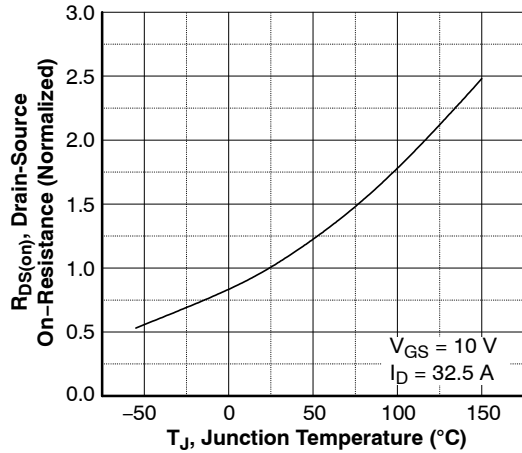


Figure 9. On-Resistance Variation vs. Temperature

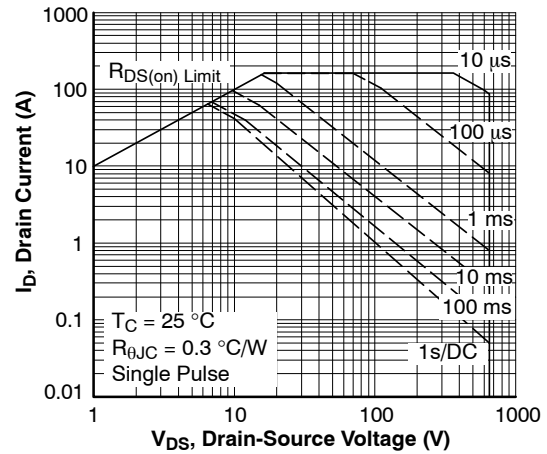


Figure 10. Maximum Safe Operating Area

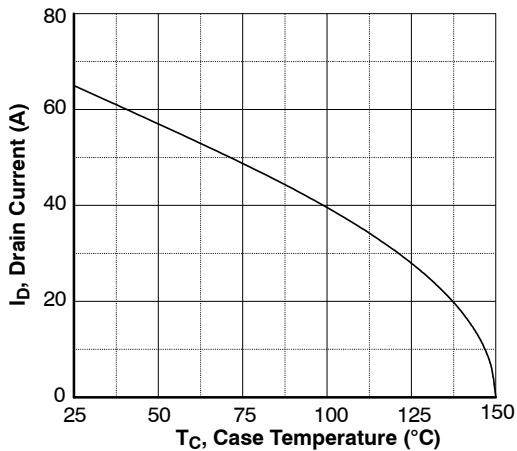


Figure 11. Maximum Drain Current vs. Case Temperature

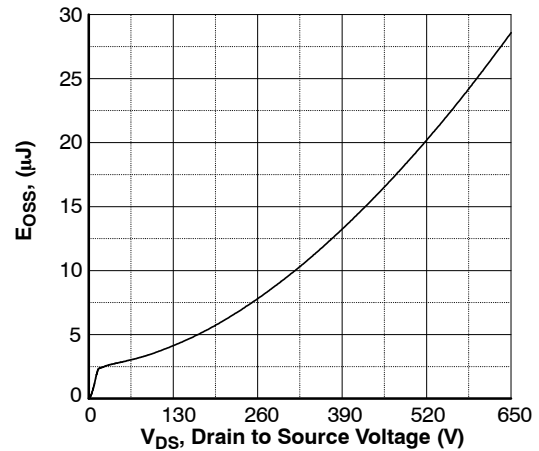


Figure 12. E_{OSS} vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

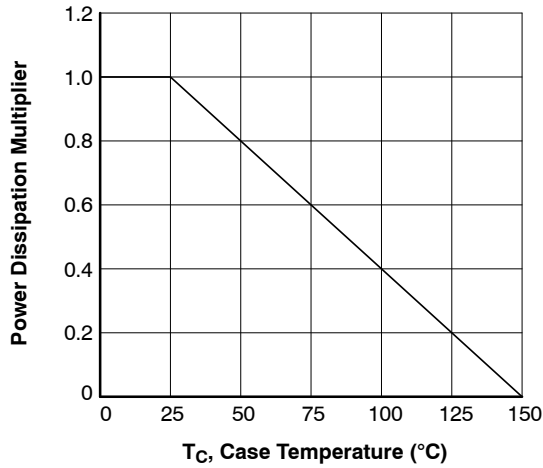


Figure 13. Normalized Power Dissipation vs. Case Temperature

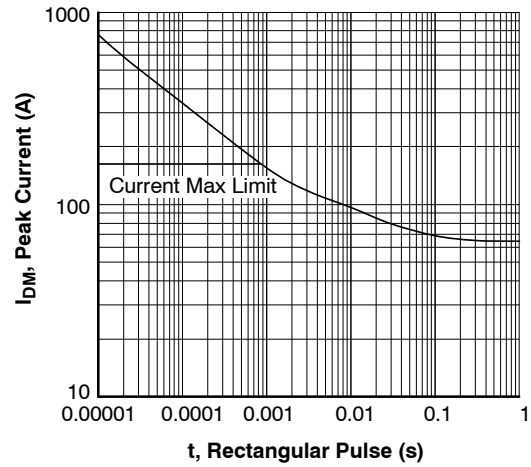


Figure 14. Peak Current Capability

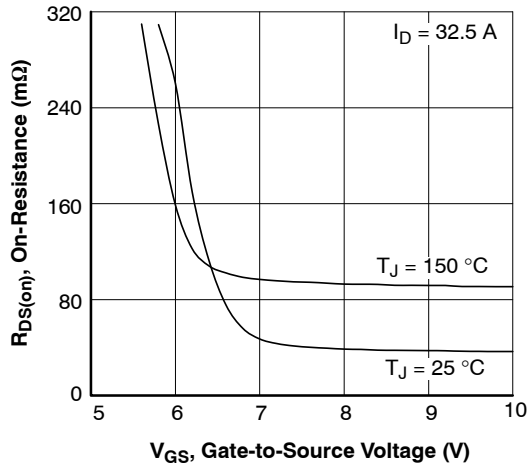


Figure 15. $R_{DS(on)}$ vs. Gate Voltage

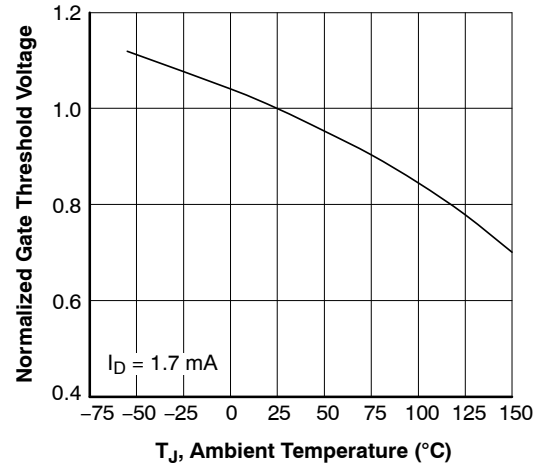


Figure 16. Normalized Gate Threshold Voltage vs. Temperature

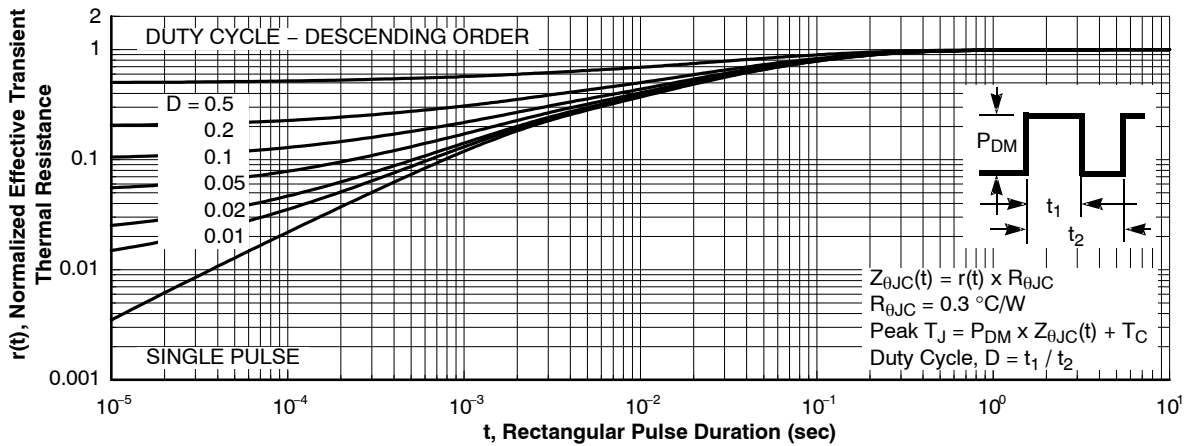


Figure 17. Transient Thermal Response Curve



Figure 18. Gate Charge Test Circuit & Waveform

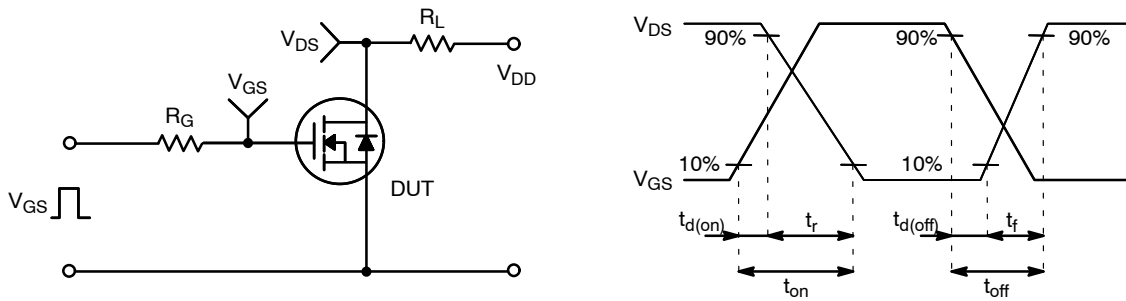


Figure 19. Resistive Switching Test Circuit & Waveforms

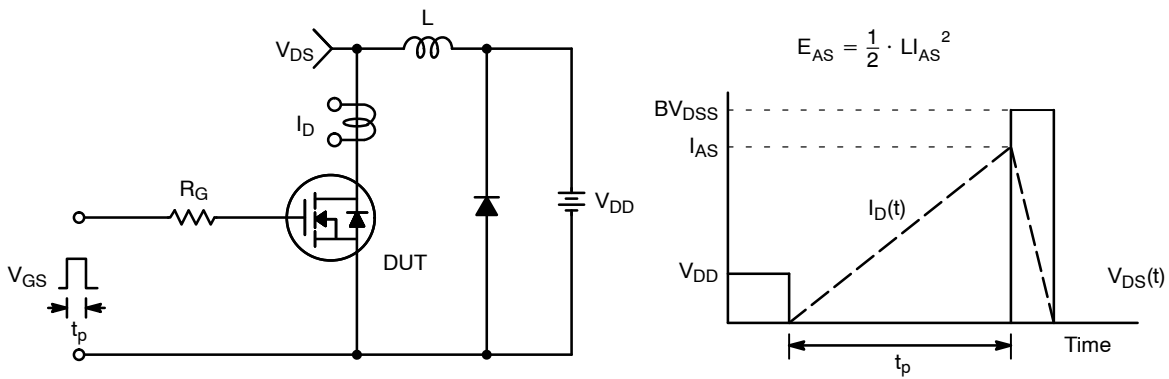


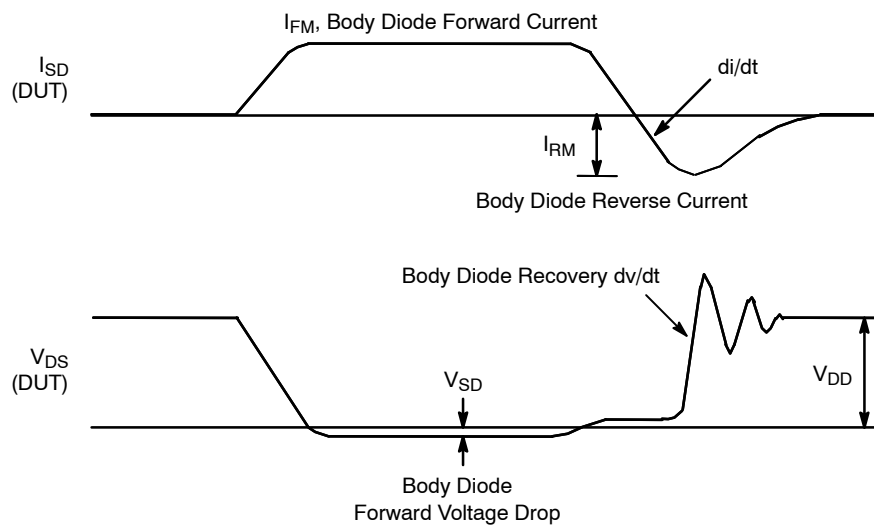
Figure 20. Unclamped Inductive Switching Test Circuit & Waveforms

The diagram shows a switching circuit. A MOSFET labeled 'DUT' has its drain connected to a positive terminal (+) and its source connected to a negative terminal (-). The drain-source voltage is labeled V_{DS} . A current source I_{SD} is connected between the negative terminal and ground. A MOSFET labeled 'Driver' is connected to the negative terminal of the DUT. The gate of the Driver MOSFET is connected to a pulse source V_{GS} through a resistor R_G . The drain of the Driver MOSFET is connected to the negative terminal of the DUT. The source of the Driver MOSFET is connected to ground. A load inductor L is connected between the negative terminal of the DUT and a positive supply V_{DD} . The positive terminal of the DUT is also connected to V_{DD} . Text at the bottom right states:
 - dv/dt controlled by R_G
 - I_{SD} controlled by pulse period

V_{GS}
(Driver)

$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$

10 V



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REVISION HISTORY

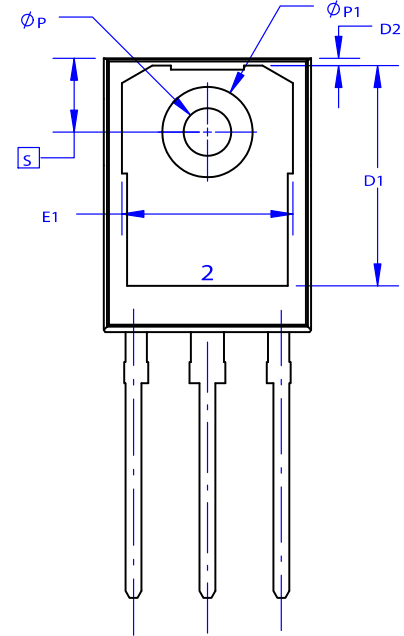
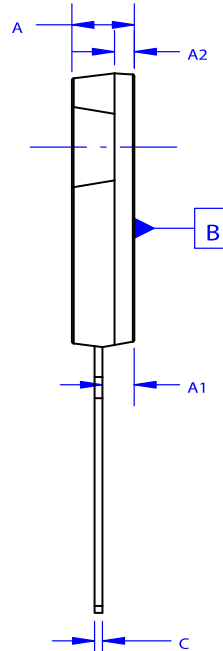
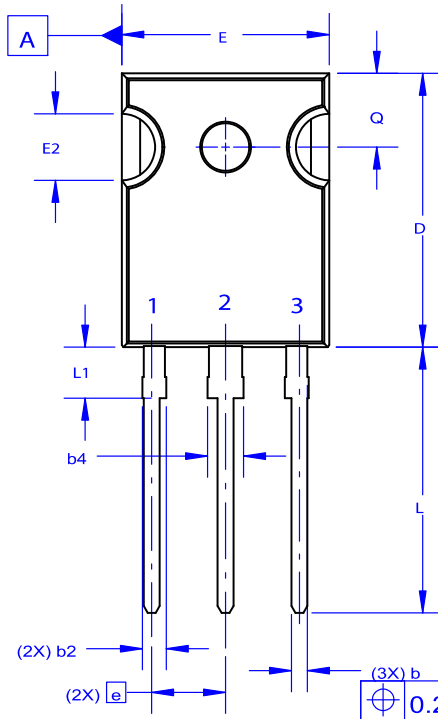
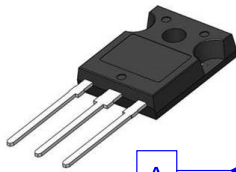
Revision	Description of Changes	Date
1	Rebranded the Data Sheet to onsemi format.	10/15/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



TO-247-3LD
CASE 340CX
ISSUE A

DATE 06 JUL 2020



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC
MARKING DIAGRAM*


XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.60	6.80	7.00

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DESCRIPTION:	TO-247-3LD	PAGE 1 OF 1

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