# ESD Protection Diode

## 27 V Dual Line Automotive Bus Protector

# NUP2125, SZNUP2125

The SZ/NUP2125 has been designed to protect both CAN and LIN transceivers from ESD and other harmful transient voltage events. This device provides bidirectional protection for each data line with a single compact SC-70 (SOT-323) package, giving the system designer a low cost option for improving system reliability and meeting stringent EMI requirements.

### Features

- 200 W Peak Power Dissipation per Line (8/20 μs Waveform)
- Diode Capacitance Matching
- Low Reverse Leakage Current (< 100 nA)
- IEC Compatibility: – IEC 61000-4-2 (ESD): Level 4
  – IEC 61000-4-4 (EFT): 50 A – 5/50 ns
  – IEC 61000-4-5 (Lighting) 3.0 A (8/20 μs)
- ISO 7637-1, Nonrepetitive EMI Surge Pulse 2, 8.0 A (1/50 μs)
- ISO 7637-3, Repetitive Electrical Fast Transient (EFT) EMI Surge Pulses, 50 A (5/50 ns)
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices

### Applications

- Automotive Networks
  - CAN / CAN-FD
  - Low and High-Speed CAN
  - Fault Tolerant CAN
  - LIN

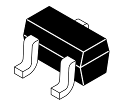
**MAXIMUM RATINGS** ($T_A$ = 25 °C unless otherwise noted)

| Symbol | Rating | Max | Unit |
|---|---|---|---|
| PPK | Peak Power Dissipation, 8/20 μs Double Exponential Waveform (Note 1) | 200 | W |
| $T_J$, $T_{stg}$ | Junction and Storage Temperature Range | −55 to +175 | °C |
| $T_L$ | Lead Solder Temperature (10 s) | 260 | °C |
| ESD | Human Body Model (HBM)<br>Machine Model (MM)<br>IEC 61000-4-2 Contact<br>IEC 61000-4-2 Air<br>ISO 10605 Contact (330 pF / 330 Ω)<br>ISO 10605 Contact (330 pF / 2 kΩ)<br>ISO 10605 Contact (150 pF / 2 kΩ) | ±8.0<br>±1.6<br>±30<br>±30<br>±30<br>±30<br>±30 | kV<br>kV<br>kV<br>kV<br>kV<br>kV<br>kV |
| $I_{PP}$ | Maximum Peak Pulse Current, 8/20 μs | 3 | A |

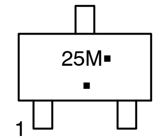
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Non-repetitive current pulse per Figure 1.

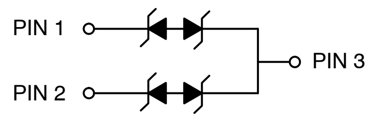
**MARKING DIAGRAM**

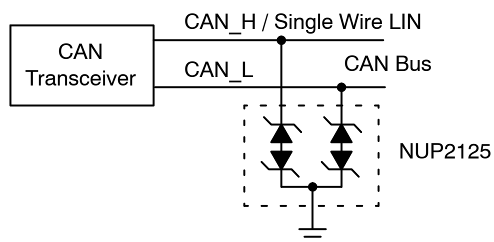


SC-70
CASE 419




25 = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)




### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NUP2125WTT1G | SC-70 (Pb-Free) | 3000 / Tape & Reel |
| SZNUP2125WTT1G* | SC-70 (Pb-Free) | 3000 / Tape & Reel |
| NUP2125WTT3G | SC-70 (Pb-Free) | 10000 / Tape & Reel |
| SZNUP2125WTT3G* | SC-70 (Pb-Free) | 10000 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

* SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

### ELECTRICAL CHARACTERISTICS

($T_A$ = 25 °C unless otherwise noted)

| Symbol | Parameter |
|---|---|
| $I_{PP}$ | Maximum Reverse Peak Pulse Current |
| $V_C$ | Clamping Voltage @ $I_{PP}$ |
| $V_{RWM}$ | Working Peak Reverse Voltage |
| $I_R$ | Maximum Reverse Leakage Current @ $V_{RWM}$ |
| $V_{BR}$ | Breakdown Voltage @ $I_T$ |
| $I_T$ | Test Current |

*See Application Note AND8308/D for detailed explanations of data sheet parameters.

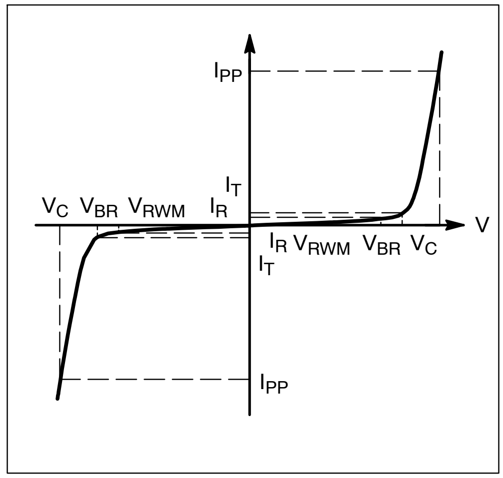



**Figure 1. Bi-Directional**

### ELECTRICAL CHARACTERISTICS ($T_J$ = 25 °C, unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{RWM}$ | Reverse Working Voltage | (Note 2) | 24 | – | – | V |
| $V_{BR}$ | Breakdown Voltage | $I_T$ = 1 mA (Note 3) | 27 | 28.5 | 32 | V |
| $I_R$ | Reverse Leakage Current | $V_{RWM}$ = 24 V | – | 15 | 100 | nA |
| $V_C$ | Clamping Voltage | IEC61000-4-2, +/− 8 kV Contact | See Figures 8–9 | | | |
| $V_C$ | Clamping Voltage<br>TLP<br>(See Figures 12–13)<br>(Note 6) | ITLP = 4 A<br>ITLP = 8 A<br>ITLP = 16 A<br>ITLP = 20 A | –<br>–<br>–<br>– | 42<br>43<br>56<br>69 | –<br>–<br>–<br>– | V |
| $V_C$ | Clamping Voltage<br>8/20 s Waveform<br>(See Figures 6–7) | IPP = 1 A<br>IPP = 13 A | –<br>– | 33.4<br>44.0 | 36.6<br>50.0 | V |
| Rdyn | Dynamic Resistance | TLP Pulse | – | 0.94 | – | Ω |
| $C_J$ | Capacitance | $V_R$ = 0 V, f = 1 MHz (Line to GND) | – | 7.0 | 10 | pF |
| | | $V_R$ = 5 V, f = 1 MHz (Line to GND) | – | 4.5 | 6.0 | pF |
| | | $V_R$ = 5 V, f = 1 MHz (Line to GND),<br>$T_A$ = +150 °C | – | 5.0 | – | pF |
| ΔC | Diode Capacitance Matching | $V_R$ = 0 V, 5 MHz (Note 5) | – | 0.26 | 2 | % |
| $I_L$ | Insertion Loss | f = 1 GHz<br>f = 5 GHz | – | 8.7<br>1.7 | – | dB |
| $R_L$ | Return Loss | f = 1 GHz<br>f = 5 GHz | – | 1.5<br>1.0 | – | dB |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Surge protection devices are normally selected according to the working peak reverse voltage ($V_{RWM}$), which should be equal or greater than the DC or continuous peak operating voltage level.
3. $V_{BR}$ is measured at pulse test current $I_T$.
4. Pulse waveform per Figure 6.
5. ΔC is the percentage difference between $C_J$ of lines 1 and 2 measured according to the test conditions given in the electrical characteristics table.
6. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 4 ns, averaging window; $t_1$ = 30 ns to $t_2$ = 60 ns.

## TYPICAL PERFORMANCE CURVES

($T_J$ = 25 °C UNLESS OTHERWISE NOTED)

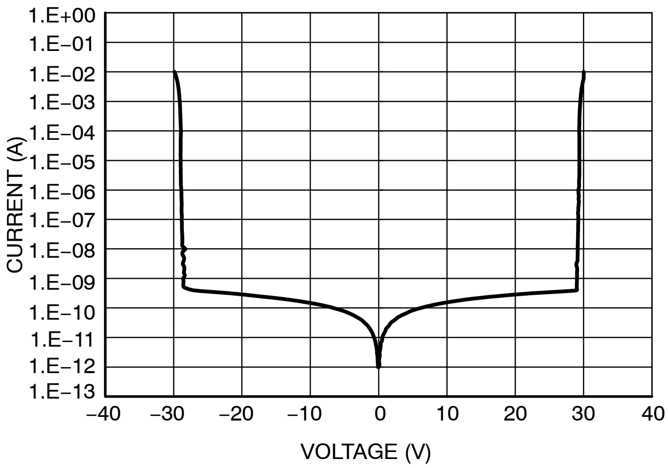



**Figure 2. IV Characteristics**

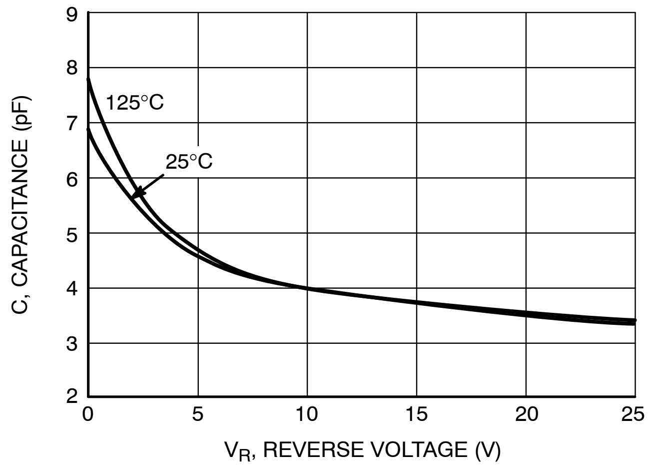



**Figure 3. CV Characteristics**

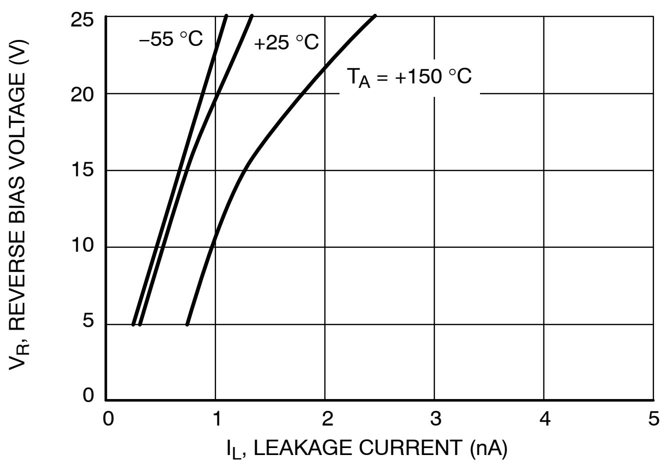



**Figure 4. $I_R$ vs. Temperature Characteristics**

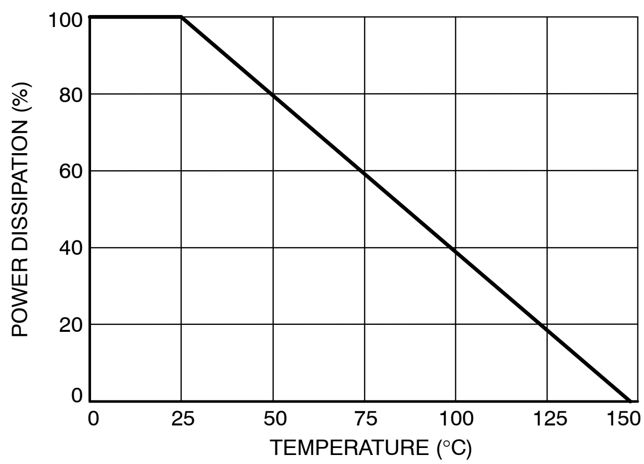



**Figure 5. Steady State Power Derating**

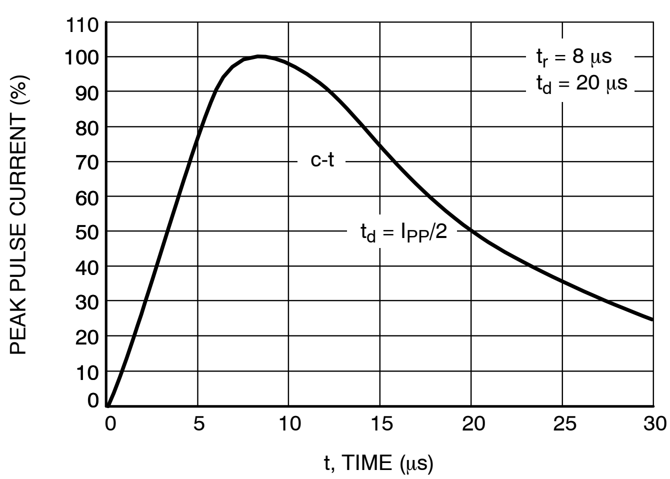



**Figure 6. Pulse Waveform (8/20 µs)**

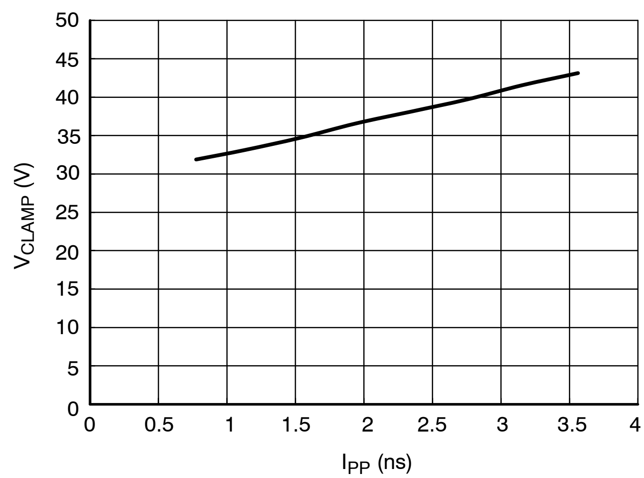



**Figure 7. Clamping Voltage vs. Peak Pulse Current (8/20 µs)**

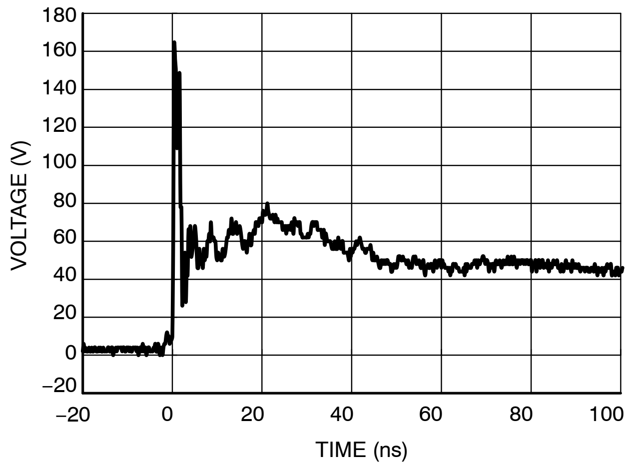



**Figure 8. IEC61000-4-2 +8 kV Contact**

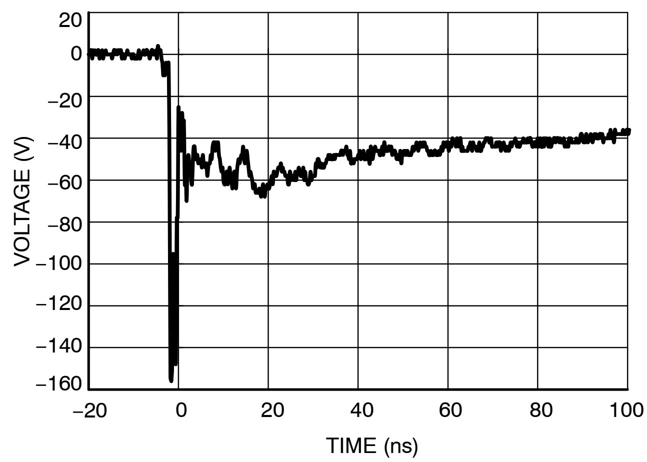



**Figure 9. IEC61000-4-2 −8 kV Contact**

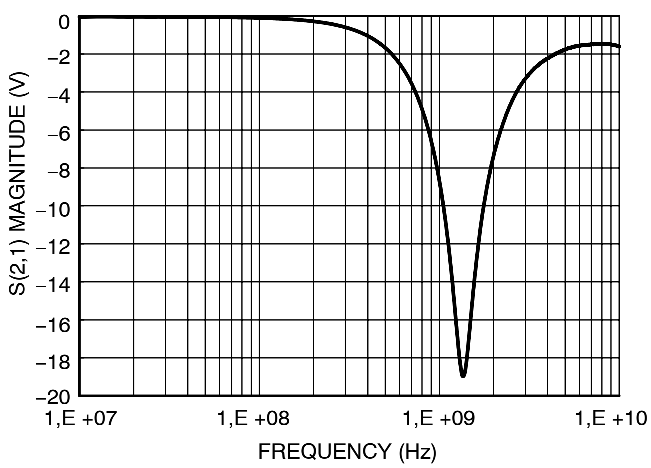



**Figure 10. Typical Insertion Loss**

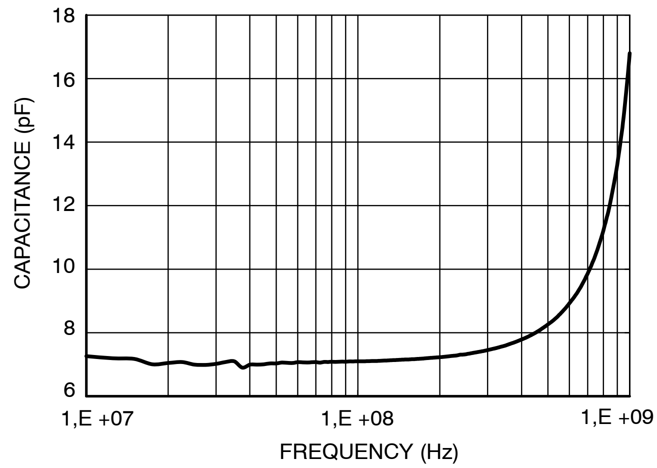



**Figure 11. Typical Capacitance vs. Frequency**

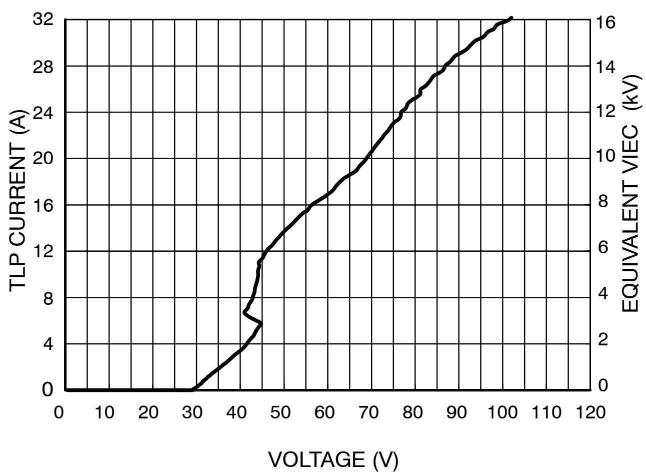



**Figure 12. Positive TLP IV Curve**

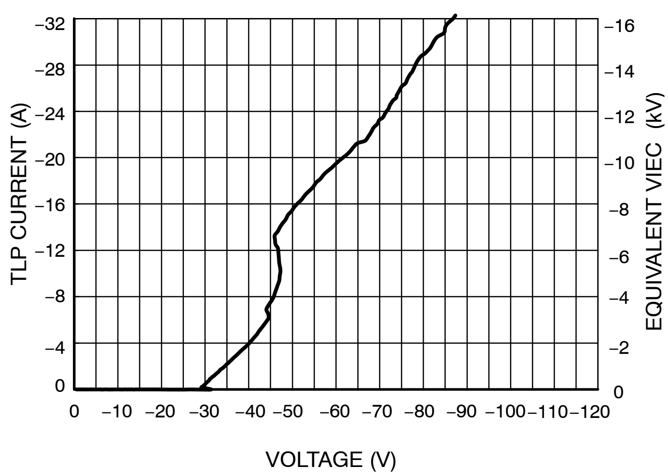



**Figure 13. Negative TLP IV Curve**

### Surge Protection Diode Circuit

Surge protection diodes provide protection to a transceiver by clamping a surge voltage to a safe level. Surge protection diodes have high impedance below and low impedance above their breakdown voltage. A surge protection Zener diode has its junction optimized to absorb the high peak energy of a transient event, while a standard Zener diode is designed and specified to clamp a steady state voltage.

Figure 14 provides an example of a dual bidirectional surge protection diode array that can be used for protection with the high-speed CAN network. The bidirectional array is created from four identical Zener TVS diodes. The clamping voltage of the composite device is equal to the breakdown voltage of the diode that is reversed biased, plus the diode drop of the second diode that is forwarded biased.

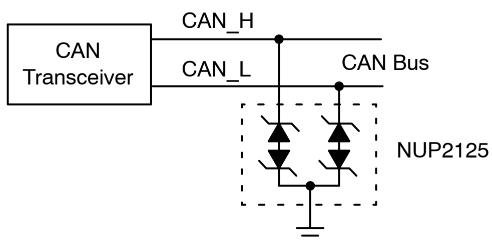



**Figure 14. High-Speed and Fault Tolerant CAN Surge Protection Circuit**

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how creates these screenshots and how to interpret them please refer to AND8307/D.

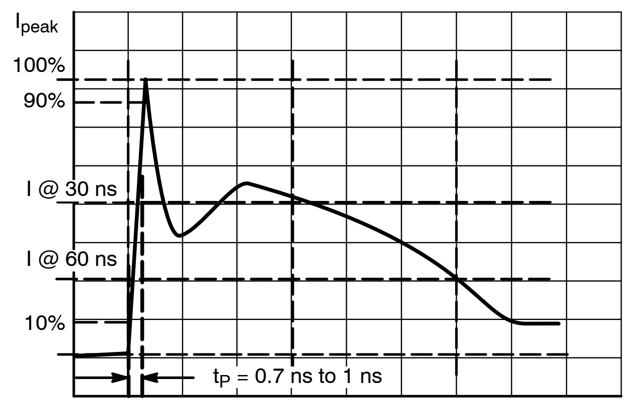



**Figure 15. IEC61000-4-2 Current Waveform**

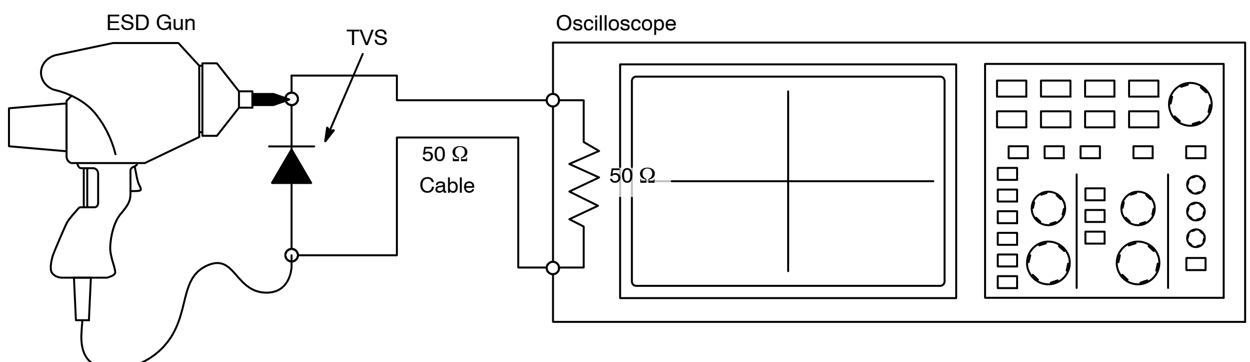



**Figure 16. Diagram of ESD Clamping Voltage Test Setup**

**Transmission Line Pulse (TLP) Measurement**

TLP provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 17. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 18 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

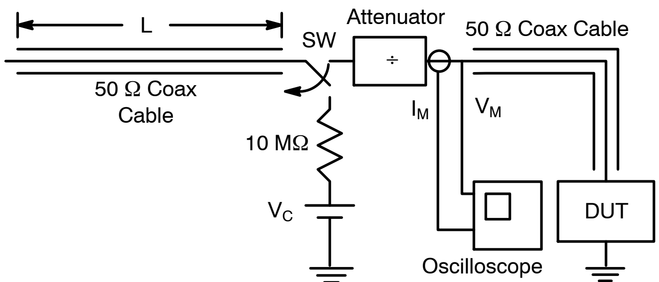



**Figure 17. Basic TLP System**

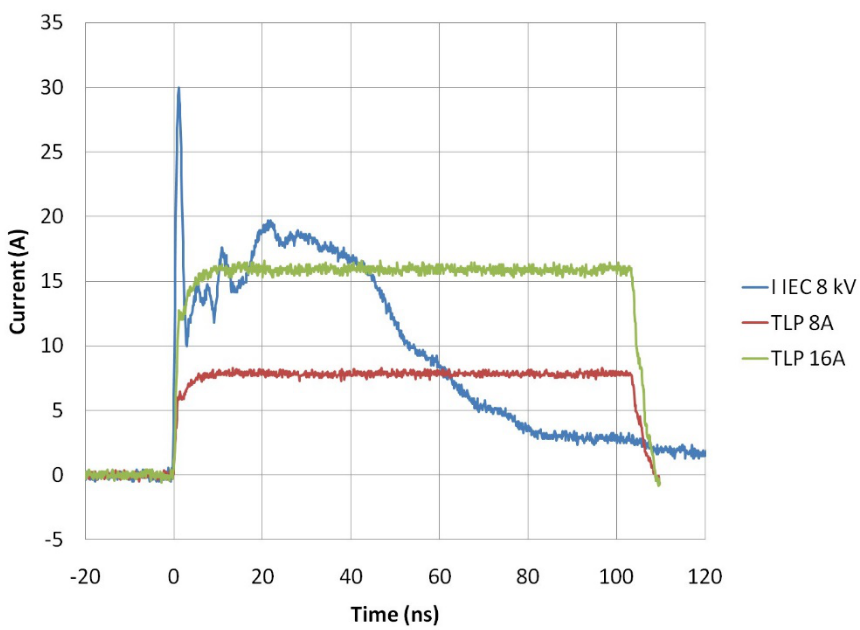



**Figure 18. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms**

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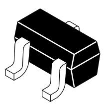
DeviceNet is a trademark of Rockwell Automation.

## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| 9 | Updated document layout to align with NUP2205/D, including removal of Flammability Rating from page 1 and relocation of Ordering Information to page 1. Revised and expanded Maximum Ratings and Electrical Characteristics tables (added Rdyn, IL, RL; updated TLP data). Updated figure titles and replaced selected plots with data derived from the provided Excel files. Added IEC/ISO test conditions, updated clamping-voltage values, and introduced extended characterization sections (IEC ESD ±8 kV, TLP curves, insertion loss, capacitance vs. frequency). Performed structural cleanup, removed obsolete content, aligned terminology, corrected IL and RL sign convention, and updated Figures 10 and 11. | 5/7/2026 |

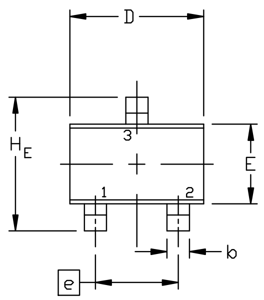
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



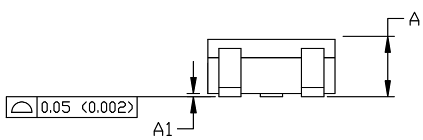
**SCALE 4:1**

**SC−70 (SOT−323)**
CASE 419
ISSUE R

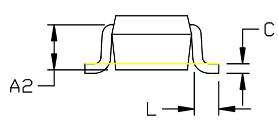
DATE 11 OCT 2022




TOP VIEW



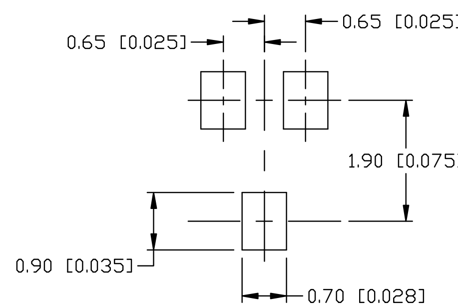

SIDE VIEW




END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH

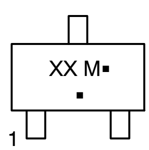
| DIM | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.80 | 0.90 | 1.00 | 0.032 | 0.035 | 0.040 |
| A1 | 0.00 | 0.05 | 0.10 | 0.000 | 0.002 | 0.004 |
| A2 | 0.70 REF | | | 0.028 BSC | | |
| b | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| c | 0.10 | 0.18 | 0.25 | 0.004 | 0.007 | 0.010 |
| D | 1.80 | 2.00 | 2.20 | 0.071 | 0.080 | 0.087 |
| E | 1.15 | 1.24 | 1.35 | 0.045 | 0.049 | 0.053 |
| e | 1.20 | 1.30 | 1.40 | 0.047 | 0.051 | 0.055 |
| e1 | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.20 | 0.38 | 0.56 | 0.008 | 0.015 | 0.022 |
| $H_E$ | 2.00 | 2.10 | 2.40 | 0.079 | 0.083 | 0.095 |




* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT

**GENERIC**
**MARKING DIAGRAM**




XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
CANCELLED

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE-ANODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE-CATHODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

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|---|---|---|
| DESCRIPTION: | SC−70 (SOT−323) | PAGE 1 OF 1 |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT:** www.onsemi.com/support
**For additional information, please contact your local Sales Representative at**
www.onsemi.com/support/sales

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