

MOSFET – Power, Single N-Channel, DUAL COOL®

40 V, 0.78 mΩ, 310 A

NTMFSC0D8N04XM

Features

- Dual Sided Cooling Package
- Latest 40 V Power MOSFET Technology for Motor Drive Applications
- Extreme Lower On-Resistance to Minimize Conduction Losses
- Lower Gate Charge to Minimize Gate Driving and Switching Losses
- Soft Body Diode Reverse Recovery
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

Applications

- Motor Drive
- ORing FET
- Battery Protection

MAXIMUM RATINGS (T_J = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain-to-Source Voltage	40	V
V _{GS}	Gate-to-Source Voltage	DC ±20	V
I _D	Continuous Drain Current (Note 2)	T _C = 25 °C	310 A
		T _C = 100 °C	219
P _D	Power Dissipation (Note 2)	T _C = 25 °C	135 W
I _{DM}	Pulsed Drain Current	T _C = 25 °C, t _p = 10 μs	1463 A
T _J , T _{stg}	Operating Junction and Storage Temperature Range	-55 to +175	°C
I _S	Continuous Source-Drain Current (Body Diode)	150	A
E _{AS}	Single Pulse Avalanche Energy (I _{PK} = 69 A)	248	mJ
T _L	Lead Temperature Soldering Purposes (1/8" from case for 10 s)	260	°C

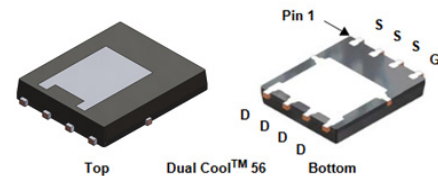
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

THERMAL CHARACTERISTICS

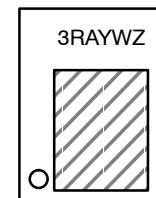
Symbol	Parameter	Max	Unit
R _{θJC}	Junction-to-Case (Bottom) – Steady State (Note 2)	1.1	°C/W
R _{θJC}	Junction-to-Case (Top) – Steady State (Note 2)	1.7	
R _{θJA}	Junction-to-Ambient – Steady State (Notes 1, 2)	39	

V _{(BR)DSS}	R _{DS(ON) MAX}	I _{D MAX}
40 V	0.78 mΩ @ 10 V	310 A



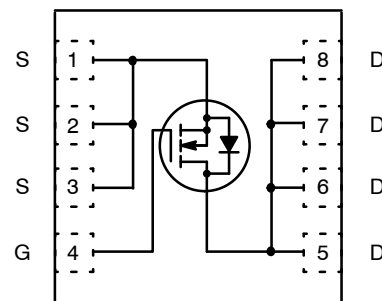
DFN8 5x6
CASE 506EG

MARKING DIAGRAM



- 3R = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- Z = Assembly Lot Code

N-Channel MOSFET



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	40			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}$, Referenced to $25\text{ }^\circ\text{C}$		15		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 40\text{ V}, T_J = 25\text{ }^\circ\text{C}$			10	μA
		$V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$			100	
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 3)

$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		0.63	0.78	$\text{m}\Omega$
		$V_{GS} = 7\text{ V}, I_D = 50\text{ A}$		0.86	1.25	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 180\text{ }\mu\text{A}$	2.5	3.0	3.5	V
$\Delta V_{GS(TH)}/\Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$V_{GS} = V_{DS}, I_D = 180\text{ }\mu\text{A}$		-7		mV/ $^\circ\text{C}$
g_{FS}	Forward Trans-conductance	$V_{DS} = 5\text{ V}, I_D = 50\text{ A}$		244		S

CHARGES & CAPACITANCES

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}, f = 1\text{ MHz}$		4651		pF
C_{OSS}	Output Capacitance			3319		
C_{RSS}	Reverse Transfer Capacitance			69		
Q_{OSS}	Output Charge	$V_{GS} = 10\text{ V}, V_{DD} = 20\text{ V}, I_D = 50\text{ A}$		100		nC
$Q_{G(TOT)}$	Total Gate Charge			72		
$Q_{G(TH)}$	Threshold Gate Charge			14		
Q_{GS}	Gate-to-Source Charge			21		
Q_{GD}	Gate-to-Drain Charge			13		
V_{GP}	Gate Plateau Voltage			4.5		
R_G	Gate Resistance	$f = 1\text{ MHz}$		0.65	1.2	Ω

SWITCHING CHARACTERISTICS (Note 3)

$t_{d(ON)}$	Turn-On Delay Time	Resistive Load $V_{GS} = 0/10\text{ V}, V_{DD} = 20\text{ V},$ $I_D = 50\text{ A}, R_G = 2.5\text{ }\Omega$		28		ns
t_r	Rise Time			10		
$t_{d(OFF)}$	Turn-Off Delay Time			45		
t_f	Fall Time			9.5		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

V_{SD}	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}, T_J = 25\text{ }^\circ\text{C}$		0.81	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 50\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.66	1.0	
t_{RR}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 50\text{ A}, V_{DD} = 50\text{ V}$		69		ns
t_a	Charge Time			36		
t_b	Discharge Time			33		
Q_{RR}	Reverse Recovery Charge			144		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

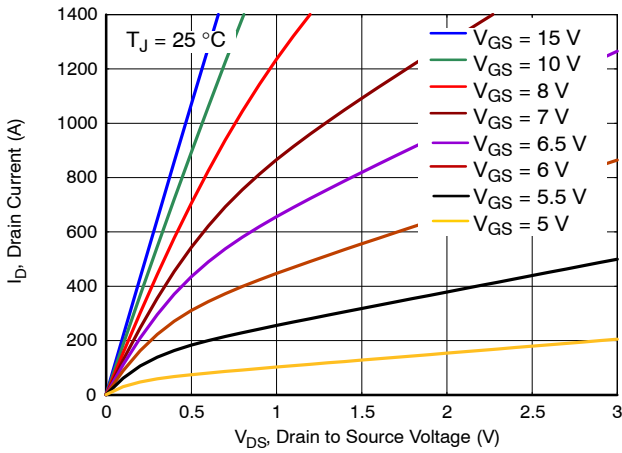


Figure 1. On-Region Characteristics

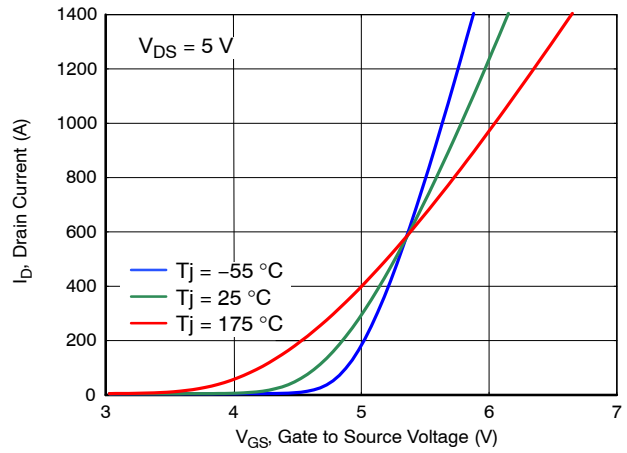


Figure 2. Transfer Characteristics

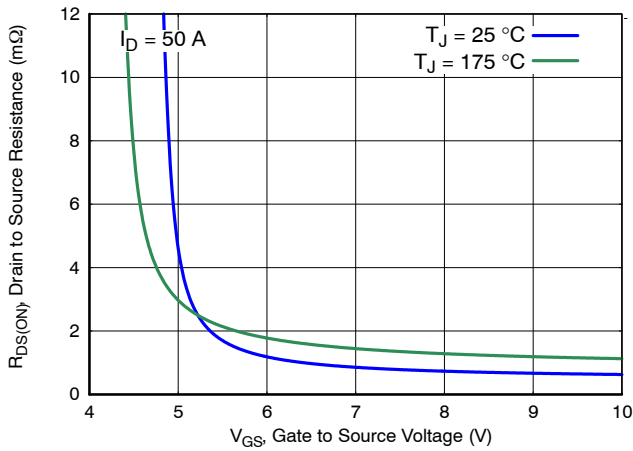


Figure 3. On-Resistance vs. Gate Voltage

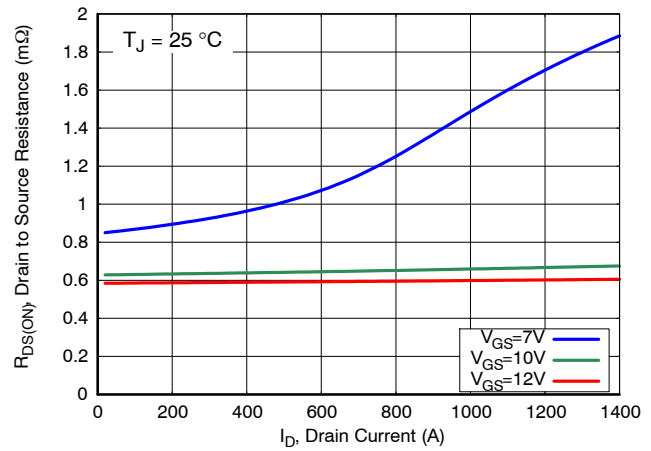


Figure 4. On-Resistance vs. Drain Current

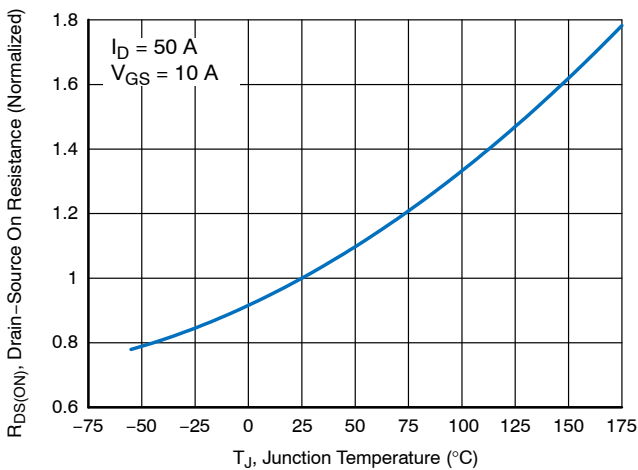


Figure 5. Normalized ON Resistance vs. Junction Temperature

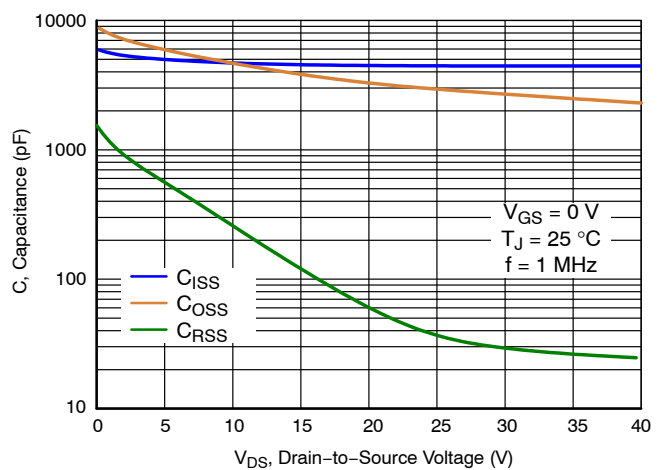


Figure 6. Capacitance Characteristics

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TYPICAL CHARACTERISTICS

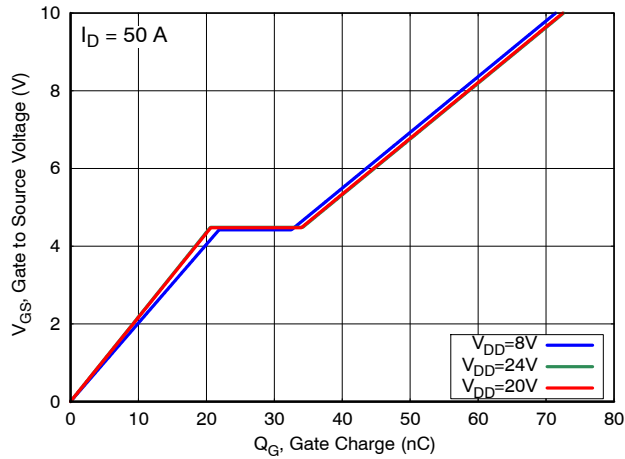


Figure 7. Gate Charge Characteristics

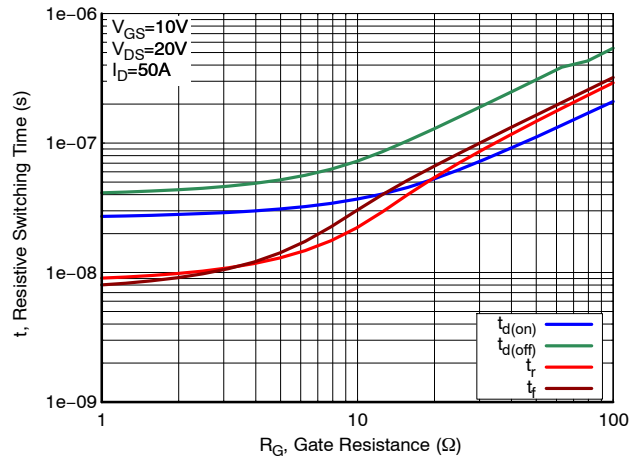


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

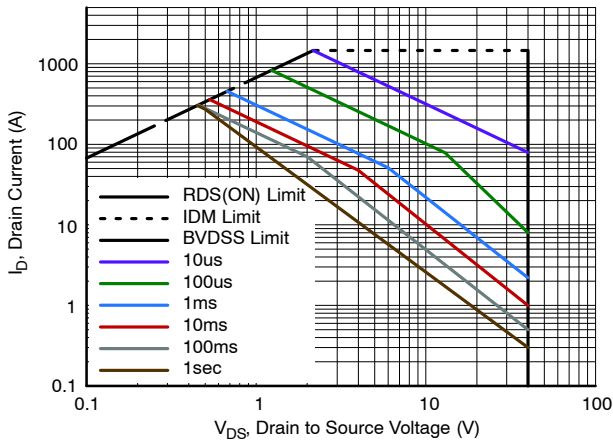


Figure 9. Safe Operating Area (SOA)

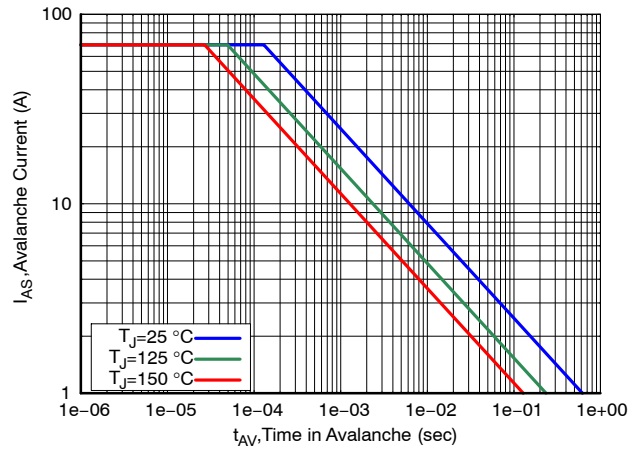


Figure 10. Avalanche Current vs Pulse Time (UIS)

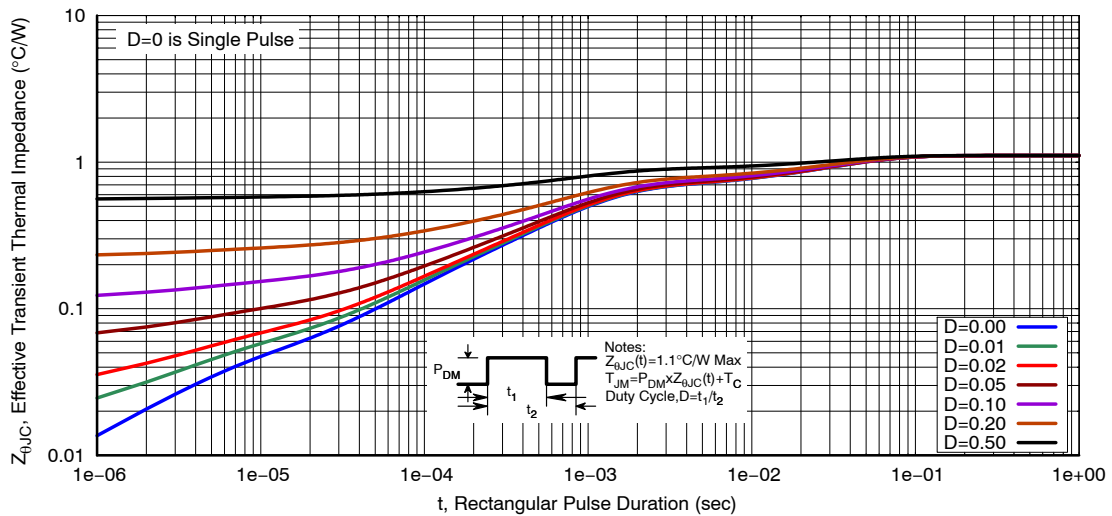


Figure 11. Transient Thermal Response

NTMFSC0D8N04XM

ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSC0D8N04XMTWG	3R	DFN8 5x6 (Pb-Free/Halogen Free)	3,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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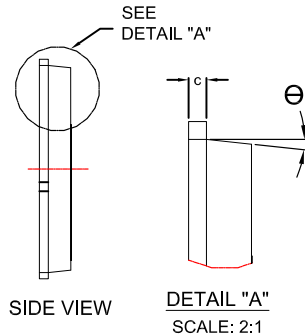
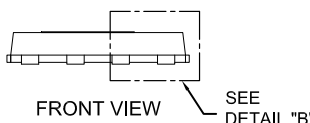
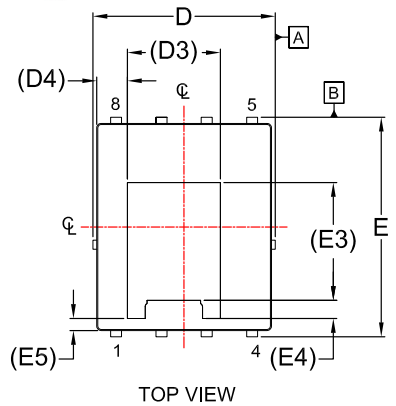
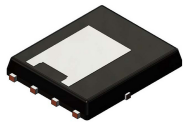
REVISION HISTORY

Revision	Description of Changes	Date
2	Revision to add figure in the existing datasheet.	8/27/2025
3	Added Figure 5 (Normalized ON Resistance vs. Junction Temperature)	5/25/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

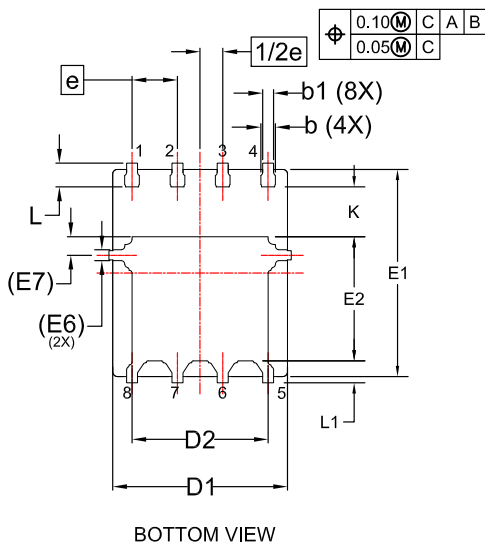
DFN8 5x6.15, 1.27P, DUAL COOL
CASE 506EG
ISSUE D

DATE 25 AUG 2020

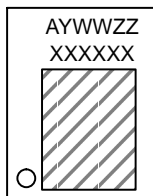


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

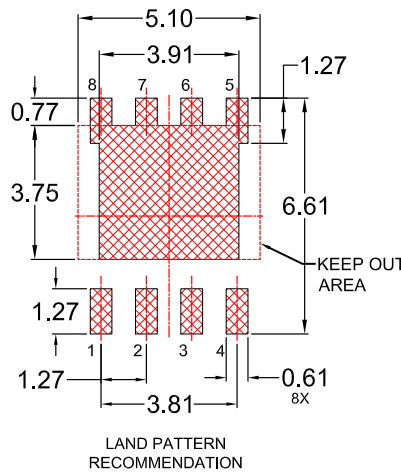
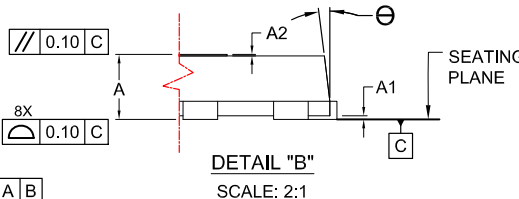


GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



LAND PATTERN RECOMMENDATION
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
Θ	0°	---	12°

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DESCRIPTION:	DFN8 5x6.15, 1.27P, DUAL COOL	PAGE 1 OF 1

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