

MOSFET – Power, Single N-Channel, SO8-FL

30 V, 462 A, 0.58 mΩ

NTMFS0D55N03CG

Features

- Wide SOA to Improve Inrush Current Management
- Advanced Package (5x6mm) with Excellent Thermal Conduction
- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

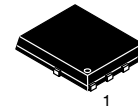
- Hot Swap Application
- Power Load Switch
- Battery Management and Protection

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

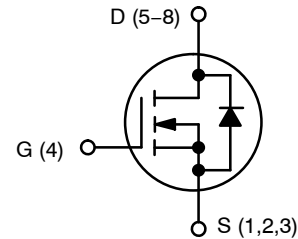
Symbol	Parameter		Value	Unit	
V_{DSS}	Drain-to-Source Voltage		30	V	
V_{GS}	Gate-to-Source Voltage		± 20	V	
I_D	Continuous Drain Current $R_{\theta JC}$ (Note 3)	Steady State	$T_C = 25^\circ\text{C}$	462	A
			$T_C = 100^\circ\text{C}$	326	
			$T_C = 25^\circ\text{C}$	199	
P_D	Power Dissipation $R_{\theta JC}$ (Note 3)		$T_C = 25^\circ\text{C}$	199	W
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	65	A
			$T_A = 100^\circ\text{C}$	46	
			$T_A = 25^\circ\text{C}$	3.9	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		$T_A = 25^\circ\text{C}$	3.9	W
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	35	A
			$T_A = 100^\circ\text{C}$	25	
			$T_A = 25^\circ\text{C}$	1.1	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 2, 3)		$T_A = 25^\circ\text{C}$	1.1	W
I_{DM}	Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	900	A	
I_S	Source Current (Body Diode)		166	A	
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($I_L = 45.5 \text{ A}_{pk}$)		1346	mJ	
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 to +175	$^\circ\text{C}$	
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	0.58 mΩ @ 10 V	462 A

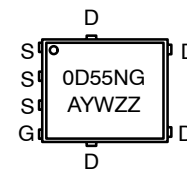


DFN5 (SO-8FL)
CASE 506EZ



N-CHANNEL MOSFET

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 1)	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 1)	38	
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	133	

- Surface-mounted on FR4 board using 1 in² pad, 2 oz Cu pad.
- Surface-mounted on FR4 board using minimum pad, 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30	–	–	V	
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, ref to 25°C	–	12	–	mV/°C	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}$	$T_J = 25^\circ\text{C}$	–	–	1.0	μA
			$T_J = 125^\circ\text{C}$	–	–	100	
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA	

ON CHARACTERISTICS (Note 4)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 330\ \mu\text{A}$	1.3	–	2.2	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient	$I_D = 330\ \mu\text{A}$, ref to 25°C	–	–5	–	mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$	–	0.5	0.58	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 3\text{ V}, I_D = 30\text{ A}$	–	108	–	S
R_G	Gate Resistance	$T_A = 25^\circ\text{C}$	–	0.4	3.0	Ω

CHARGES AND CAPACITANCES

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$	10150	14500	18500	pF
C_{OSS}	Output Capacitance		4501	6430	8359	
C_{RSS}	Reverse Transfer Capacitance		48	120	222	
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$	121.1	173	224.9	nC
$Q_{G(TH)}$	Threshold Gate Charge		15.4	22	28.6	
Q_{GS}	Gate-to-Source Charge		27.3	39	50.7	
Q_{GD}	Gate-to-Drain Charge		4.4	11	20.5	

SWITCHING CHARACTERISTICS (Note 5)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}, R_G = 3.0\ \Omega$	–	30	–	ns
t_r	Rise Time		–	13	–	
$t_{d(OFF)}$	Turn-Off Delay Time		–	98	–	
t_f	Fall Time		–	20	–	

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 30\text{ A}$	$T_J = 25^\circ\text{C}$	–	0.75	1.2	V
			$T_J = 125^\circ\text{C}$	–	0.62	–	
t_{RR}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, V_{DS} = 15\text{ V}, I_S = 30\text{ A}$	–	104	–	ns	
Q_{RR}	Reverse Recovery Charge		–	177	–	nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

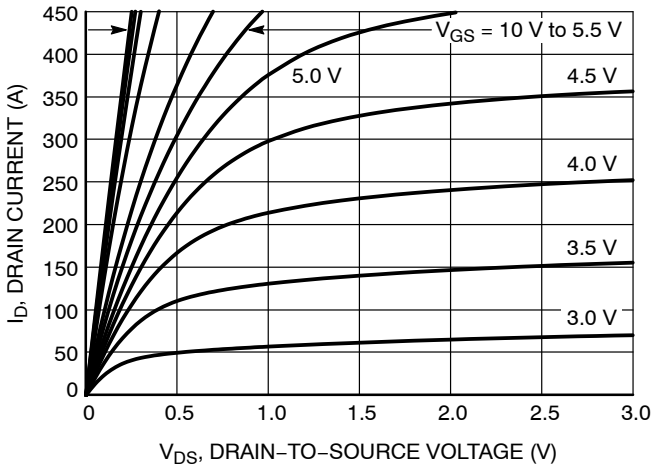


Figure 1. On-Region Characteristics

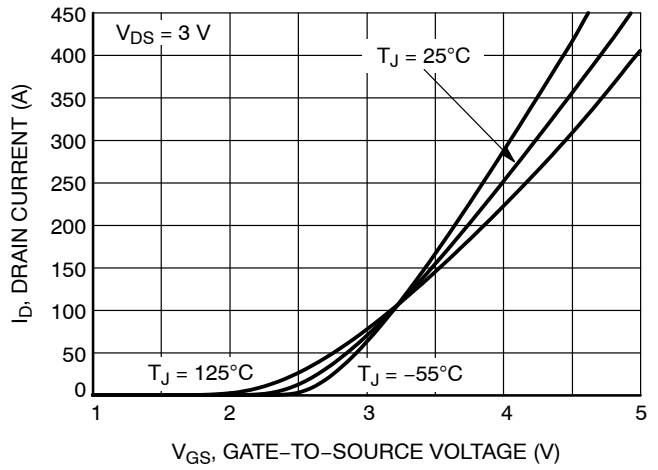


Figure 2. Transfer Characteristics

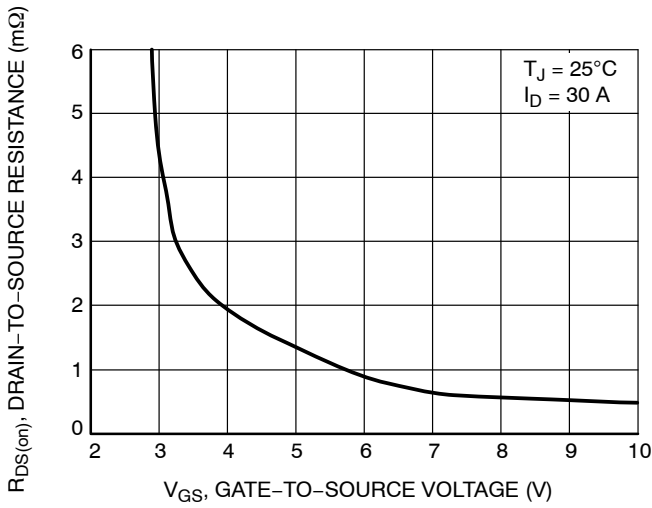


Figure 3. On-Resistance vs. Gate-to-Source Voltage

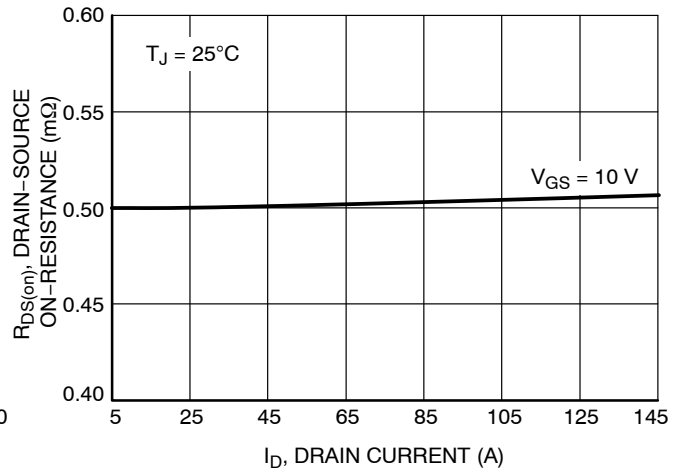


Figure 4. On-Resistance vs. Drain Current

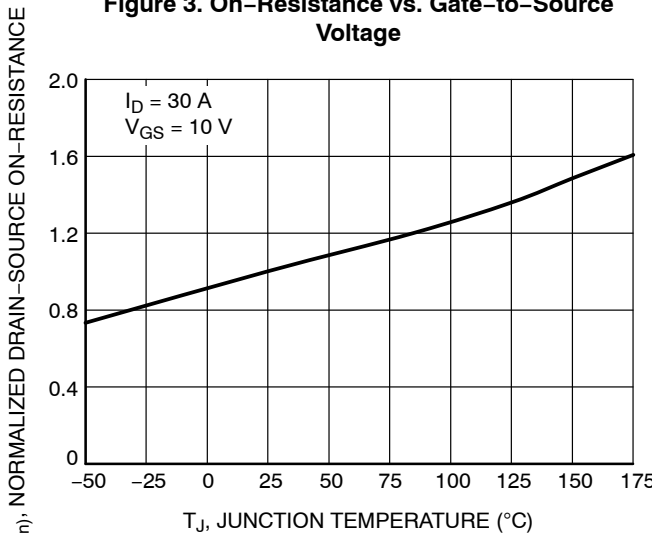


Figure 5. On-Resistance Variation with Temperature

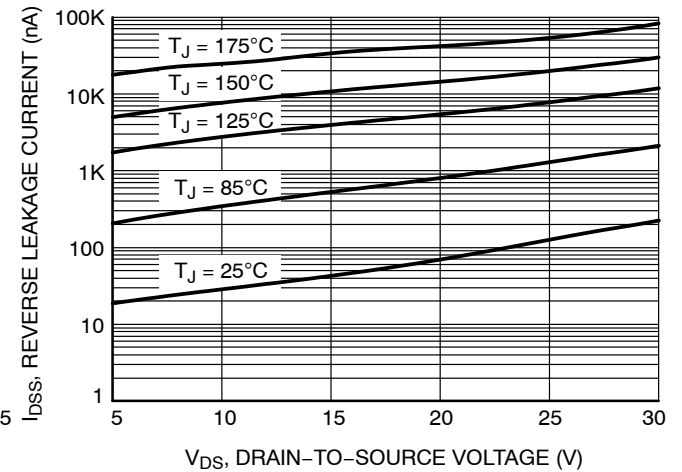


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS (continued)

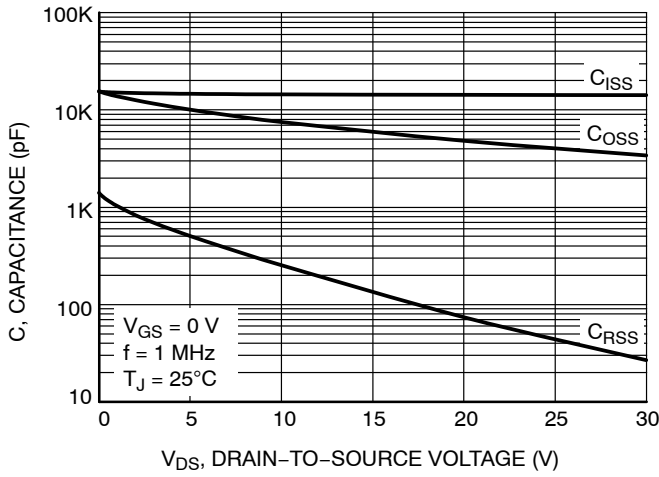


Figure 7. Capacitance Variation

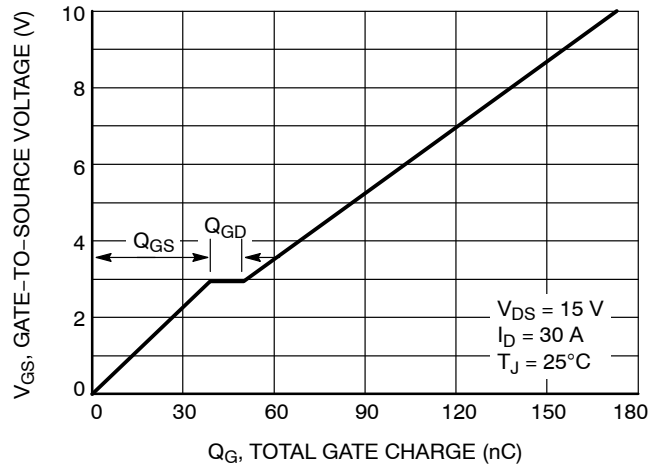


Figure 8. Gate-to-Source Voltage vs. Total Charge

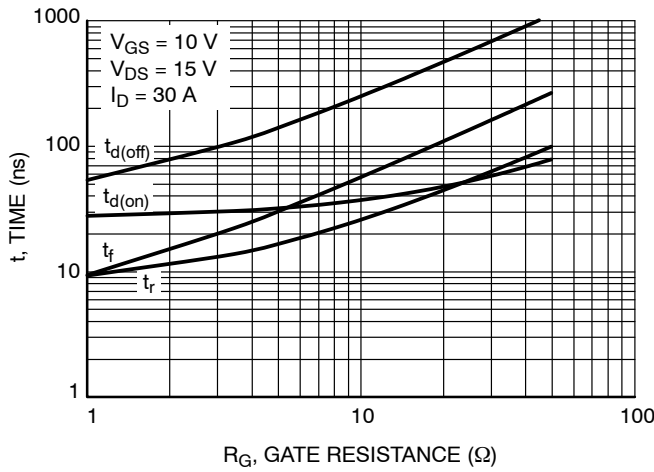


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

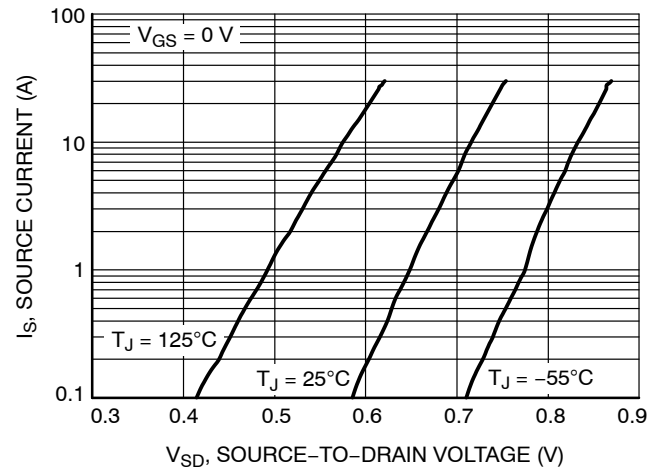


Figure 10. Diode Forward Voltage vs. Current

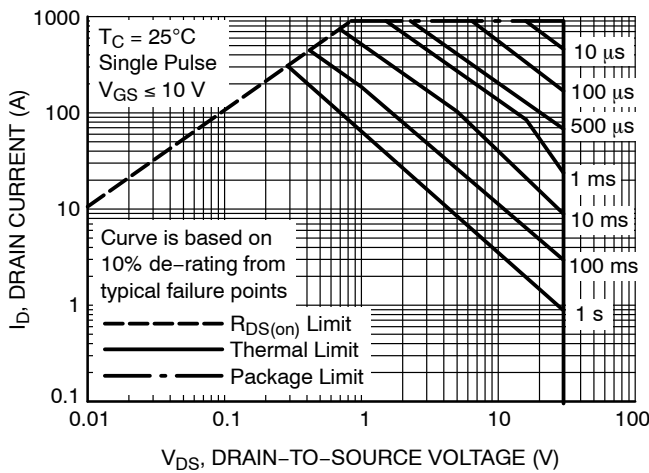


Figure 11. Safe Operating Area

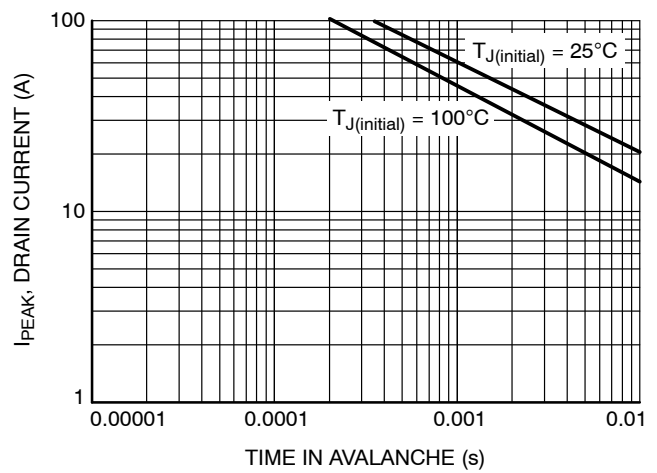


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS (continued)

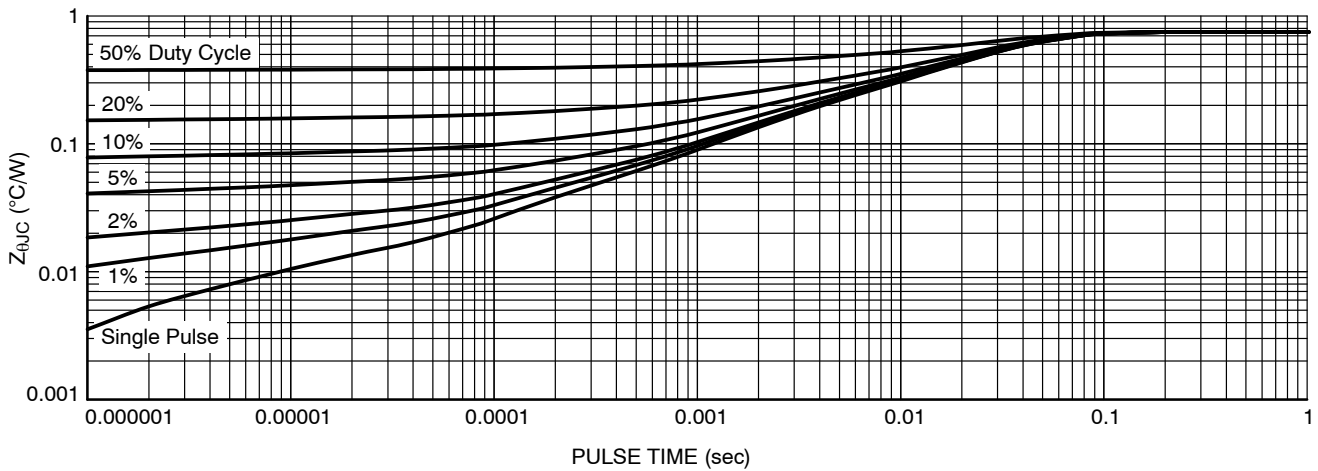
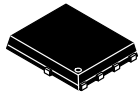


Figure 13. Junction-to-Case Transient Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMFS0D55N03CGT1G	0D55NG	DFN5 (Pb-Free)	1,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



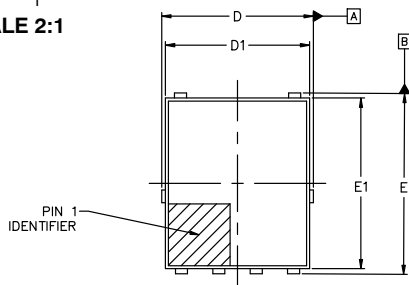
1
SCALE 2:1

DFN-5, 4.90x5.90x1.00, 1.27P
CASE 506EZ
ISSUE C

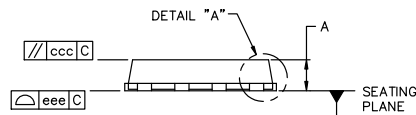
DATE 18 JUN 2026

NOTES:

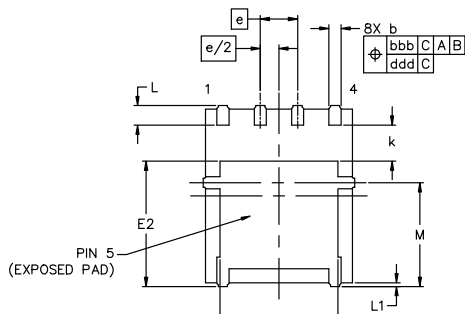
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.



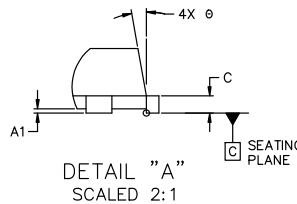
TOP VIEW



SIDE VIEW



BOTTOM VIEW



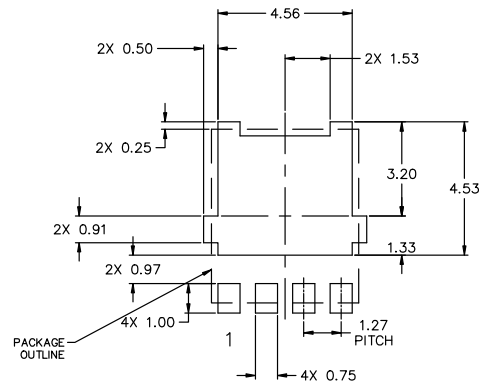
MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.80	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
k	1.10	1.20	1.40
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
ø	0°	---	12°
TOLERANCE FORM & POSITION			
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.10		

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN-5, 4.90x5.90x1.00, 1.27P	PAGE 1 OF 1

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