

# Enhancement Mode Gallium Nitride (GaN) HEMT

700 V, 75 mΩ, 21 A, PDSO-E3 (DPAK)

## NTD100N70GN1

### Features

- Low  $R_{DS(ON)}$  to Minimize Conduction Losses
- Ultra Low Gate Charge for High Speed Switching
- $FOM-Q_G = 280 \text{ nC} \cdot \text{m}\Omega$
- Small Footprint for High Density PCB Design
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### Typical Applications

- High Density Power Modules
- High Frequency AC-DC and DC-DC Converters
- High Performance PSU for Consumer and Industrial
- Resonant Conversion

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter                                                                                                                                           | Symbol          | Value      | Unit             |
|-----------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|------------|------------------|
| Drain-to-Source Voltage                                                                                                                             | $V_{DSS}$       | 700        | V                |
| Drain-to-Source Transient Voltage,<br>$t_P < 200 \mu\text{s}$                                                                                       | $V_{DS(TRAN)}$  | 800        | V                |
| Pulsed Drain-to-Source Voltage,<br>$T_J = 25^\circ\text{C}$ ( $t_{TOTAL} < 10\text{h}$ ) / $T_J = 125^\circ\text{C}$<br>( $t_{TOTAL} < 1\text{h}$ ) | $V_{DS(PULSE)}$ | 750        | V                |
| Gate-to-Source Voltage                                                                                                                              | $V_{GS}$        | -6 to 7    | V                |
| Gate-to-Source Transient Voltage,<br>$t_P = 50 \text{ ns}$ , $f_P = 100 \text{ kHz}$ , Open Drain                                                   | $V_{GS(PULSE)}$ | -20 to 10  | V                |
| Continuous Drain Current, $T_{CASE} = 25^\circ\text{C}$                                                                                             | $I_{DS}$        | 21         | A                |
| Pulsed Drain Current, $t_P < 10 \mu\text{s}$ ,<br>$T_C = 25^\circ\text{C}$<br>$T_C = 125^\circ\text{C}$                                             | $I_{DS(PULSE)}$ | 41<br>23   | A                |
| Power Dissipation, $V_{GS} = 6 \text{ V}$ ,<br>$T_{CASE} = 25^\circ\text{C}$                                                                        | $P_{TOT}$       | 105        | W                |
| Operating Junction Temperature                                                                                                                      | $T_J$           | -55 to 150 | $^\circ\text{C}$ |
| Storage Temperature                                                                                                                                 | $T_{STG}$       | -55 to 150 | $^\circ\text{C}$ |

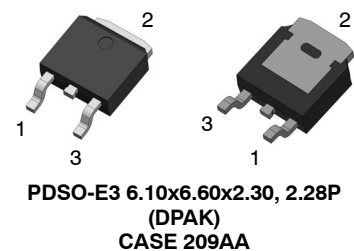
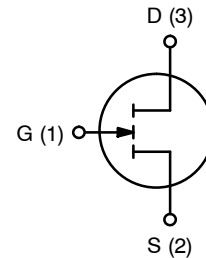
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

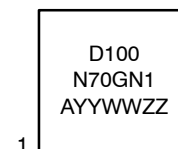
| Parameter                            | Symbol          | Value | Unit               |
|--------------------------------------|-----------------|-------|--------------------|
| Junction-to-Case                     | $R_{\theta JC}$ | 1.19  | $^\circ\text{C/W}$ |
| Junction-to-Ambient                  | $R_{\theta JA}$ | 54.8  | $^\circ\text{C/W}$ |
| Maximum Soldering Temperature (MSL3) | $T_{SLD}$       | 260   | $^\circ\text{C}$   |

1. Device on 1 in<sup>2</sup>, 2 oz copper pad on single layer FR-4 PCB

| $V_{(BR)DSS}$ | $R_{DS(ON)} \text{ TYP}$ | $I_D \text{ MAX}$ |
|---------------|--------------------------|-------------------|
| 700 V         | 75 mΩ                    | 21 A              |



### MARKING DIAGRAM



D100N70GN1 = Specific Device Code  
A = Assembly Location  
YY = Year  
WW = Work Week  
ZZ = Assembly Lot Code

### ORDERING INFORMATION

| Device          | Package        | Shipping <sup>†</sup> |
|-----------------|----------------|-----------------------|
| NTD100N70GN1TXG | PDSO-E3 (DPAK) | 2500 / Tape & Reel    |

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# NTD100N70GN1

## ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|                                   |               |                                                                                 |     |     |    |               |
|-----------------------------------|---------------|---------------------------------------------------------------------------------|-----|-----|----|---------------|
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}$                                                           | 700 |     |    | V             |
| Drain-to-Source Leakage Current   | $I_{DSS}$     | $V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}$                                    |     | 0.8 | 48 | $\mu\text{A}$ |
|                                   |               | $V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}, T_J = 125\text{ }^{\circ}\text{C}$ |     | 9   |    |               |
| Gate-to-Source Leakage Current    | $I_{GSS}$     | $V_{GS} = 6\text{ V}, V_{DS} = 0\text{ V}$                                      |     | 45  |    | $\mu\text{A}$ |

### ON CHARACTERISTICS

|                               |              |                                                                               |     |     |     |                  |
|-------------------------------|--------------|-------------------------------------------------------------------------------|-----|-----|-----|------------------|
| Drain-to-Source On Resistance | $R_{DS(ON)}$ | $V_{GS} = 6\text{ V}, I_{DS} = 0.5\text{ A}$                                  |     | 75  | 100 | $\text{m}\Omega$ |
|                               |              | $V_{GS} = 6\text{ V}, I_{DS} = 6\text{ A}$                                    |     | 75  |     |                  |
|                               |              | $V_{GS} = 6\text{ V}, I_{DS} = 6\text{ A}, T_J = 125\text{ }^{\circ}\text{C}$ |     | 151 |     |                  |
| Gate Threshold Voltage        | $V_{GS(TH)}$ | $V_{DS} = V_{GS}, I_{DS} = 19.5\text{ mA}, T_J = 25\text{ }^{\circ}\text{C}$  | 1.2 | 1.6 | 2.5 | V                |
|                               |              | $V_{DS} = V_{GS}, I_{DS} = 19.5\text{ mA}, T_J = 125\text{ }^{\circ}\text{C}$ |     | 1.5 |     |                  |

### DYNAMIC CHARACTERISTICS

|                                    |               |                                                                     |  |      |  |               |
|------------------------------------|---------------|---------------------------------------------------------------------|--|------|--|---------------|
| Input Capacitance                  | $C_{ISS}$     | $V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 100\text{ kHz}$    |  | 139  |  | $\text{pF}$   |
| Output Capacitance                 | $C_{OSS}$     |                                                                     |  | 47   |  |               |
| Reverse Transfer Capacitance       | $C_{RSS}$     |                                                                     |  | 0.52 |  |               |
| Output Capacitance, Energy Related | $C_{OSS(ER)}$ | $V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$         |  | 68.7 |  | $\text{pF}$   |
| Output Capacitance, Time Related   | $C_{OSS(TR)}$ |                                                                     |  | 90.9 |  |               |
| Output Charge                      | $Q_{OSS}$     |                                                                     |  | 36.3 |  | $\text{nC}$   |
| Output Capacitance Stored Energy   | $E_{OSS}$     |                                                                     |  | 5.5  |  | $\mu\text{J}$ |
| Gate Resistance                    | $R_G$         | $f = 5\text{ MHz}$                                                  |  | 7    |  | $\Omega$      |
| Gate Charge                        | $Q_G$         | $V_{DS} = 400\text{ V}, I_{DS} = 6\text{ A}, V_{GS} = 0/6\text{ V}$ |  | 3.8  |  | $\text{nC}$   |
| Gate-to-Source Charge              | $Q_{GS}$      |                                                                     |  | 0.3  |  |               |
| Gate-to-Drain Charge               | $Q_{GD}$      |                                                                     |  | 1.4  |  |               |
| Gate Plateau Voltage               | $V_{PLAT}$    |                                                                     |  | 2.1  |  | V             |

### REVERSE CONDUCTION CHARACTERISTICS

|                                 |                 |                                                          |  |     |    |   |
|---------------------------------|-----------------|----------------------------------------------------------|--|-----|----|---|
| Source-to-Drain Reverse Voltage | $V_{SD}$        | $V_{GS} = 0\text{ V}, I_{SD} = 6\text{ A}$               |  | 2.4 |    | V |
| Pulsed Reverse Current          | $I_{SD(PULSE)}$ | $V_{GS} = 6\text{ V}, t_{PULSE} = 10\text{ }\mu\text{s}$ |  |     | 41 | A |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS ( $T_J = 25\text{ }^{\circ}\text{C}$  UNLESS OTHERWISE SPECIFIED)

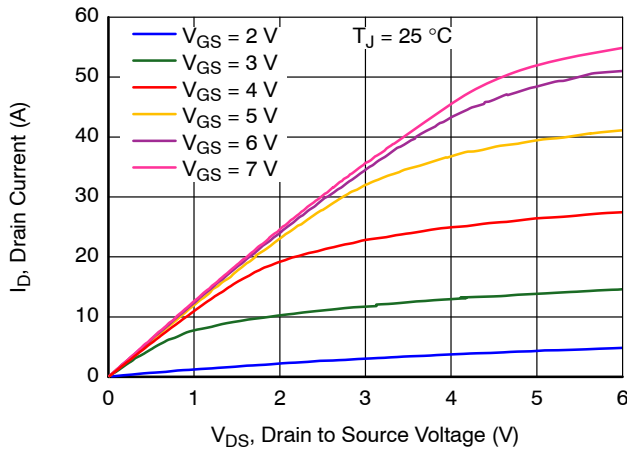


Figure 1. Output Characteristics at  $T_J = 25\text{ }^{\circ}\text{C}$

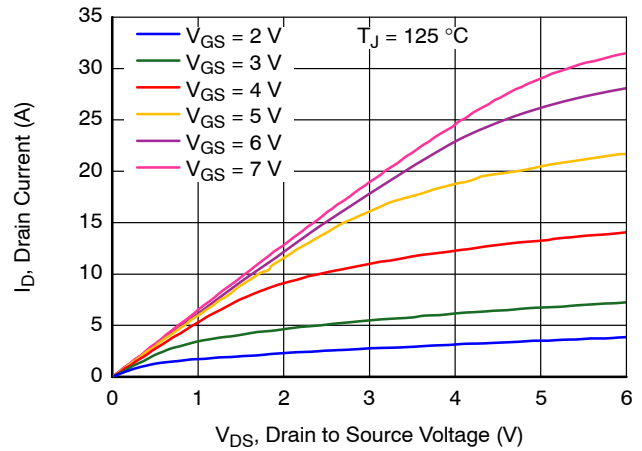


Figure 2. Output Characteristics at  $T_J = 125\text{ }^{\circ}\text{C}$

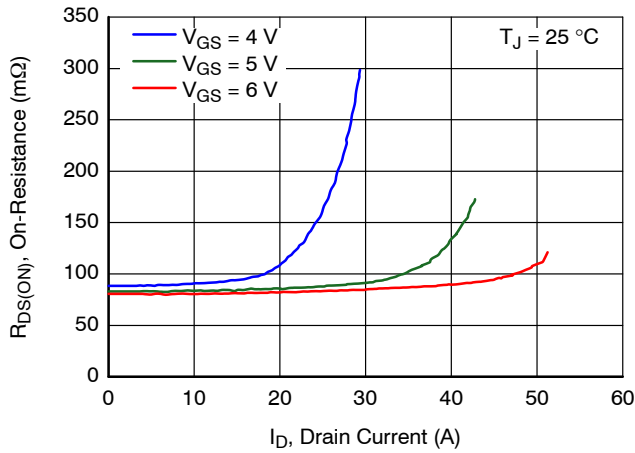


Figure 3. On-Resistance vs. Drain Current at  $T_J = 25\text{ }^{\circ}\text{C}$

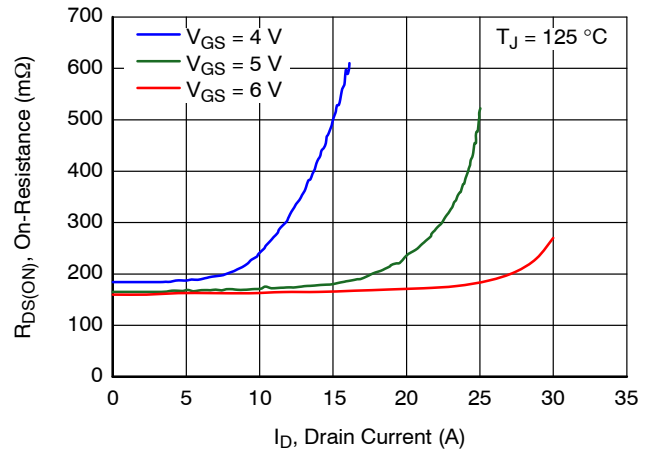


Figure 4. On-Resistance vs. Drain Current at  $T_J = 125\text{ }^{\circ}\text{C}$

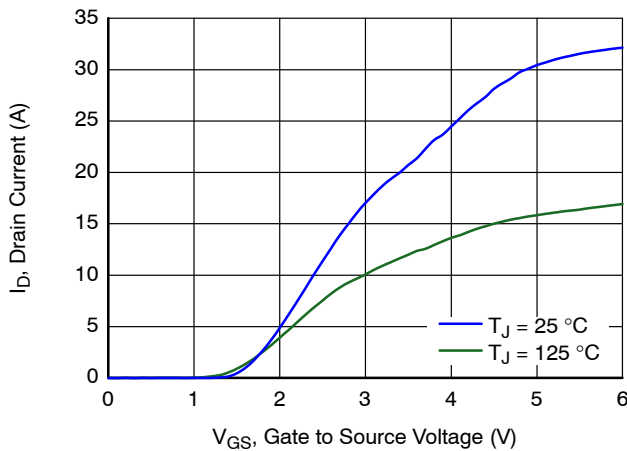


Figure 5. Transfer Characteristics at  $V_{DS} = 3\text{ V}$

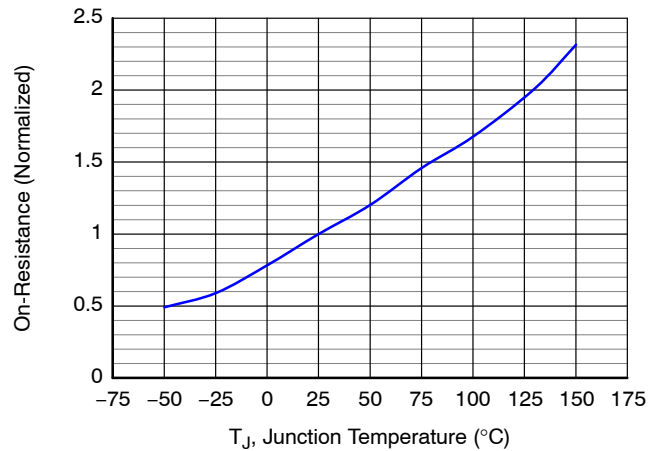
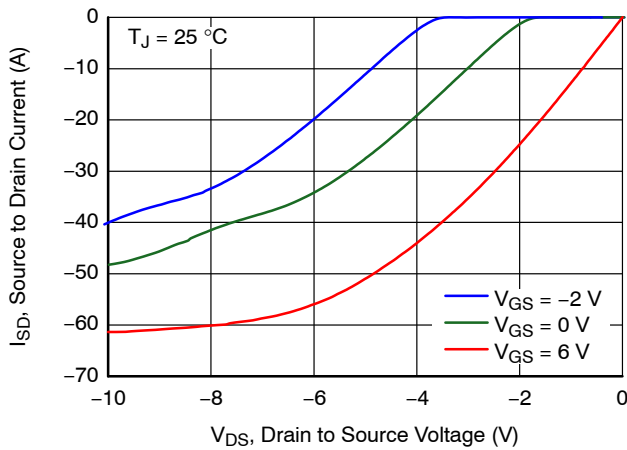
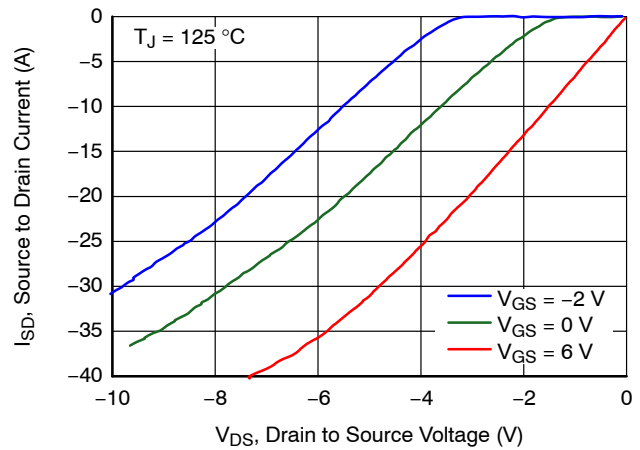


Figure 6. Normalized On-Resistance vs. Temperature at  $V_{GS} = 6\text{ V}$

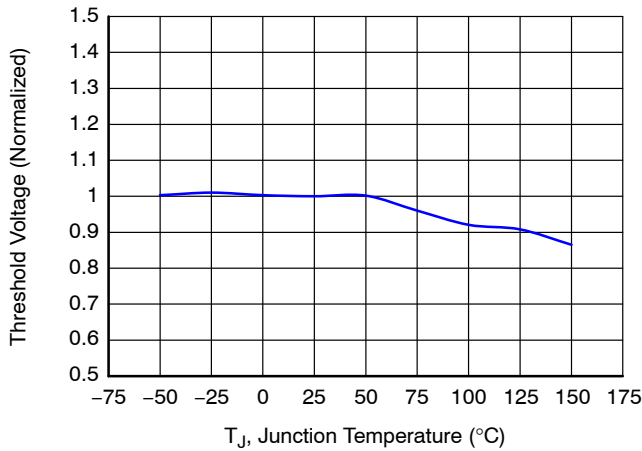
## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED) (CONTINUED)



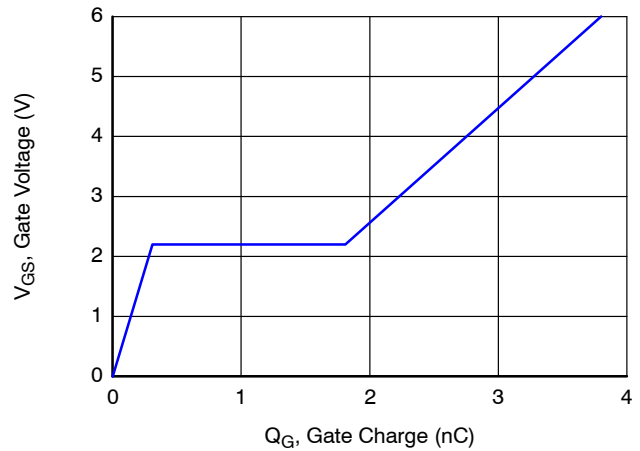
**Figure 7. Reverse Conduction Characteristics at  $T_J = 25^\circ\text{C}$**



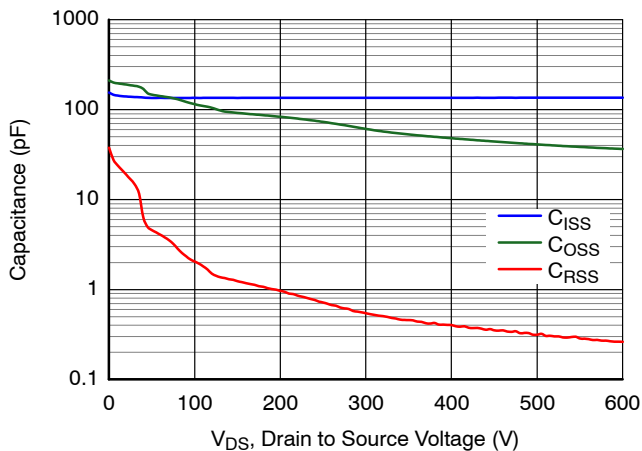
**Figure 8. Reverse Conduction Characteristics at  $T_J = 125^\circ\text{C}$**



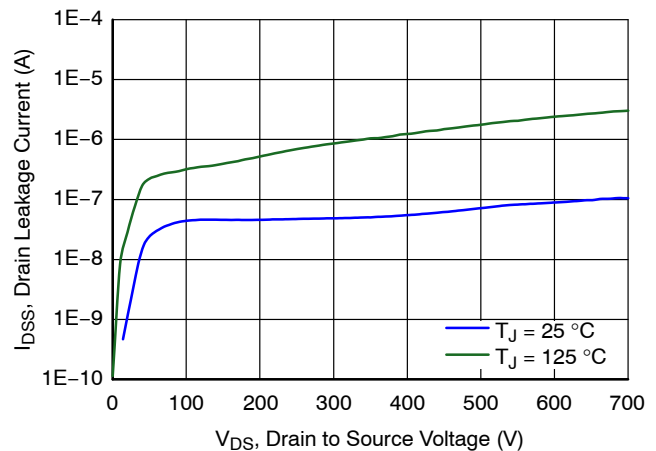
**Figure 9. Normalized Threshold Voltage vs. Temperature**



**Figure 10. Gate Charge Characteristics at  $I_{DS} = 20\text{ A}$**



**Figure 11. Capacitance Characteristics**



**Figure 12. Drain Leakage Characteristics**

TYPICAL CHARACTERISTICS ( $T_J = 25\text{ }^{\circ}\text{C}$  UNLESS OTHERWISE SPECIFIED) (CONTINUED)

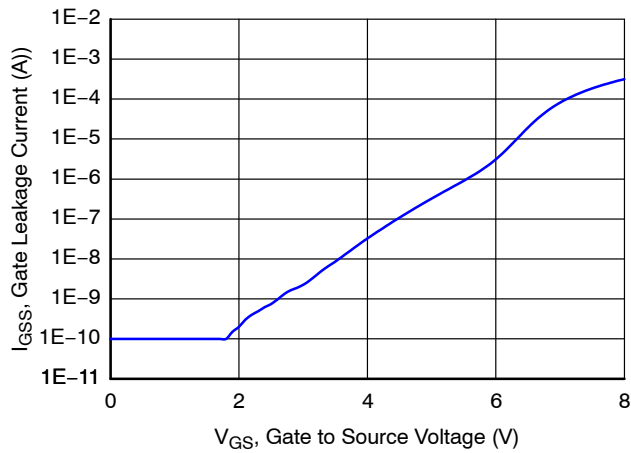


Figure 13. Gate Leakage Characteristics

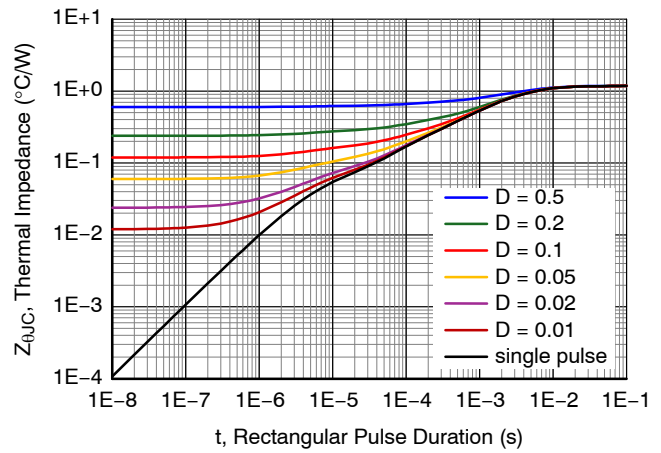


Figure 14. Transient Thermal Impedance

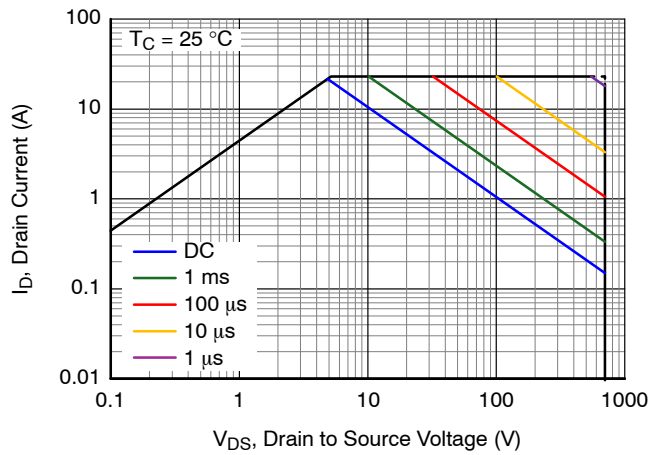


Figure 15. Safe Operating Area at  $T_C = 25\text{ }^{\circ}\text{C}$

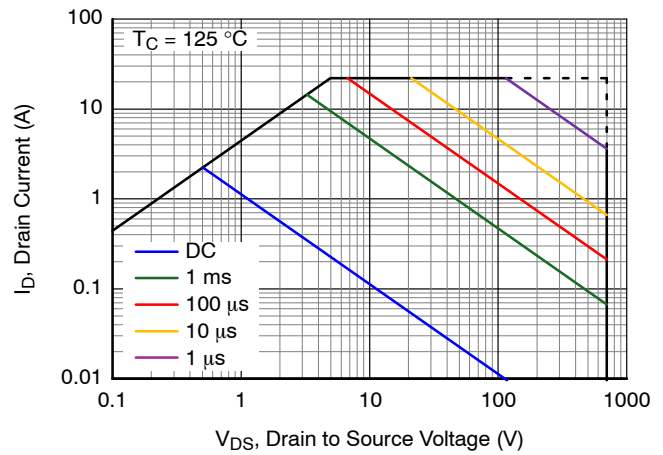


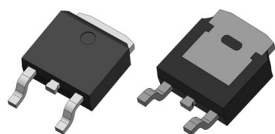
Figure 16. Safe Operating Area at  $T_C = 125\text{ }^{\circ}\text{C}$

# NTD100N70GN1

## REVISION HISTORY

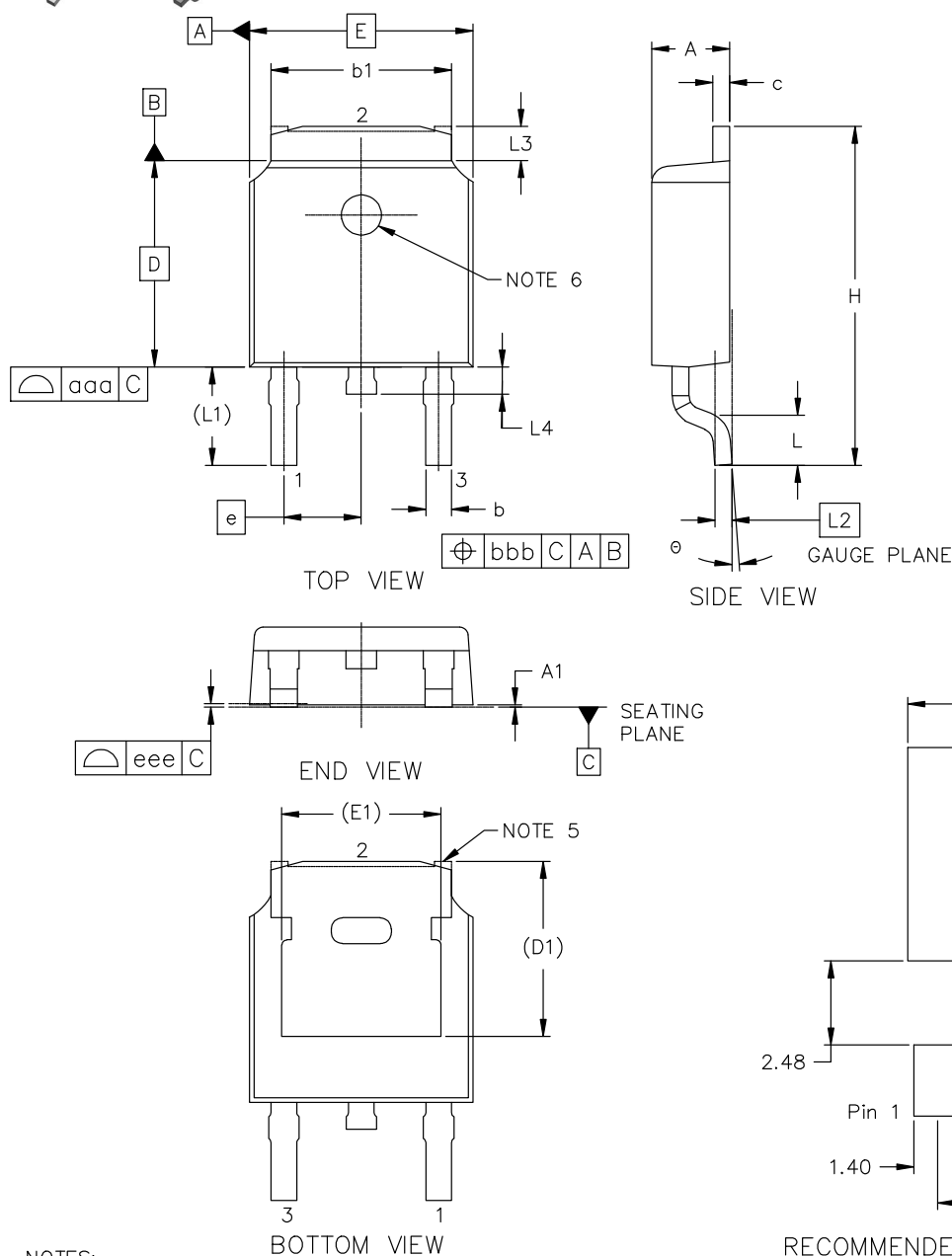
| Revision | Description of Changes               | Date      |
|----------|--------------------------------------|-----------|
| 0        | Initial production document release. | 6/17/2026 |



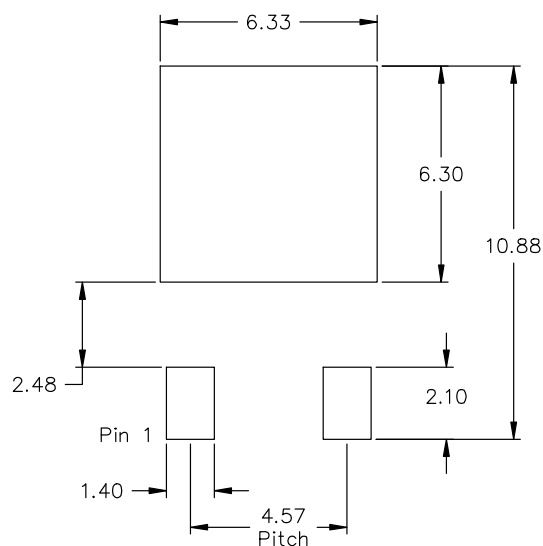


**PDSO-E3 6.10x6.60x2.30, 2.28P**  
CASE 209AA  
ISSUE O

DATE 04 MAY 2026



| MILLIMETERS               |           |      |       |
|---------------------------|-----------|------|-------|
| DIM                       | MIN       | NOM  | MAX   |
| A                         | 2.20      | 2.30 | 2.40  |
| A1                        | 0.00      | 0.07 | 0.13  |
| b                         | 0.63      | 0.76 | 0.90  |
| b1                        | 5.10      | 5.33 | 5.46  |
| c                         | 0.43      | 0.53 | 0.61  |
| D                         | 6.10 BSC  |      |       |
| D1                        | 5.30 REF  |      |       |
| E                         | 6.60 BSC  |      |       |
| E1                        | 4.83 REF  |      |       |
| e                         | 2.286 BSC |      |       |
| H                         | 9.40      | 9.95 | 10.50 |
| L                         | 1.38      | 1.50 | 1.75  |
| L1                        | 2.90 REF  |      |       |
| L2                        | 0.50 BSC  |      |       |
| L3                        | 0.88      | 1.08 | 1.28  |
| L4                        | 0.50      | 0.75 | 1.00  |
| ø                         | 0°        | 5°   | 10°   |
| TOLERANCE FORM & POSITION |           |      |       |
| aaa                       | 0.15      |      |       |
| bbb                       | 0.20      |      |       |
| eee                       | 0.10      |      |       |



## RECOMMENDED MOUNTING FOOTPRINT

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

- NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.
  4. PACKAGE OUTLINE EXCLUSIVE OF METAL BURR DIMENSIONS.
  5. SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
  6. MOLD EJECTION PIN MARK IS OPTIONAL.

|                         |  |                                      |                                                                                                                                                                                     |
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**PDSO-E3 6.10x6.60x2.30, 2.28P**  
CASE 209AA  
ISSUE O

DATE 04 MAY 2026

**GENERIC  
MARKING DIAGRAM\***

|                               |
|-------------------------------|
| XXXXXXX<br>XXXXXXX<br>AYYWWZZ |
|-------------------------------|

XXXX = Specific Device Code  
A = Assembly Location  
YY = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                         |                                      |                                                                                                                                                                                     |
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