Low-Power 16-bit I/O Expander for I^{2}C Bus with Interrupt

NLA9535, NLA9535C

The NLA9535 and NLA9535C provide 16 bits of General Purpose parallel Input / Output (GPIO) expansion through the I^{2}C-bus / SMBus.

The devices consist of two 8-bit Configuration (Input or Output selection), Input, Output and Polarity Inversion (active-HIGH or active-LOW operation) registers. At power on, all I/Os default to inputs. Each I/O may be configured as either input or output by writing to its corresponding I/O configuration bit. The data for each Input or Output is kept in its corresponding Input or Output register. The Polarity Inversion register may be used to invert the polarity of the read register. All registers can be read by the system controller.

The devices provide an open-drain interrupt output which is activated when any input state differs from its corresponding input port register state. The interrupt output is used to indicate to the system controller that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (AD0, AD1, AD2) are used to configure the I^{2}C-bus target address of the device. Up to 64 devices are allowed to share the same I^{2}C-bus / SMBus.

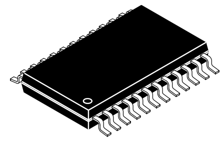
The NLA9535 is identical to the NLA9555 without the internal I/O pull-up resistors. This significantly reduces power consumption when the I/Os are held LOW.

The NLA9535C is identical to the NLA9535 with high impedance open-drain outputs on the I/O pins.

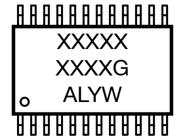
Features

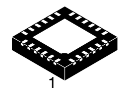
- V_{DD} Operating Range: 1.65 V to 5.5 V
- SDA Sink Capability: 30 mA
- 5.5 V Tolerant I/Os
- Polarity Inversion Register
- Active LOW Interrupt Output
- Low Standby Current
- Noise Filter on SCL/SDA Inputs
- No Glitch on Power-up, Internal Power-on Reset
- 64 Programmable Target Addresses Using Three Address Pins
- 16 I/O Pins Which Default to 16 Inputs
- I^{2}C SCL Clock Frequencies Supported:
  - Standard Mode: 100 kHz
  - Fast Mode: 400 kHz
  - Fast Mode +: 1 MHz
- ESD Performance: 2000 V Human Body Model
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAMS

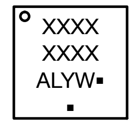


TSSOP-24
DT SUFFIX
CASE 948H





WQFN24
MT SUFFIX
CASE 485BG



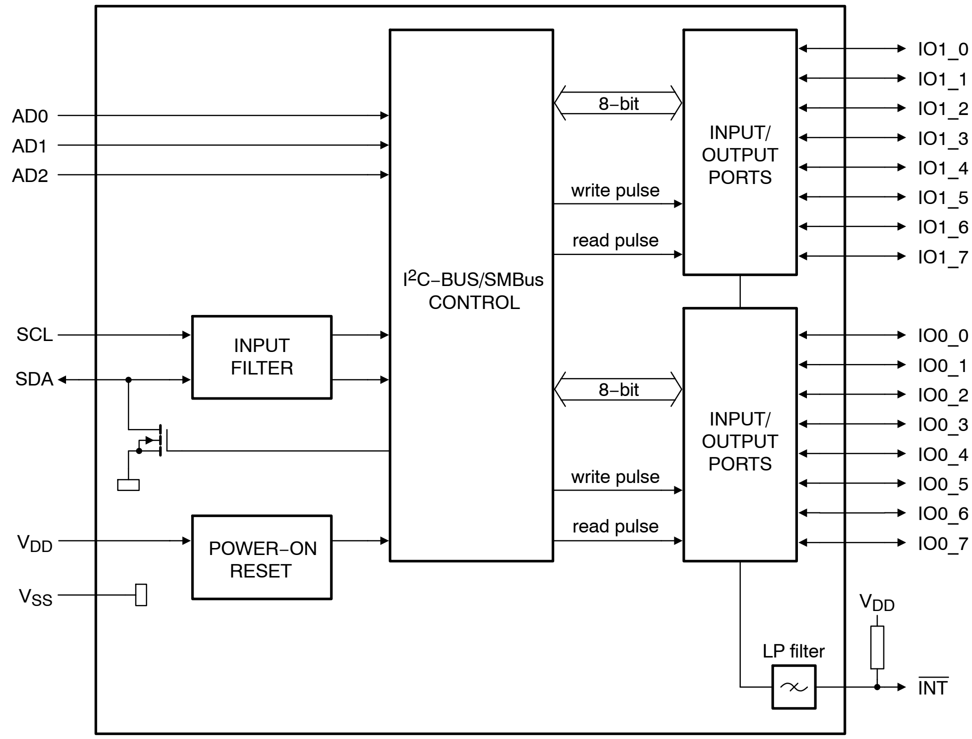
XXXX	=	Specific Device Code
A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

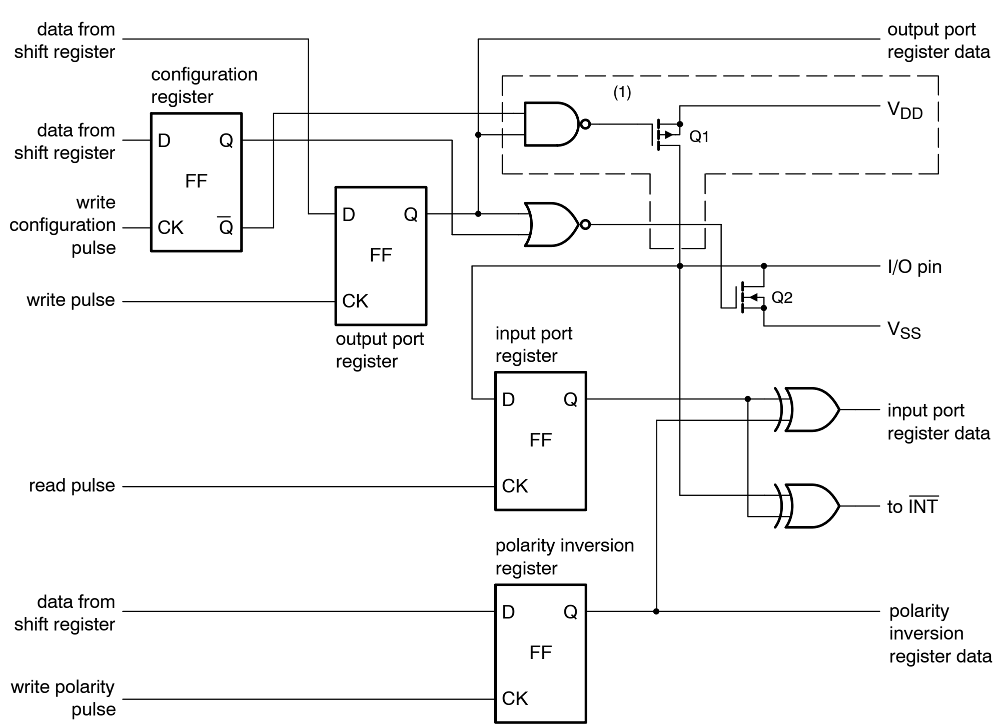
See detailed ordering and shipping information on page 17 of this data sheet.

BLOCK DIAGRAM



Remark: All I/Os are set as inputs at reset.

Figure 1. Block Diagram



At power-on reset, all registers return to default values.

1. NLA9535C I/Os are open-drain only. The portion of the NLA9535 schematic marked inside the dotted line box is not in NLA9535C.

Figure 2. Simplified Schematic of I/Os

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PIN ASSIGNMENT

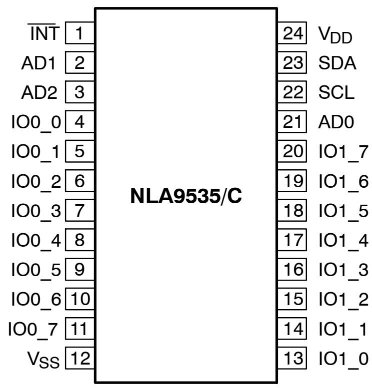
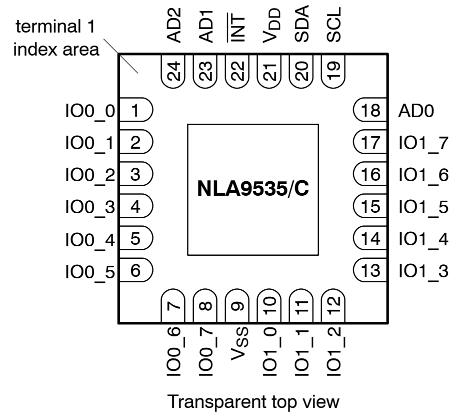


Figure 3. TSSOP24



(The exposed thermal pad at the bottom is not connected to internal circuitry)

Figure 4. WQFN24

Table 1. PIN DESCRIPTIONS

Symbol	Pin		Description
	SOIC24, TSSOP24	WQFN24	
$\overline{INT}$	1	22	Interrupt Output (active-LOW, connect to VDD through a pull-up resistor)
AD1	2	23	Address Input 1
AD2	3	24	Address Input 2
IO0_0	4	1	Port 0 I/O 0
IO0_1	5	2	Port 0 I/O 1
IO0_2	6	3	Port 0 I/O 2
IO0_3	7	4	Port 0 I/O 3
IO0_4	8	5	Port 0 I/O 4
IO0_5	9	6	Port 0 I/O 5
IO0_6	10	7	Port 0 I/O 6
IO0_7	11	8	Port 0 I/O 7
V_{SS}	12	9	Supply Ground
IO1_0	13	10	Port 1 I/O 0
IO1_1	14	11	Port 1 I/O 1
IO1_2	15	12	Port 1 I/O 2
IO1_3	16	13	Port 1 I/O 3
IO1_4	17	14	Port 1 I/O 4
IO1_5	18	15	Port 1 I/O 5
IO1_6	19	16	Port 1 I/O 6
IO1_7	20	17	Port 1 I/O 7
AD0	21	18	Address Input 0
SCL	22	19	Serial Clock Line, connect to VDD through a pull-up resistor
SDA	23	20	Serial Data Line, connect to VDD through a pull-up resistor
V_{DD}	24	21	Supply Voltage

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Table 2. MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{DD}	DC Supply Voltage		−0.5 to +6.5	V
$V_{I/O}$	Input / Output Pin Voltage		−0.5 to +6.5	V
I_I	Input Current		±20	mA
I_O	Output Current		±50	mA
I_{DD}	DC Supply Current		±100	mA
I_{GND}	DC Ground Current		±200	mA
P_{TOT}	Total Power Dissipation		200	mW
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		150	°C
θ_{JA}	Thermal Resistance (Note 1)	TSSOP-24 WQFN24	91 68	°C/W
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34		UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Charged Device Model (Note 3)	> 3000 > 2000	V
$I_{LATCHUP}$	Latchup Performance Above V_{DD} and Below GND at 125 °C (Note 4)		±200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. Operating the device outside its recommended conditions, but still within its maximum rated limits may not cause immediate damage. However, doing so can lead to reduced performance, unpredictable behavior, and potentially shorten the device’s lifespan or reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22-A114-A.
3. Tested to EIA / JESD22-C101-A.
4. Tested to EIA / JESD78.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Positive DC Supply Voltage	1.65	5.5	V
$V_{I/O}$	Switch Input / Output Voltage	0	5.5	V
T_A	Operating Free-Air Temperature	−55	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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Table 4. DC ELECTRICAL CHARACTERISTICS V_{DD} = 1.65 V to 5.5 V, unless otherwise specified.

Symbol	Parameter	Conditions	T_A = −55 °C to +125 °C			Unit
			Min	Typ	Max	
SUPPLIES						
I_{DD}	Supply Current	Operating mode; no load; I/O = Inputs; AD2, AD1, AD0, V_I = V_{DD} or 0 V; f_{SCL} = 1 MHz; V_{DD} = 4.5 V f_{SCL} = 1 MHz; V_{DD} = 3.0 V f_{SCL} = 1 MHz; V_{DD} = 2.3 V f_{SCL} = 1 MHz; V_{DD} = 1.65 V f_{SCL} = 400 kHz; V_{DD} = 4.5 V f_{SCL} = 400 kHz; V_{DD} = 3.0 V f_{SCL} = 400 kHz; V_{DD} = 2.3 V f_{SCL} = 400 kHz; V_{DD} = 1.65 V f_{SCL} = 100 kHz; V_{DD} = 4.5 V f_{SCL} = 100 kHz; V_{DD} = 3.0 V f_{SCL} = 100 kHz; V_{DD} = 2.3 V f_{SCL} = 100 kHz; V_{DD} = 1.65 V		 112 53 35 23 47 23 15 10 14 7 5 3	 150 90 88 70 55 45 44 35 25 23 22 18	μA
I_{STB}	Standby Current	Standby mode; no load; V_I = 0 V; f_{SCL} = 0 Hz; I/O = inputs V_I = V_{DD}; f_{SCL} = 0 Hz; I/O = inputs		 0.3 0.3	 15 5.0	 μA μA
V_{POR+}	Power-On Reset Voltage (Note 5)	V_{DD} Rising; no load; V_I = V_{DD} or 0 V			1.55	V
V_{POR-}	Power-On Reset Voltage (Note 5)	V_{DD} Falling; no load; V_I = V_{DD} or 0 V	0.64			V
INPUT SCL; Input / Output SDA						
V_{IH}	High-Level Input Voltage		0.7 x V_{DD}			V
V_{IL}	Low-Level Input Voltage				0.3 x V_{DD}	V
I_{OL}	Low-Level Output Current	V_{OL} = 0.4 V; V_{DD} < 2.3 V	10			mA
		V_{DD} ≥ 2.3 V	20			
		V_{DD} ≥ 4.5 V	30	–	–	
I_L	Leakage Current	V_I = V_{DD} or 0 V			±1	μA
C_I	Input Capacitance	V_I = 0 V		4.6	6	pF
I/Os						
V_{IH}	High-Level Input Voltage		0.7 x V_{DD}			V
V_{IL}	Low-Level Input Voltage				0.3 x V_{DD}	V
I_{OL}	Low-Level Output Current (Note 6)	V_{OL} = 0.5 V; V_{DD} = 1.65 V V_{OL} = 0.5 V; V_{DD} = 2.3 V V_{OL} = 0.5 V; V_{DD} = 3.0 V V_{OL} = 0.5 V; V_{DD} = 4.5 V	8 12 17 25	20 28 35 42		mA
$I_{OL(tot)}$	Total Low-Level Output Current (Note 6)	V_{OL} = 0.5 V; V_{DD} = 4.5 V			200	mA
V_{OH}	High-Level Output Voltage (NLA9535 Only)	I_{OH} = −3 mA; V_{DD} = 1.65 V I_{OH} = −4 mA; V_{DD} = 1.65 V I_{OH} = −8 mA; V_{DD} = 2.3 V I_{OH} = −10 mA; V_{DD} = 2.3 V I_{OH} = −8 mA; V_{DD} = 3.0 V I_{OH} = −10 mA; V_{DD} = 3.0 V I_{OH} = −8 mA; V_{DD} = 4.5 V I_{OH} = −10 mA; V_{DD} = 4.5 V	1.2 1.1 1.8 1.7 2.6 2.5 4.1 4.0			V
V_{OL}	Low-Level Output Voltage	I_{OH} = 3 mA; V_{DD} = 1.65 V I_{OH} = 4 mA; V_{DD} = 1.65 V I_{OH} = 8 mA; V_{DD} = 2.3 V I_{OH} = 10 mA; V_{DD} = 2.3 V I_{OH} = 8 mA; V_{DD} = 3.0 V I_{OH} = 10 mA; V_{DD} = 3.0 V I_{OH} = 8 mA; V_{DD} = 4.5 V I_{OH} = 10 mA; V_{DD} = 4.5 V			0.4 0.4 0.25 0.25 0.25 0.25 0.2 0.2	V
I_{LH}	Input Leakage Current	V_{DD} = 5.5 V; V_I = V_{DD}			1	μA

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Table 4. DC ELECTRICAL CHARACTERISTICS V_{DD} = 1.65 V to 5.5 V, unless otherwise specified. (continued)

Symbol	Parameter	Conditions	T_A = –55 °C to +125 °C			Unit
			Min	Typ	Max	
I/Os						
I_{LL}	Input Leakage Current	V_{DD} = 5.5 V; V_I = 0 V			–1	μA
$C_{I/O}$	Input / Output Capacitance (Note 7)			5.0	6.0	pF
INTERRUPT ($\overline{INT}$)						
I_{OL}	Low-Level Output Current	V_{OL} = 0.4 V	6.0			mA
C_O	Output Capacitance			5.0	5.5	pF
INPUTS AD0, AD1, AD2						
V_{IH}	High-Level Input Voltage		0.7 x V_{DD}			V
V_{IL}	Low-Level Input Voltage				0.3 x V_{DD}	V
I_L	Leakage Current	V_I = V_{DD} or 0 V			±1	μA
C_I	Input Capacitance			4.5	5.0	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. The power-on reset circuit resets the I^2C bus logic with $V_{DD} < V_{POR+}$ and set all I/Os to inputs upon power-up. Thereafter, V_{DD} must be lower than V_{POR-} to reset the part.
6. Each bit must be limited to a maximum of 25 mA and the total package limited to 200 mA due to internal bussing limits.
7. The value is not tested, but verified on sampling basis.

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Table 5. AC ELECTRICAL CHARACTERISTICS V_{DD} = 1.65 V to 5.5 V; T_A = −55 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Standard Mode		Fast Mode		Fast Mode +		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0	0.1	0	0.4	0	1.0	MHz
t_{BUF}	Bus-Free Time between a STOP and START Condition	4.7		1.3		0.5		μs
$t_{HD:STA}$	Hold Time (Repeated) START Condition	4.0		0.6		0.26		μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	4.7		0.6		0.26		μs
$t_{SU:STO}$	Setup Time for STOP Condition	4.0		0.6		0.26		μs
$t_{HD:DAT}$	Data Hold Time	0		0		0		ns
$t_{VD:ACK}$	Data Valid Acknowledge Time (Note 8)		3.45		0.9		0.45	μs
$t_{VD:DAT}$	Data Valid Time (Note 9)		3.45		0.9		0.45	μs
$t_{SU:DAT}$	Data Setup Time	250		100		50		ns
t_{LOW}	LOW Period of SCL	4.7		1.3		0.5		μs
t_{HIGH}	HIGH Period of SCL	4.0		0.6		0.26		μs
t_f	Fall Time of SDA and SCL (Notes 11 and 12)		300	20 + 0.1C_b (Note 10)	300		120	ns
t_r	Rise Time of SDA and SCL		1000	20 + 0.1C_b (Note 10)	300		120	ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter (Note 13)		50		50		50	ns
PORT TIMING: C_L ≤ 100 pF (See Figures 6, 9 and 10)								
$t_{V(Q)}$	Data Output Valid Time (V_{DD} = 4.5 V to 5.5 V) (V_{DD} = 2.3 V to 4.5 V) (V_{DD} = 1.65 V to 2.3 V)		300 350 550		300 350 550		300 350 550	ns
$t_{SU(D)}$	Data Input Setup Time	100		100		100		ns
$t_{H(D)}$	Data Input Hold Time	1		1		1		μs
INTERRUPT TIMING: C_L ≤ 100 pF (See Figures 9 and 10)								
$t_{V(INT\_N)}$	Data Valid Time		4		4		4	μs
$t_{RST(INT\_N)}$	Reset Delay Time		4		4		4	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. $t_{VD:ACK}$ = time for Acknowledgment signal from SCL LOW to SDA (out) LOW.
9. $t_{VD:DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
10. C_b = total capacitance of one bus line in pF.
11. A controller device must internally provide a hold time of al least 300 ns for the SDA signal (refer to V_{IL} of the SCL signal) in order to bridge the undefined region SCL's falling edge.
12. The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
13. Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

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Device Address

Before the bus controller can access a target device, it must send the address of the target it is accessing and the operation it wants to perform (read or write) following a START condition. The target address of the NLA9535/NLA9535C is shown in Figure 5. Address pins AD2, AD1, and AD0 choose 1 of 64 target addresses. To conserve power, no internal pull-up resistors are provided on AD2, AD1, and AD0.

A logic 1 on the last bit of the first byte selects a read operation while a logic 0 selects a write operation.

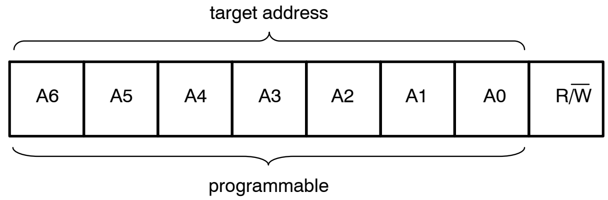

Figure 5. NLA9535/NLA9535C device Address

Table 6. NLA9535/NLA9535C ADDRESS MAP

Address Input			Target Address							
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	HEX
GND	SCL	GND	0	0	1	0	0	0	0	20h
GND	SCL	VDD	0	0	1	0	0	0	1	22h
GND	SDA	GND	0	0	1	0	0	1	0	24h
GND	SDA	VDD	0	0	1	0	0	1	1	26h
VDD	SCL	GND	0	0	1	0	1	0	0	28h
VDD	SCL	VDD	0	0	1	0	1	0	1	2Ah
VDD	SDA	GND	0	0	1	0	1	1	0	2Ch
VDD	SDA	VDD	0	0	1	0	1	1	1	2Eh
GND	SCL	SCL	0	0	1	1	0	0	0	30h
GND	SCL	SDA	0	0	1	1	0	0	1	32h
GND	SDA	SCL	0	0	1	1	0	1	0	34h
GND	SDA	SDA	0	0	1	1	0	1	1	36h
VDD	SCL	SCL	0	0	1	1	1	0	0	38h
VDD	SCL	SDA	0	0	1	1	1	0	1	3Ah
VDD	SDA	SCL	0	0	1	1	1	1	0	3Ch
VDD	SDA	SDA	0	0	1	1	1	1	1	3Eh
GND	GND	GND	0	1	0	0	0	0	0	40h
GND	GND	VDD	0	1	0	0	0	0	1	42h
GND	VDD	GND	0	1	0	0	0	1	0	44h
GND	VDD	VDD	0	1	0	0	0	1	1	46h
VDD	GND	GND	0	1	0	0	1	0	0	48h
VDD	GND	VDD	0	1	0	0	1	0	1	4Ah
VDD	VDD	GND	0	1	0	0	1	1	0	4Ch
VDD	VDD	VDD	0	1	0	0	1	1	1	4Eh
GND	GND	SCL	0	1	0	1	0	0	0	50h
GND	GND	SDA	0	1	0	1	0	0	1	52h
GND	VDD	SCL	0	1	0	1	0	1	0	54h
GND	VDD	SDA	0	1	0	1	0	1	1	56h
VDD	GND	SCL	0	1	0	1	1	0	0	58h
VDD	GND	SDA	0	1	0	1	1	0	1	5Ah
VDD	VDD	SCL	0	1	0	1	1	1	0	5Ch

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Table 6. NLA9535/NLA9535C ADDRESS MAP (continued)

Address Input			Target Address							
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	HEX
VDD	VDD	SDA	0	1	0	1	1	1	1	5Eh
SCL	SCL	GND	1	0	1	0	0	0	0	A0h
SCL	SCL	VDD	1	0	1	0	0	0	1	A2h
SCL	SDA	GND	1	0	1	0	0	1	0	A4h
SCL	SDA	VDD	1	0	1	0	0	1	1	A6h
SDA	SCL	GND	1	0	1	0	1	0	0	A8h
SDA	SCL	VDD	1	0	1	0	1	0	1	AAh
SDA	SDA	GND	1	0	1	0	1	1	0	ACh
SDA	SDA	VDD	1	0	1	0	1	1	1	AEh
SCL	SCL	SCL	1	0	1	1	0	0	0	B0h
SCL	SCL	SDA	1	0	1	1	0	0	1	B2h
SCL	SDA	SCL	1	0	1	1	0	1	0	B4h
SCL	SDA	SDA	1	0	1	1	0	1	1	B6h
SDA	SCL	SCL	1	0	1	1	1	0	0	B8h
SDA	SCL	SDA	1	0	1	1	1	0	1	BAh
SDA	SDA	SCL	1	0	1	1	1	1	0	BCh
SDA	SDA	SDA	1	0	1	1	1	1	1	BEh
SCL	GND	GND	1	1	0	0	0	0	0	C0h
SCL	GND	VDD	1	1	0	0	0	0	1	C2h
SCL	VDD	GND	1	1	0	0	0	1	0	C4h
SCL	VDD	VDD	1	1	0	0	0	1	1	C6h
SDA	GND	GND	1	1	0	0	1	0	0	C8h
SDA	GND	VDD	1	1	0	0	1	0	1	CAh
SDA	VDD	GND	1	1	0	0	1	1	0	CCh
SDA	VDD	VDD	1	1	0	0	1	1	1	CEh
SCL	GND	SCL	1	1	1	0	0	0	0	E0h
SCL	GND	SDA	1	1	1	0	0	0	1	E2h
SCL	VDD	SCL	1	1	1	0	0	1	0	E4h
SCL	VDD	SDA	1	1	1	0	0	1	1	E6h
SDA	GND	SCL	1	1	1	0	1	0	0	E8h
SDA	GND	SDA	1	1	1	0	1	0	1	EAh
SDA	VDD	SCL	1	1	1	0	1	1	0	ECh
SDA	VDD	SDA	1	1	1	0	1	1	1	EEh

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REGISTERS

Command Byte

During a write transmission, the address byte is followed by the command byte. The command byte determines which of the following registers will be written or read.

Table 7. COMMAND BYTE

COMMAND	REGISTER
0	Input Port 0
1	Input Port 1
2	Output Port 0
3	Output Port 1
4	Polarity Inversion Port 0
5	Polarity Inversion Port 1
6	Configuration Port 0
7	Configuration Port 1

Registers 0 and 1: Input Port Registers

These registers are input-only. They reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Registers 6 or 7. Writes to these registers have no effect.

The externally-applied logic level determines the default value ‘X’.

Table 8. INPUT PORT 0 REGISTER

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 9. INPUT PORT 1 REGISTER

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

Registers 2 and 3: Output Port Registers

These registers are output-only. They reflect the outgoing logic levels of the pins defined as outputs by Registers 6 and 7. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the values that are in the flip-flops controlling the output selection, **not** the actual pin values.

Table 10. OUTPUT PORT 0 REGISTER

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 11. OUTPUT PORT 1 REGISTER

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

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Registers 4 and 5: Polarity Inversion Registers

These registers allow the polarity of the data in the input port registers to be inverted. The input port data polarity will be inverted when its corresponding bit in these registers is set (written with ‘1’), and retained when the bit is cleared (written with a ‘0’).

Table 12. POLARITY INVERSION PORT 0 REGISTER

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 13. POLARITY INVERSION PORT 1 REGISTER

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

Registers 6 and 7: Configuration Registers

The I/O pin directions are configured through the configuration registers. When a bit in the configuration registers is set (written with ‘1’), the bit’s corresponding port pin is enabled as an input with the output driver in high-impedance. When a bit is cleared (written with ‘0’), the corresponding port pin is enabled as an output. At reset, the device’s ports are inputs.

Table 14. CONFIGURATION PORT 0 REGISTER

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 15. CONFIGURATION PORT 1 REGISTER

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

Power-on Reset

Upon application of power, an internal Power-On Reset (POR) holds the NLA9535/NLA9535C in a reset condition while V_{DD} is ramping up. When V_{DD} has reached V_{POR+}, the reset condition is released and the NLA9535/NLA9535C registers and I^{2}C– and SMBus state machine will initialize to their default states. The reset is typically completed by the POR and the part enabled by the time the power supply is above V_{POR+}. However, when doing a power reset cycle, it is necessary to lower the power supply below V_{POR-}, and then restored to the operating voltage.

I/O Port (see Figure 2)

When an I/O pin is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V. In the case of NLA9535C, FET Q1 has been removed and the open-drain FET Q2 will function the same as NLA9535.

When the I/O pin is configured as an output on the NLA9535, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. With the NLA9535C, an external pullup is required to pull the I/O pin HIGH when its corresponding output port register bit is a 1. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either V_{DD} or V_{SS}.

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BUS TRANSACTIONS

Writing to the Port Registers

To transmit data to the NLA9535/NLA9535C, the bus controller must first send the device address with the least significant bit set to logic 0 (see Figure 5). The command byte is sent after the address and determines which registers will receive the data following the command byte.

There are eight registers within the NLA9535/ NLA9535C. These registers are configured to operate as four register pairs: Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. Data bytes are sent alternately to each register in a register pair (see Figures 6 and 7). For example, if one byte is sent to Output Port 1 (register 3), then the next byte will be stored in Output Port 0 (register 2). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

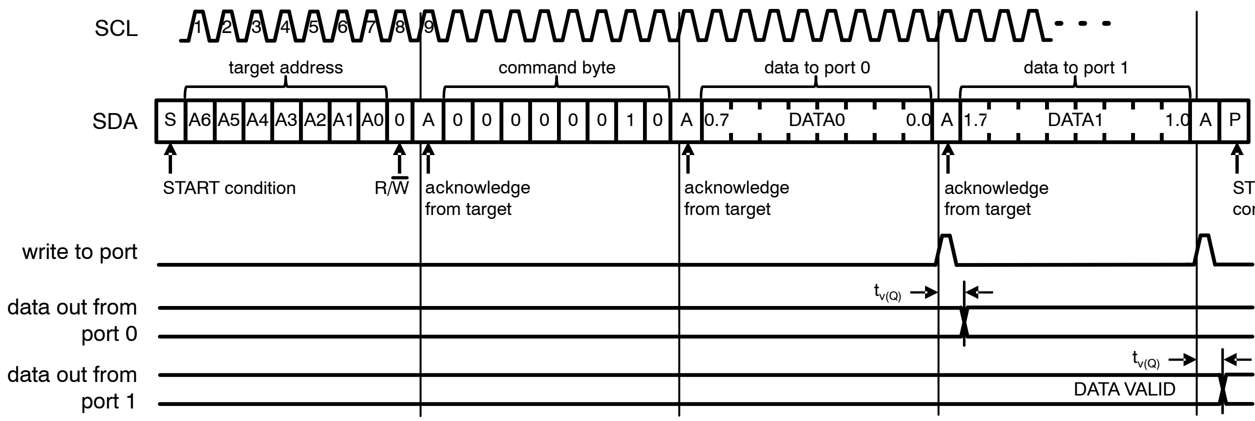

Figure 6. Write to Output Port Registers

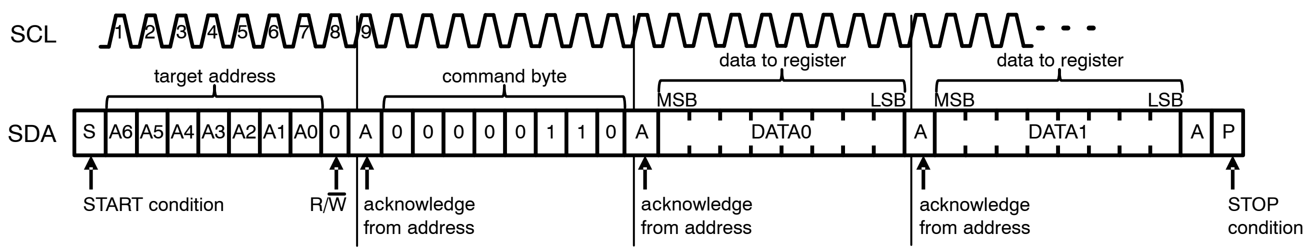

Figure 7. Write to Configuration Registers

Reading the Port Registers

To read data from the NLA9535/NLA9535C, the bus controller must first send the NLA9535/NLA9535C address with the least significant bit set to logic 0 (see Figure 5). The command byte is sent after the address and determines which register will be accessed.

After a restart, the device address must be sent again, but this time, the least significant bit is set to logic 1. Data from the register defined by the command byte will then be sent by the NLA9535/NLA9535C (see Figures 8, 9 and 10). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but with data alternately coming from each register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission but the bus controller must not acknowledge the data for the final byte received.

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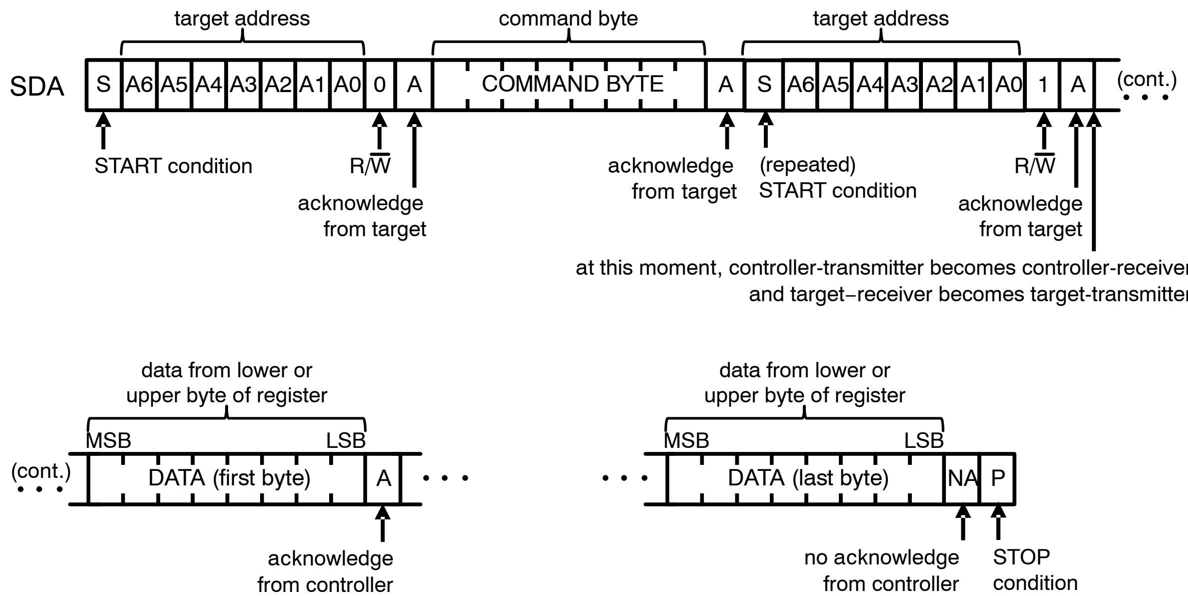
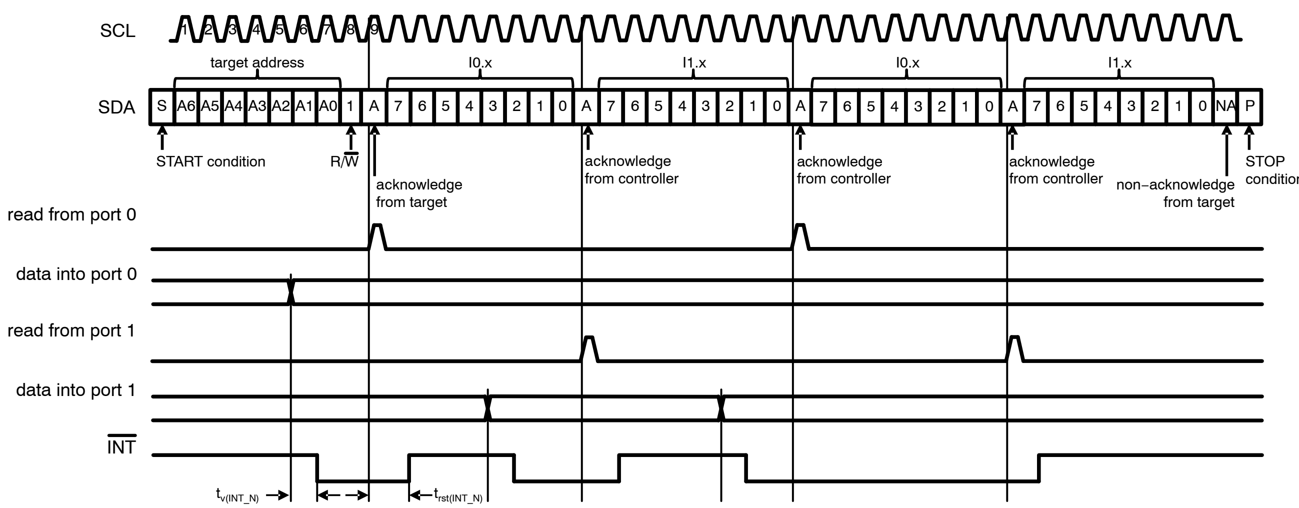


Remark: Transfer can be stopped at any time by a STOP condition.

Figure 8. Read from Register



Remark: Transfer of data can be stopped at any time by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Figure 9. Read from Input Port Register, Scenario 1

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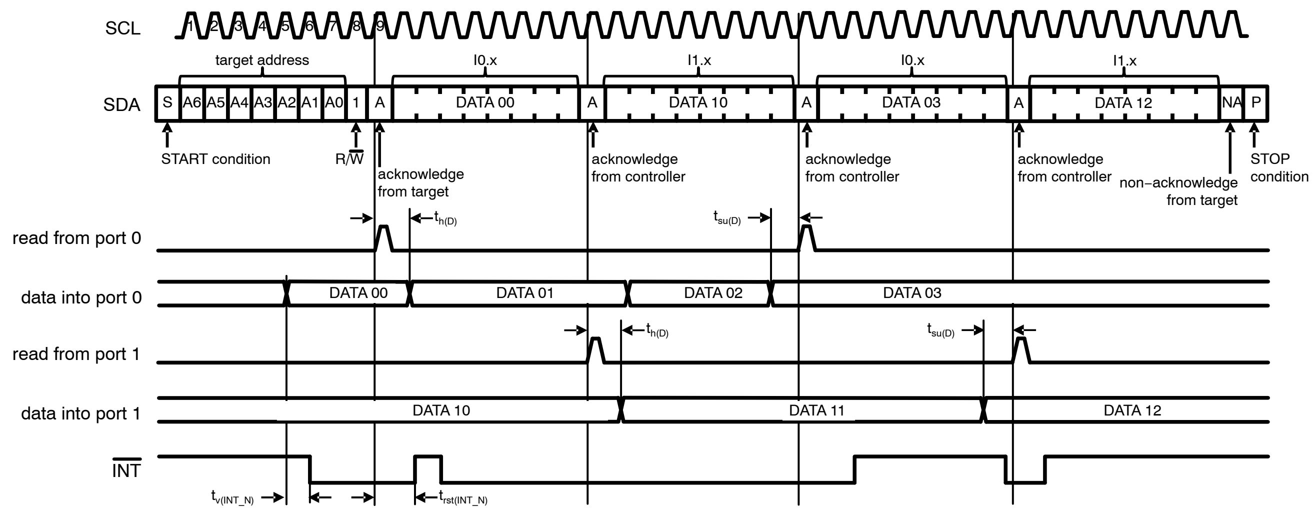

Remark: Transfer of data can be stopped at any time by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Figure 10. Read from Input Port Register, Scenario 2

Interrupt Output

The open-drain interrupt output is activated when an I/O pin configured as an input changes state. The interrupt is deactivated when the input pin returns to its previous state or when the Input Port register is read (see Figure 9). A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

Remark: Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

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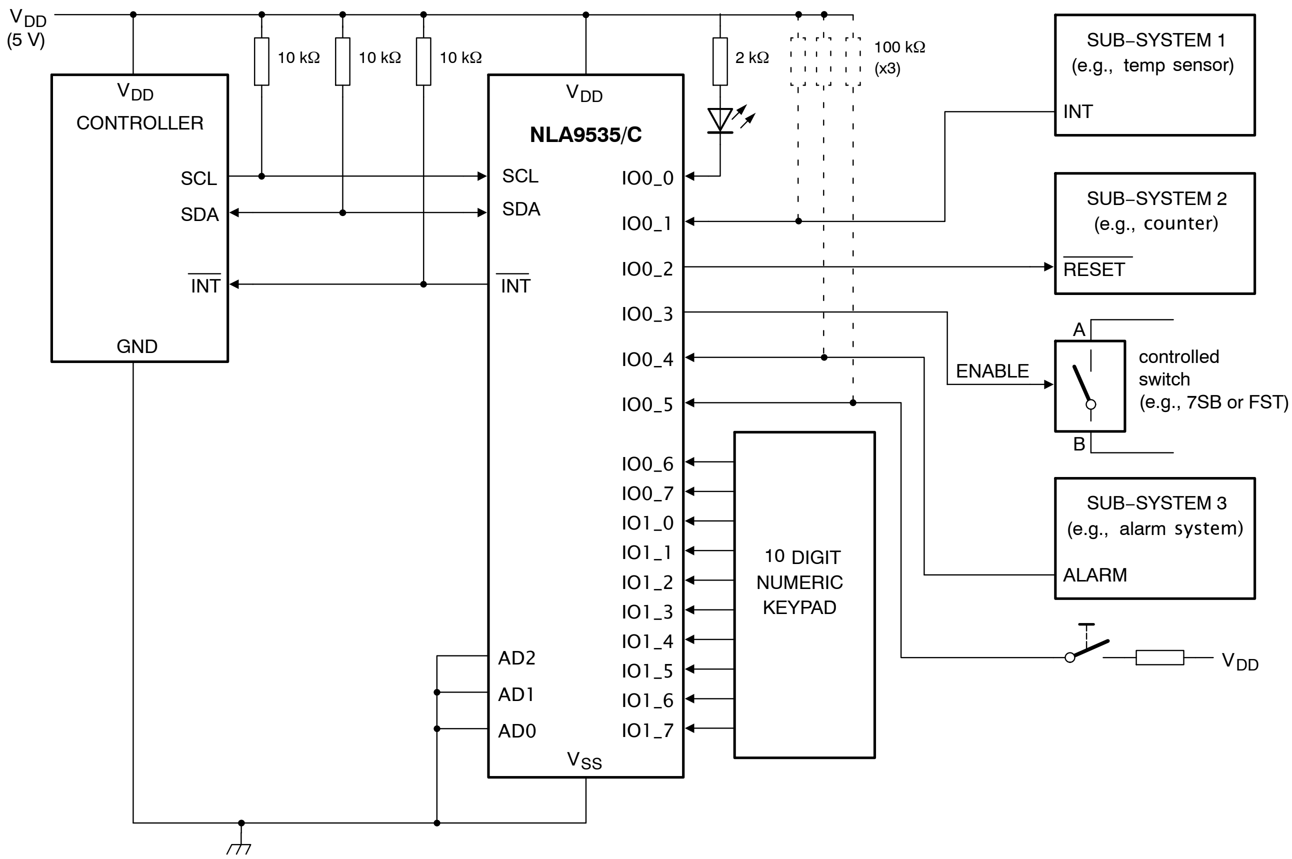
APPLICATION INFORMATION



Device address configured as 0100 000xb for this example.

IO0_2, IO0_3 configured as outputs.
IO0_0, IO0_1, IO0_4, IO0_5 configured as inputs.
IO0_6, IO0_7, and IO1_0 to IO1_7 configured as inputs.

Figure 11. Typical Application

Characteristics of the I^{2}C-Bus

The I^{2}C-bus is meant for 2-way, 2-line communication between different ICs or modules. The two lines are the serial data line (SDA) and the serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may only be initiated when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Changes in the data line during the HIGH period of the clock pulse will be interpreted as control signals (see Figure 12).

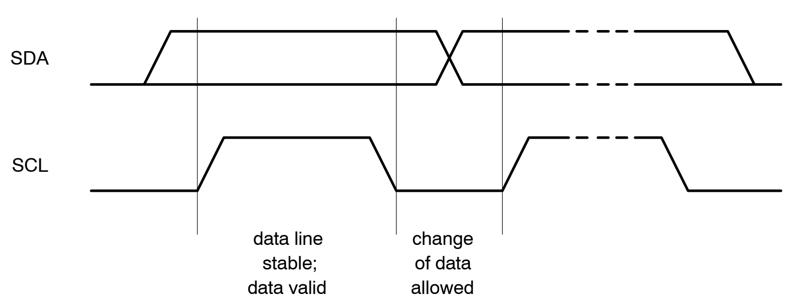


Figure 12. Bit Transfer

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START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A START condition (S) occurs when there is a HIGH-to-LOW transition of the data line while the clock is HIGH. A STOP condition (P) occurs when there is a LOW-to-HIGH transition of the data line while the clock is HIGH (see Figure 13).

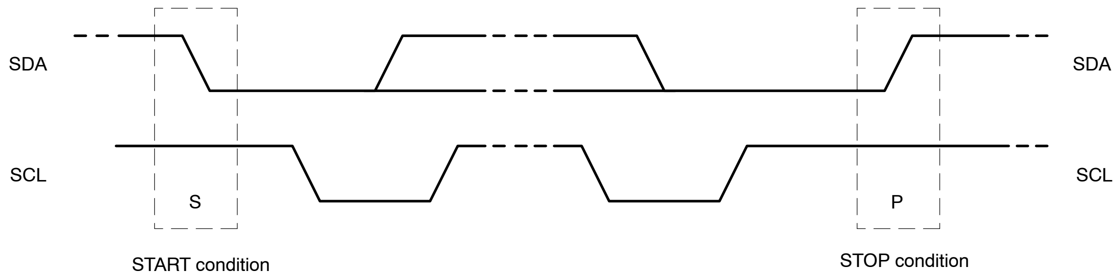

Figure 13. Definition of START and STOP Conditions

System Configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'controller' and the devices which are controlled by the controller are the 'targets' (see Figure 14).

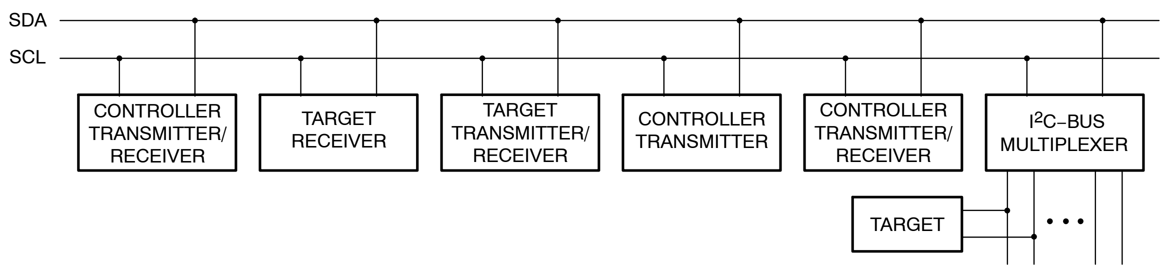

Figure 14. System Configuration

Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each 8-bit byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the controller generates an extra clock pulse for the acknowledge bit.

A target receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a controller must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, such that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse; set-up time and hold time must be taken into account.

A controller receiver signals an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the controller to generate a STOP condition.

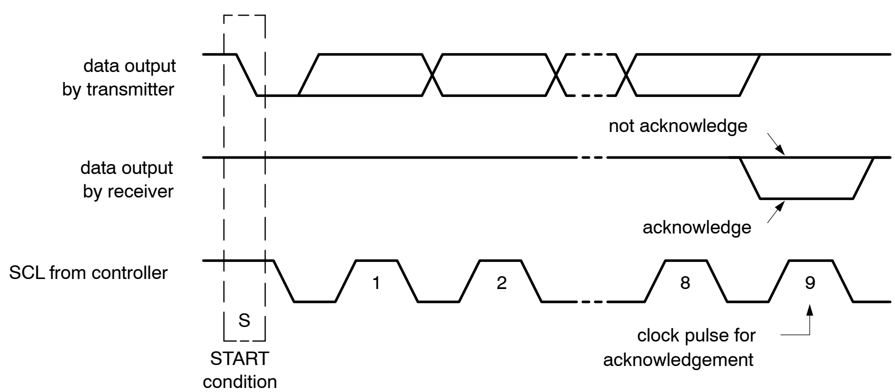

Figure 15. Acknowledgement of the I^{2}C Bus

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TIMING AND TEST SETUP

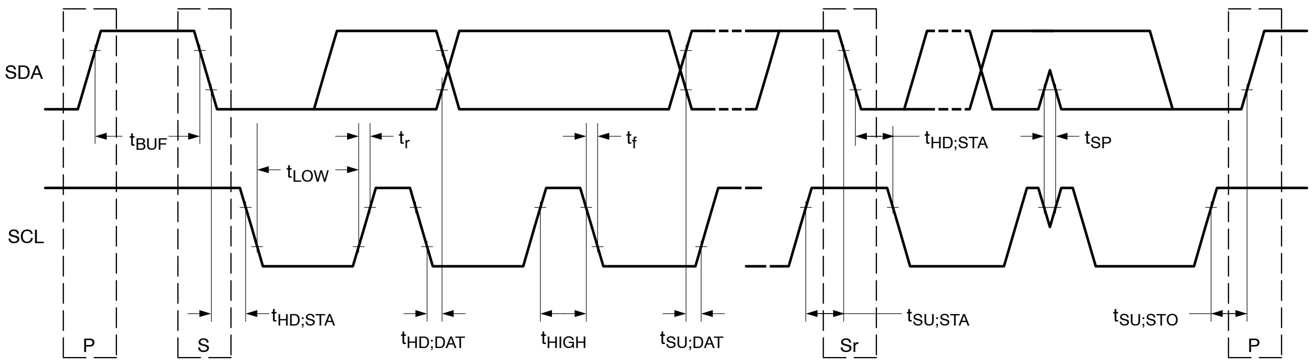
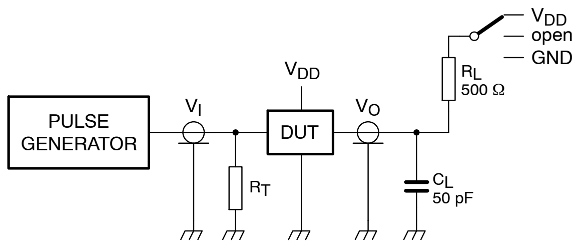


Figure 16. Definition of Timing on the I²C Bus



R_L = load resistor.
C_L = load capacitance includes jig and probe capacitance.
R_T = termination resistance should be equal to the output impedance of Z_o of the pulse generators.

Figure 17. Test Circuitry for Switching Times

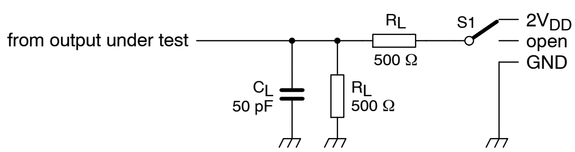


Figure 18. Load Circuit

Table 16. ORDERING INFORMATION

Device	Marking	Package	Shipping†
NLA9535DTR2G	NLA 9535	TSSOP-24 (Pb-Free)	2500 / Tape & Reel
NLA9535DTR2G-Q*	NLA 9535	TSSOP-24 (Pb-Free)	2500 / Tape & Reel
NLA9535MTTXG	NLA 9535	WQFN24 (Pb-Free)	3000 / Tape & Reel
NLA9535MTTXG-Q*	NLA 9535	WQFN24 (Pb-Free)	3000 / Tape & Reel
NLA9535CDTR2G	NLA 9535C	TSSOP-24 (Pb-Free)	2500 / Tape & Reel

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Table 16. ORDERING INFORMATION (continued)

Device	Marking	Package	Shipping†
NLA9535CDTR2G-Q*	NLA 9535C	TSSOP-24 (Pb-Free)	2500 / Tape & Reel
NLA9535CMTTXG	NLA 9535C	WQFN24 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
* -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

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REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	6/3/2026

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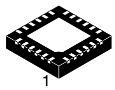
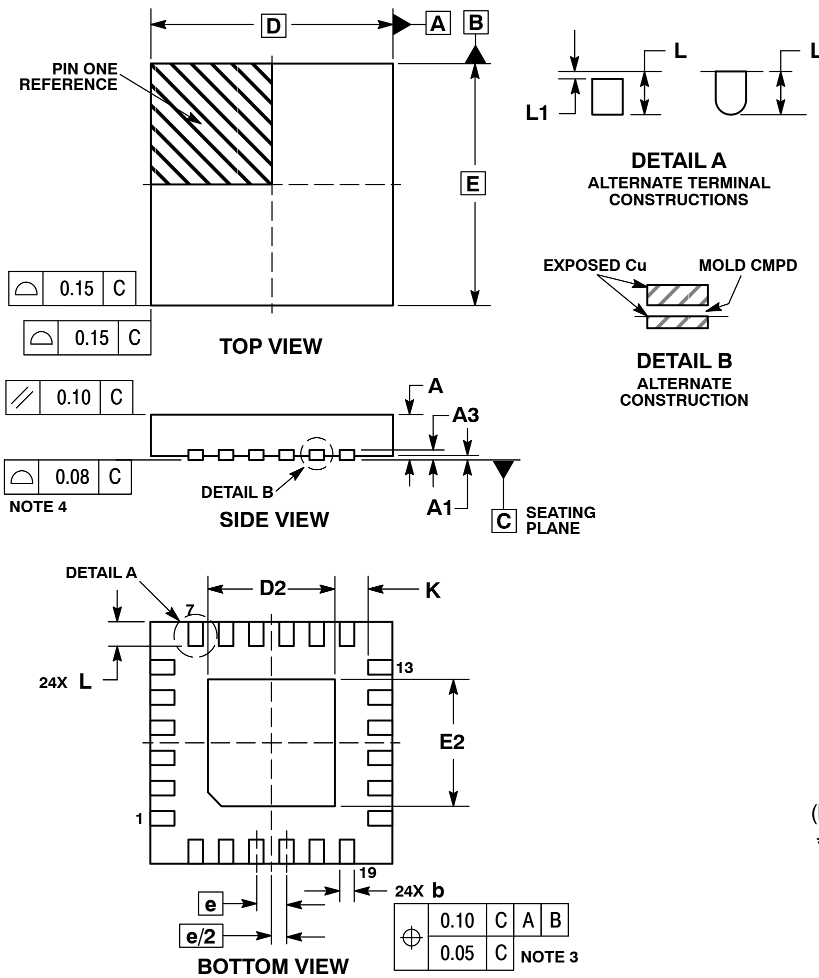
PACKAGE DIMENSIONS



SCALE 2:1

WQFN24 4x4, 0.5P
CASE 485BG
ISSUE A

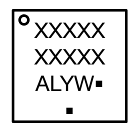
DATE 17 APR 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.00	2.20
E	4.00 BSC	
E2	2.00	2.20
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.15

GENERIC MARKING DIAGRAM*

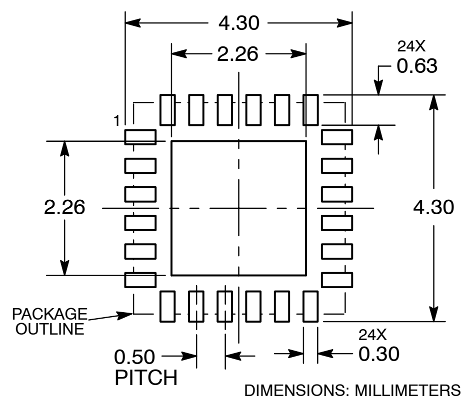


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

MOUNTING FOOTPRINT



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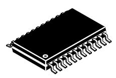
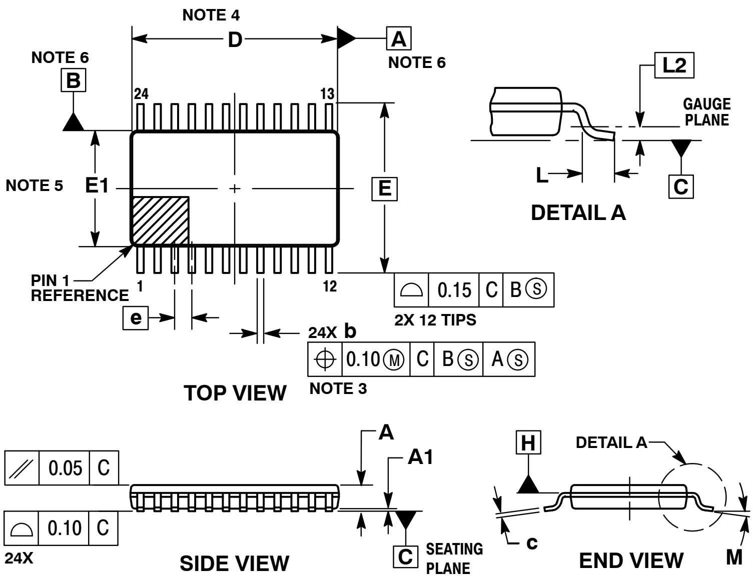


SCALE 1:1

TSSOP24 7.8x4.4, 0.65P
CASE 948H
ISSUE B

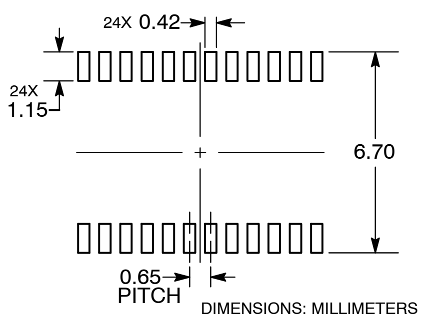
DATE 21 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

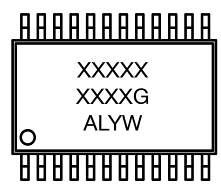
	MILLIMETERS	
DIM	MIN	MAX
A	---	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.50	0.75
L2	0.25 BSC	
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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