

# Configurable Multifunction Gate

## NL7SZ97

The NL7SZ97 is an advanced high-speed CMOS multifunction gate. The device allows the user to choose logic functions MUX, AND, OR, NAND, NOR, INVERT and BUFFER. The device has Schmitt-trigger inputs, thereby enhancing noise immunity.

### Features

- Designed for 1.65 V to 5.5 V  $V_{CC}$  Operation
- 3.3 ns  $t_{PD}$  at  $V_{CC} = 5\text{ V}$  (Typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- $I_{OFF}$  Supports Partial Power Down Protection
- Sink 24 mA at 3.0 V
- Available in SC-88 and SC-74 Packages
- Chip Complexity < 100 FETs
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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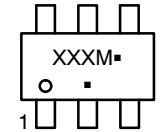
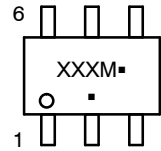
SC-88/SC70-6/  
SOT-363  
CASE 419B-02



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SC-74  
CASE 318F-05

### MARKING DIAGRAMS



XXX = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

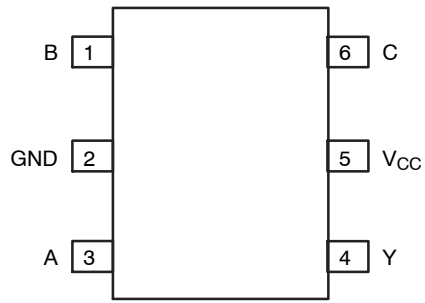
(Note: Microdot may be in either location or may not be present)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

# NL7SZ97



(SC-88 / SC-74)

Figure 1. Pinout (Top View)

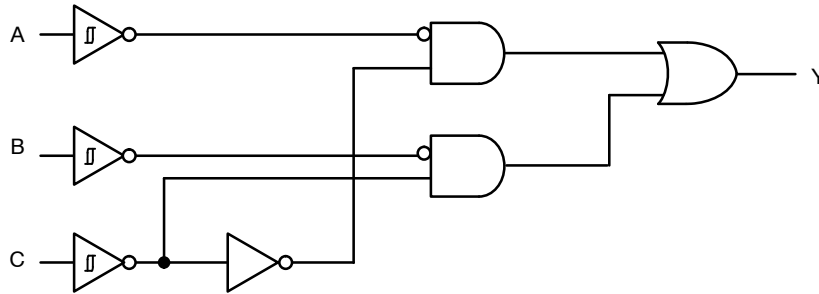


Figure 2. Function Diagram

## PIN ASSIGNMENT

Pin	Function
1	B
2	GND
3	A
4	Y
5	V <sub>CC</sub>
6	C

## FUNCTION TABLE\*

Input			Output
A	B	C	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	H
H	H	L	H
H	H	H	H

\* To select a logic function, please refer to "Logic Configurations section".

LOGIC CONFIGURATIONS

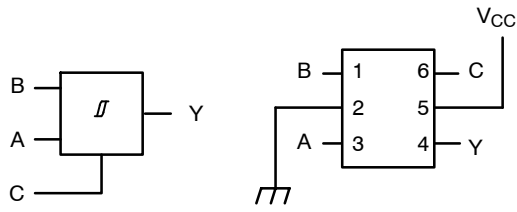


Figure 3. 2-Input MUX

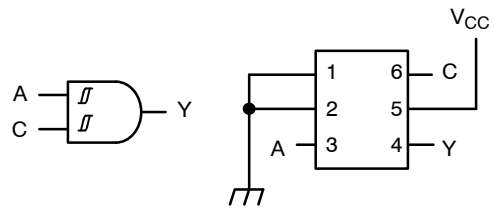


Figure 4. 2-Input AND (When B = "L")

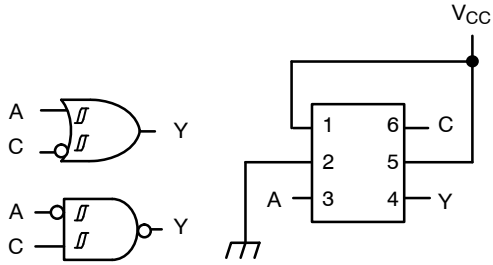


Figure 5. 2-Input OR with Input C Inverted (When B = "H")

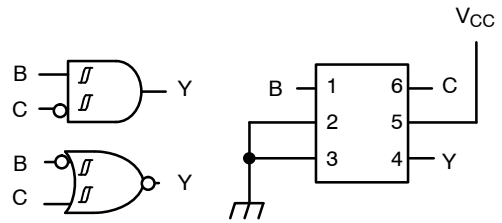


Figure 6. 2-Input AND with Input C Inverted (When A = "L")

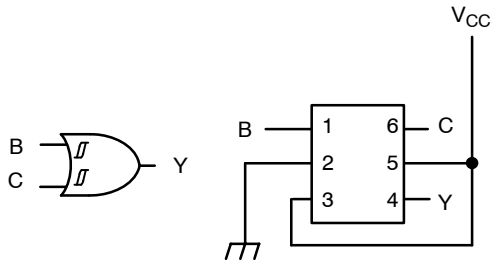


Figure 7. 2-Input OR (When A = "H")

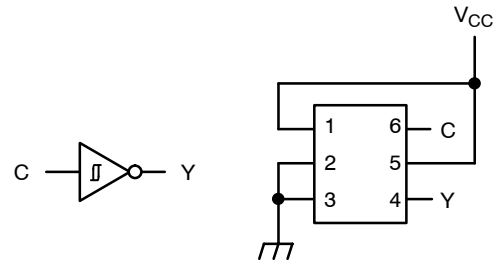


Figure 8. Inverter (When A = "L" and B = "H")

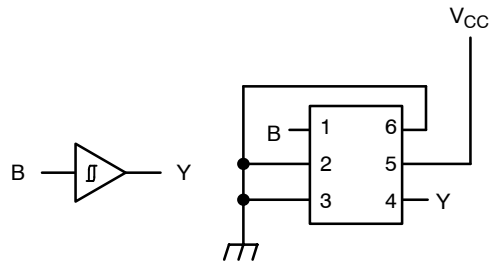


Figure 9. Buffer (When A = C = "L")

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +6.5	V
$V_{IN}$	DC Input Voltage	-0.5 to +6.5	V
$V_{OUT}$	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ( $V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +6.5 -0.5 to +6.5	V
$I_{IK}$	DC Input Diode Current $V_{IN} < GND$	-50	mA
$I_{OK}$	DC Output Diode Current $V_{OUT} < GND$	-50	mA
$I_{OUT}$	DC Output Source/Sink Current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC Supply Current per Supply Pin or Ground Pin	$\pm 100$	mA
$T_{STG}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature, 1 mm from Case for 10 Secs	260	$^{\circ}C$
$T_J$	Junction Temperature Under Bias	+150	$^{\circ}C$
$\theta_{JA}$	Thermal Resistance (Note 2)	SC-88 SC-74	$^{\circ}C/W$
$P_D$	Power Dissipation in Still Air	SC-88 SC-74	mW
MSL	Moisture Sensitivity	Level 1	
$F_R$	Flammability Rating Oxygen Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage (Note 3) Human Body Mode Charged Device Model	>2000 >200	V
$I_{LATCHUP}$	Latchup Performance (Note 4)	$\pm 100$	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow per JESD51-7.
3. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Positive DC Supply Voltage	1.65	5.5	V
$V_{IN}$	DC Input Voltage	0	5.5	V
$V_{OUT}$	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ( $V_{CC} = 0$ V)	0 0 0	$V_{CC}$ 5.5 5.5	V
$T_A$	Operating Free-Air Temperature	-55	+125	$^{\circ}C$
$t_r, t_f$	Input Rise or Fall Rate $V_{CC} = 1.65$ V to 1.95 V $V_{CC} = 2.3$ V to 2.7 V $V_{CC} = 3.0$ V to 3.6 V $V_{CC} = 4.5$ V to 5.5 V	0 0 0 0	No Limit No Limit No Limit No Limit	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25 °C			-40 °C ≤ T <sub>A</sub> ≤ 85 °C		-55 °C ≤ T <sub>A</sub> ≤ 125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V <sub>T+</sub>	Positive Input Threshold Voltage		1.65	-	-	1.4	-	1.4	-	1.4	V
			2.3	-	-	1.8	-	1.8	-	1.8	
			3.0	-	-	2.2	-	2.2	-	2.2	
			4.5	-	-	3.1	-	3.1	-	3.1	
			5.5	-	-	3.6	-	3.6	-	3.6	
V <sub>T-</sub>	Negative Input Threshold Voltage		1.65	0.2	-	-	0.2	-	0.2	-	V
			2.3	0.4	-	-	0.4	-	0.4	-	
			3.0	0.6	-	-	0.6	-	0.6	-	
			4.5	1.0	-	-	1.0	-	1.0	-	
			5.5	1.2	-	-	1.2	-	1.2	-	
V <sub>H</sub>	Negative Input Threshold Voltage		1.65	0.1	0.48	0.9	0.1	0.9	0.1	0.9	V
			2.3	0.25	0.75	1.1	0.25	1.1	0.25	1.1	
			3.0	0.4	0.93	1.2	0.4	1.2	0.4	1.2	
			4.5	0.6	1.2	1.5	0.6	1.5	0.6	1.5	
			5.5	0.7	1.4	1.7	0.7	1.7	0.7	1.7	
V <sub>OH</sub>	High-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	1.65 to 5.5	V <sub>CC</sub> - 0.1	V <sub>CC</sub>	-	V <sub>CC</sub> - 0.1	-	V <sub>CC</sub> - 0.1	-	V
		I <sub>OH</sub> = -4 mA	1.65	1.20	1.52	-	1.20	-	1.20	-	
		I <sub>OH</sub> = -8 mA	2.3	1.9	2.1	-	1.9	-	1.9	-	
		I <sub>OH</sub> = -16 mA	3	2.4	2.7	-	2.4	-	2.4	-	
		I <sub>OH</sub> = -24 mA	3	2.3	2.5	-	2.3	-	2.3	-	
		I <sub>OH</sub> = -32 mA	4.5	3.8	4	-	3.8	-	3.8	-	
V <sub>OL</sub>	Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	1.65 to 5.5	-	-	0.1	-	0.1	-	0.1	V
		I <sub>OL</sub> = 4 mA	1.65	-	0.08	0.45	-	0.45	-	0.45	
		I <sub>OL</sub> = 8 mA	2.3	-	0.2	0.3	-	0.3	-	0.4	
		I <sub>OL</sub> = 16 mA	3	-	0.28	0.4	-	0.4	-	0.5	
		I <sub>OL</sub> = 24 mA	3	-	0.38	0.55	-	0.55	-	0.55	
		I <sub>OL</sub> = 32 mA	4.5	-	0.42	0.55	-	0.55	-	0.65	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	1.65 to 5.5	-	-	+0.1	-	+1.0	-	+1.0	μA
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>IN</sub> = 5.5 V or V <sub>OUT</sub> = 5.5 V	0	-	-	1.0	-	10	-	10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = 5.5 V or GND	5.5	-	-	1.0	-	10	-	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25 °C			-40 °C ≤ T <sub>A</sub> ≤ 85 °C		-55 °C ≤ T <sub>A</sub> ≤ 125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
				t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, (A or B or C) to Y (Figures 10 and 11)	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 30 pF	1.65 to 1.95	-	8.6	14.4	
R <sub>L</sub> = 500 Ω, C <sub>L</sub> = 30 pF	2.3 to 2.7	-	5.1	8.3		-	8.3	-	8.3		
R <sub>L</sub> = 500 Ω, C <sub>L</sub> = 50 pF	3.0 to 3.6	-	3.9	6.3		-	6.3	-	6.3		
	4.5 to 5.5	-	3.3	5.1		-	5.1	-	5.1		

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub>	2.5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub>	4.0	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)	10 MHz, V <sub>CC</sub> = 3.3 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub> 10 MHz, V <sub>CC</sub> = 5.0 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub>	16 19.5	pF

5. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

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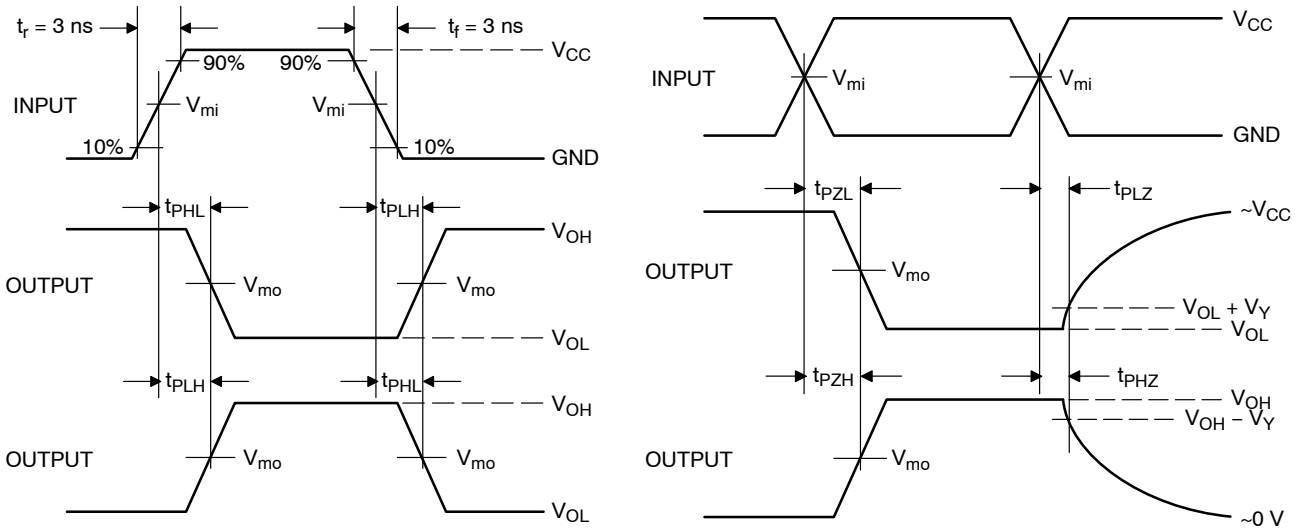


$C_L$  includes probe and jig capacitance  
 $R_T$  is  $Z_{OUT}$  of pulse generator (typically 50  $\Omega$ )  
 $f = 1$  MHz

**Figure 10. Test Circuit**

Test	Switch Position	$C_L$ , pF	$R_L$ , $\Omega$	$R_1$ , $\Omega$
$t_{PLH} / t_{PHL}$	Open	See AC Characteristics Table		
$t_{PLZ} / t_{PZL}$	$2 \times V_{CC}$	50	500	500
$t_{PHZ} / t_{PZH}$	GND	50	500	500

X = Don't Care



**Figure 11. Switching Waveforms**

$V_{CC}$ , V	$V_{mi}$ , V	$V_{mo}$ , V		$V_y$ , V
		$t_{PLH}, t_{PHL}$	$t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}$	
1.65 to 1.95	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	0.15
2.3 to 2.7	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	0.15
3.0 to 3.6	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	0.3
4.5 to 5.5	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	0.3

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## DEVICE ORDERING INFORMATION

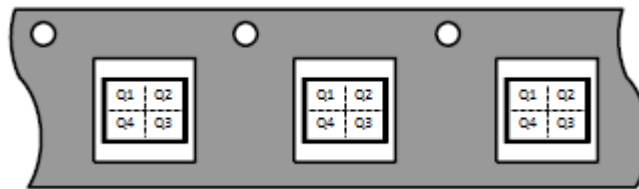
Device	Package	Specific Device Code	Pin 1 Orientation (See below)	Shipping <sup>†</sup>
NL7SZ97DFT2G	SC-88 (Pb-Free)	MK	Q4	3000 / Tape & Reel
NL7SZ97DFT2G-Q*	SC-88 (Pb-Free)	MK	Q4	3000 / Tape & Reel
NL7SZ97DBVT1G	SC-74 (Pb-Free)	AN	Q4	3000 / Tape & Reel

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

\* -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC\*Q101 Qualified and PPAP Capable.

### Pin 1 Orientation in Tape and Reel

Direction of Feed



## REVISION HISTORY

Revision	Description of Changes	Date
11	Removed three package ordering options and OPNs	02/02/2026

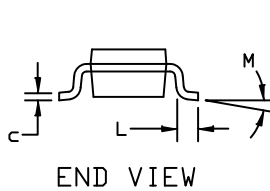
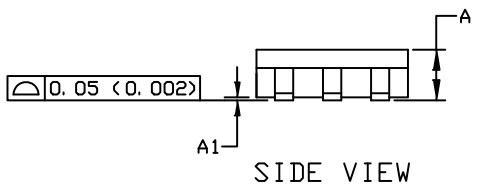
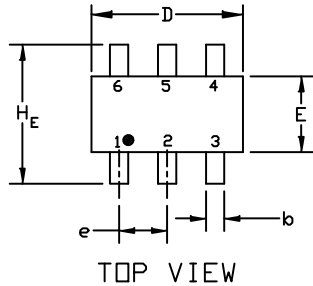
\* Please note that this document has been previously updated prior to the inclusion of this revision history table and that the changes tracked only reflect what has occurred on the noted approval dates.



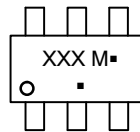
SCALE 2:1

SC-74  
CASE 318F  
ISSUE P

DATE 07 OCT 2021



GENERIC  
MARKING DIAGRAM\*



XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

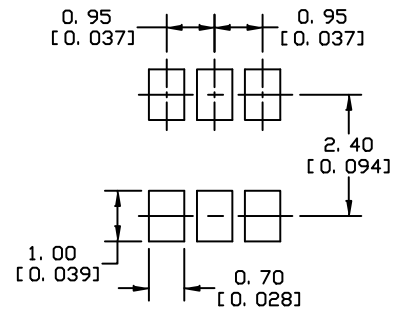
(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. CONTROLLING DIMENSION: INCHES
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
HE	2.50	2.75	3.00	0.099	0.108	0.118
L	0.20	0.40	0.60	0.008	0.016	0.024
M	0*	---	10*	0*	---	10*



\* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

SOLDERING FOOTPRINT

- |   |  |   |  |   |   |
|---|--|---|--|---|---|
| <p>STYLE 1:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. CATHODE<br/>4. CATHODE<br/>5. ANODE<br/>6. CATHODE</p>     | <p>STYLE 2:<br/>PIN 1. NO CONNECTION<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. NO CONNECTION<br/>5. COLLECTOR<br/>6. BASE</p> | <p>STYLE 3:<br/>PIN 1. EMITTER 1<br/>2. BASE 1<br/>3. COLLECTOR 2<br/>4. EMITTER 2<br/>5. BASE 2<br/>6. COLLECTOR 1</p> | <p>STYLE 4:<br/>PIN 1. COLLECTOR 2<br/>2. EMITTER 1/EMITTER 2<br/>3. COLLECTOR 1<br/>4. EMITTER 3<br/>5. BASE 1/BASE 2/COLLECTOR 3<br/>6. BASE 3</p> | <p>STYLE 5:<br/>PIN 1. CHANNEL 1<br/>2. ANODE<br/>3. CHANNEL 2<br/>4. CHANNEL 3<br/>5. CATHODE<br/>6. CHANNEL 4</p> | <p>STYLE 6:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. CATHODE<br/>4. CATHODE<br/>5. CATHODE<br/>6. CATHODE</p> |
| <p>STYLE 7:<br/>PIN 1. SOURCE 1<br/>2. GATE 1<br/>3. DRAIN 2<br/>4. SOURCE 2<br/>5. GATE 2<br/>6. DRAIN 1</p> | <p>STYLE 8:<br/>PIN 1. EMITTER 1<br/>2. BASE 2<br/>3. COLLECTOR 2<br/>4. EMITTER 2<br/>5. BASE 1<br/>6. COLLECTOR 1</p>    | <p>STYLE 9:<br/>PIN 1. EMITTER 2<br/>2. BASE 2<br/>3. COLLECTOR 1<br/>4. EMITTER 1<br/>5. BASE 1<br/>6. COLLECTOR 2</p> | <p>STYLE 10:<br/>PIN 1. ANODE/CATHODE<br/>2. BASE<br/>3. EMITTER<br/>4. COLLECTOR<br/>5. ANODE<br/>6. CATHODE</p>                                    | <p>STYLE 11:<br/>PIN 1. EMITTER<br/>2. BASE<br/>3. ANODE/CATHODE<br/>4. ANODE<br/>5. CATHODE<br/>6. COLLECTOR</p>   |   |

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DESCRIPTION:	SC-74	PAGE 1 OF 1

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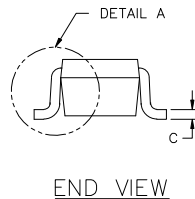
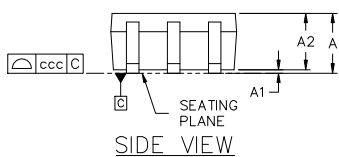
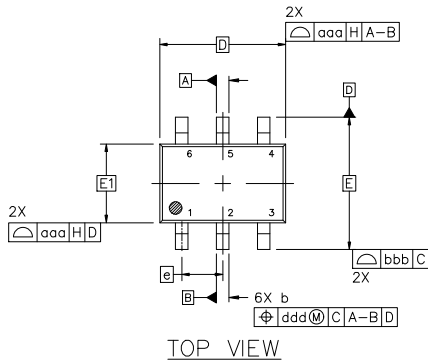


SC-88 2.00x1.25x0.90, 0.65P  
CASE 419B-02  
ISSUE Z

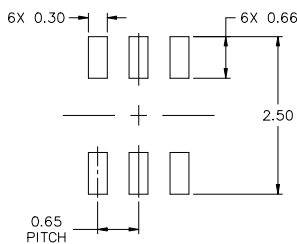
DATE 18 APR 2024

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

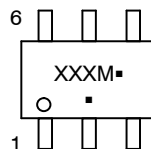


DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.00	---	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



\* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



XXX = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	SC-88 2.00x1.25x0.90, 0.65P	PAGE 1 OF 2

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**SC-88 2.00x1.25x0.90, 0.65P**  
**CASE 419B-02**  
**ISSUE Z**

DATE 18 APR 2024

<b>STYLE 1:</b> PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	<b>STYLE 2:</b> CANCELLED	<b>STYLE 3:</b> CANCELLED	<b>STYLE 4:</b> PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	<b>STYLE 5:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 6:</b> PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
<b>STYLE 7:</b> PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	<b>STYLE 8:</b> CANCELLED	<b>STYLE 9:</b> PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	<b>STYLE 10:</b> PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	<b>STYLE 11:</b> PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	<b>STYLE 12:</b> PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
<b>STYLE 13:</b> PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 14:</b> PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	<b>STYLE 15:</b> PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	<b>STYLE 16:</b> PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	<b>STYLE 17:</b> PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	<b>STYLE 18:</b> PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
<b>STYLE 19:</b> PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	<b>STYLE 20:</b> PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	<b>STYLE 21:</b> PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	<b>STYLE 22:</b> PIN 1. D1 (i) 2. GND 3. D2 (j) 4. D2 (c) 5. VBUS 6. D1 (c)	<b>STYLE 23:</b> PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	<b>STYLE 24:</b> PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
<b>STYLE 25:</b> PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	<b>STYLE 26:</b> PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	<b>STYLE 27:</b> PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	<b>STYLE 28:</b> PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	<b>STYLE 29:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	<b>STYLE 30:</b> PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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