

# 2-Bit 24 Mbps Configurable Dual-Supply Autosense Level Translator

## NL5X4002

The NL5X4002 is a 2-bit configurable dual-supply bidirectional auto sensing translator that does not require directional control pins. The A and B ports are designed to track two different power supply rails,  $V_{CCA}$  and  $V_{CCB}$  respectively. Both the  $V_{CCA}$  and  $V_{CCB}$  supply rails are configurable from 1.65 V to 5.5 V. This allows voltage logic signals on the  $V_{CCA}$  side to be translated into lower, higher or equal value voltage logic signals on the  $V_{CCB}$  side, and vice-versa.

The NL5X4002 translator has integrated 10 k $\Omega$  pullup resistors on the I/O lines. The integrated pullup resistors are used to pull the I/O lines up to either  $V_{CCA}$  or  $V_{CCB}$ .

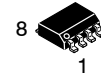
These devices are excellent matches for open-drain applications such as the I<sup>2</sup>C communication bus.

### Features

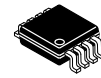
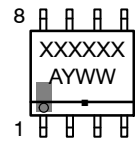
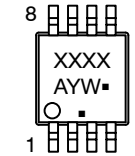
- Wide  $V_{CCA}$ ,  $V_{CCB}$  Operating Range: 1.65 V to 5.5 V
- $V_{CCA}$  and  $V_{CCB}$  are independent
  - $V_{CCA}$  may be greater than, equal to, or less than  $V_{CCB}$
- High-Speed w/ 24 Mbps Guaranteed Data Rate
- Low Bit-to-Bit skew
- Overvoltage Tolerant Enable and I/O Pins
- Non-preferential Power-Up Sequencing
- Integrated 10 k $\Omega$  Pullup Resistors (NL5X4002)
- Available packaging: SOIC-8, Micro8, UDFN8
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- I<sup>2</sup>C, SMBus, PMBus
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Cameras

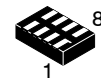
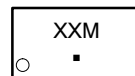

**SOIC-8 NB**  
**CASE 751**

### MARKING DIAGRAMS


**Micro8**  
**CASE 846A**


- XXXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)


**UDFN8**  
**CASE 517AJ**


- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

# NL5X4002

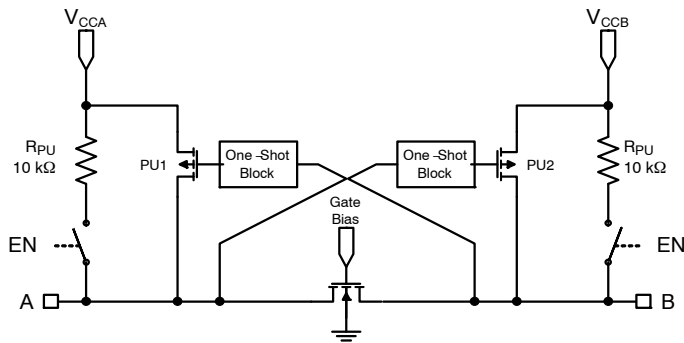


Figure 1. NL5X4002 Block Diagram (1 I/O Line)

## PIN ASSIGNMENTS

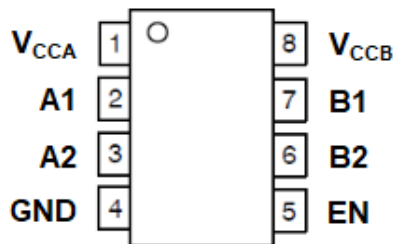


Figure 2. SOIC-8/Micro8

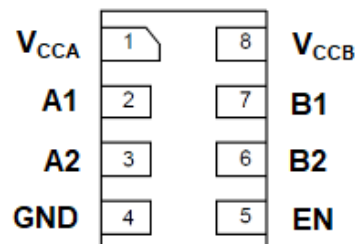


Figure 3. UDFN8

## PIN DESCRIPTIONS

Pin	Description
V <sub>CCA</sub>	A-Port Supply Voltage
V <sub>CCB</sub>	B-Port Supply Voltage
GND	Ground
An	A-Port, Referenced to V <sub>CCA</sub>
Bn	B-Port, Referenced to V <sub>CCB</sub>
EN	Enable, Referenced to V <sub>CCA</sub>

## FUNCTION TABLE

EN	Operating Mode
L	An and Bn at Hi-Z
H	An and Bn Connected

# NL5X4002

## MAXIMUM RATINGS

Symbol	Parameter	Condition	Value	Unit
V <sub>CCA</sub>	A-side DC Supply Voltage		-0.5 to +6.5	V
V <sub>CCB</sub>	B-side DC Supply Voltage		-0.5 to +6.5	V
V <sub>EN</sub>	EN Pin Input Voltage		-0.5 to +6.5	V
V <sub>IO</sub>	Input/Output Voltage	Active Mode (A-Port) Active Mode (B-Port) Tri-State Mode (EN = L) Power Down Mode (V <sub>CCA</sub> and/or V <sub>CCB</sub> = 0 V)	-0.5 to V <sub>CCA</sub> +0.5 -0.5 to V <sub>CCB</sub> +0.5 -0.5 to +6.5 -0.5 to +6.5	V
I <sub>IOK</sub>	Input/Output Clamp Current	V <sub>IO</sub> < GND	-50	mA
I <sub>IO_SC</sub>	Input/Output Short Circuit Current	Continuous	±50	mA
I <sub>CCA</sub>	DC Supply Current Through V <sub>CCA</sub>		±100	mA
I <sub>CCB</sub>	DC Supply Current Through V <sub>CCB</sub>		±100	mA
I <sub>GND</sub>	DC Ground Current Through Ground Pin		±100	mA
T <sub>STG</sub>	Storage Temperature		-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Note 1)	SOIC-8 Micro8 UDFN8	134 167 231	°C/W
P <sub>D</sub>	Power Dissipation in Still Air	SOIC-8 Micro8 UDFN8	935 748 541	mW
MSL	Moisture Sensitivity		Level 1	
F <sub>R</sub>	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	Bn to GND or V <sub>CCB</sub> All Pins 8000 2000 1000	V
I <sub>LATCHUP</sub>	Latchup Performance	Above V <sub>CC</sub> and Below GND (Note 3)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow per JESD51-7.
2. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
3. Tested to EIA/JESD78 Class II.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CCA</sub>	A-Port Supply Voltage	1.65	5.5	V	
V <sub>CCB</sub>	B-Port Supply Voltage	1.65	5.5	V	
V <sub>EN</sub>	EN Pin Input Voltage	GND	5.5	V	
V <sub>IO</sub>	Input/Output Voltage	Active Mode (A-Port) Active Mode (B-Port) Tri-State Mode (EN = L) Power Down Mode (V <sub>CCA</sub> and/or V <sub>CCB</sub> = 0 V)	GND GND GND GND	V <sub>CCA</sub> V <sub>CCB</sub> 5.5 5.5	V
T <sub>A</sub>	Operating Temperature Range	-40	+125	°C	
Δt/ΔV	Input Transition Rise or Fall Rate, V <sub>IO</sub> from 30% to 70% of V <sub>CCA</sub> /V <sub>CCB</sub>	0	10	nS/V	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# NL5X4002

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CCA} = 1.65\text{ V to }5.5\text{ V}$ ,  $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$ , unless otherwise specified)  
(Notes 4 and 5)

Symbol	Parameter	Test Conditions	-40 °C to +125 °C			Unit
			Min	Typ	Max	
$V_{IHA}$	$V_{CCA}$ Input HIGH Voltage		$V_{CCA} - 0.4$	-	-	V
$V_{ILA}$	$V_{CCA}$ Input LOW Voltage		-	-	0.15	V
$V_{IHB}$	$V_{CCB}$ Input HIGH Voltage		$V_{CCB} - 0.4$	-	-	V
$V_{ILB}$	$V_{CCB}$ Input LOW Voltage		-	-	0.15	V
$V_{IH}$	EN Pin Input HIGH Voltage		$0.65 * V_{CCA}$	-	-	V
$V_{IL}$	EN Pin Input LOW Voltage		-	-	$0.35 * V_{CCA}$	V
$V_{OHA}$	$V_{CCA}$ Output HIGH Voltage	A Port source current = -20 $\mu$ A	$2/3 * V_{CCA}$	-	-	V
$V_{OLA}$	$V_{CCA}$ Output LOW Voltage	A Port sink current = 1 mA	-	-	0.4	V
$V_{OHB}$	$V_{CCB}$ Output HIGH Voltage	B Port source current = -20 $\mu$ A	$2/3 * V_{CCB}$	-	-	V
$V_{OLB}$	$V_{CCB}$ Output LOW Voltage	B Port sink current = 1 mA	-	-	0.4	V
$I_{QVCCA}$	$V_{CCA}$ Supply Current	A and B unconnected, $V_{EN} = V_{CCA}$	-	0.5	5.0	$\mu$ A
		$V_{CCA} = 5.5\text{ V}$ , $V_{CCB} = 0\text{ V}$	-	-	-1.5	
		$V_{CCA} = 0\text{ V}$ , $V_{CCB} = 5.5\text{ V}$	-	-	1.5	
$I_{QVCCB}$	$V_{CCB}$ Supply Current	A and B unconnected, $V_{EN} = V_{CCA}$	-	0.5	5.0	$\mu$ A
		$V_{CCA} = 5.5\text{ V}$ , $V_{CCB} = 0\text{ V}$	-	-	1.5	
		$V_{CCA} = 0\text{ V}$ , $V_{CCB} = 5.5\text{ V}$	-	-	-1.5	
$I_{Z-VCCA}$	$V_{CCA}$ Tristate Output Mode Supply Current	A and B unconnected, $V_{EN} = \text{GND}$	-	0.1	5.0	$\mu$ A
$I_{Z-VCCB}$	$V_{CCB}$ Tristate Output Mode Supply Current	A and B unconnected, $V_{EN} = \text{GND}$	-	0.1	5.0	$\mu$ A
$I_I$	EN Pin Input Leakage Current		-	-	1.0	$\mu$ A
$I_{OFF}$	Power-Off Leakage Current	$V_{CCA} = 0\text{ V to }5.5\text{ V}$ ; $V_{CCB} = 0\text{ V}$ ; A = 0 V to 5.5 V	-	-	2.0	$\mu$ A
		$V_{CCA} = 0\text{ V}$ ; $V_{CCB} = 0\text{ to }5.5\text{ V}$ ; A = 0 to 5.5 V	-	-	2.0	
		$V_{CCA} = 0\text{ to }5.5\text{ V}$ ; $V_{CCB} = 0\text{ V}$ ; B = 0 to 5.5 V	-	-	2.0	
		$V_{CCA} = 0\text{ V}$ ; $V_{CCB} = 0\text{ to }5.5\text{ V}$ ; B = 0 to 5.5 V	-	-	2.0	
$I_{OZ}$	I/O Tristate Output Mode Leakage Current		-	0.1	2.0	$\mu$ A
$R_{PU}$	Pull-Up Resistors, A and B		-	10	-	k $\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Typical values are for  $V_{CCA} = +1.8\text{ V}$ ,  $V_{CCB} = +3.3\text{ V}$  and  $T_A = +25\text{ }^\circ\text{C}$ .

5. All units are production tested at  $T_A = +25\text{ }^\circ\text{C}$ . Limits over the operating temperature range are guaranteed by design.

# NL5X4002

## TIMING CHARACTERISTICS – RAIL-TO-RAIL DRIVING CONFIGURATION

(Test circuits of Figures 4, 5, 8, 9, 10 and 11,  $C_{LOAD} = 15$  pF, driver output impedance  $\leq 50 \Omega$ ,  $R_{LOAD} = 1$  M $\Omega$ , unless otherwise specified. (Notes 6, 7 and 8))

Symbol	Parameter	Conditions	-40 °C to +125 °C			Unit
			Min	Typ	Max	

**$V_{CCA} = 1.65$  V,  $V_{CCB} = 1.65$  V**

$t_{RB}$	B Port Rise Time			9	32	ns
$t_{FB}$	B Port Fall Time			11	20	ns
$t_{RA}$	A Port Rise Time			20	30	ns
$t_{FA}$	A Port Fall Time			10	13	ns
$t_{PDAB}$	Propagation Delay (A to B)			7	16	ns
$t_{PDBA}$	Propagation Delay (B to A)			12	15	ns
$t_{EN}$	Enable Time				125	ns
$t_{DIS}$	Disable Time				260	ns
$t_{SKEW}$	Skew				2	ns
MDR	Maximum Data Rate		15			Mbps

**$V_{CCA} = 1.65$  V,  $V_{CCB} = 5.5$  V**

$t_{RB}$	B Port Rise Time			9	12	ns
$t_{FB}$	B Port Fall Time			17	30	ns
$t_{RA}$	A Port Rise Time			2	4	ns
$t_{FA}$	A Port Fall Time			3	7	ns
$t_{PDAB}$	Propagation Delay (A to B)			14	24	ns
$t_{PDBA}$	Propagation Delay (B to A)			3	5	ns
$t_{EN}$	Enable Time				125	ns
$t_{DIS}$	Disable Time				260	ns
$t_{SKEW}$	Skew				2	ns
MDR	Maximum Data Rate		24			Mbps

**$V_{CCA} = 1.8$  V,  $V_{CCB} = 2.8$  V**

$t_{RB}$	B Port Rise Time			11	18	ns
$t_{FB}$	B Port Fall Time			10	15	ns
$t_{RA}$	A Port Rise Time			12	15	ns
$t_{FA}$	A Port Fall Time			5	8	ns
$t_{PDAB}$	Propagation Delay (A to B)			7	10	ns
$t_{PDBA}$	Propagation Delay (B to A)			5	9	ns
$t_{EN}$	Enable Time				125	ns
$t_{DIS}$	Disable Time				260	ns
$t_{SKEW}$	Skew				2	ns
MDR	Maximum Data Rate		24			Mbps

**$V_{CCA} = 2.5$  V,  $V_{CCB} = 3.6$  V**

$t_{RB}$	B Port Rise Time			8	12	ns
$t_{FB}$	B Port Fall Time			8	12	ns
$t_{RA}$	A Port Rise Time			7	10	ns
$t_{FA}$	A Port Fall Time			5	7	ns
$t_{PDAB}$	Propagation Delay (A to B)			7	10	ns

# NL5X4002

## TIMING CHARACTERISTICS – RAIL-TO-RAIL DRIVING CONFIGURATION (continued)

(Test circuits of Figures 4, 5, 8, 9, 10 and 11,  $C_{LOAD} = 15$  pF, driver output impedance  $\leq 50 \Omega$ ,  $R_{LOAD} = 1$  M $\Omega$ , unless otherwise specified. (Notes 6, 7 and 8))

Symbol	Parameter	Conditions	-40 °C to +125 °C			Unit
			Min	Typ	Max	

**V<sub>CCA</sub> = 2.5 V, V<sub>CCB</sub> = 3.6 V**

t <sub>PDBA</sub>	Propagation Delay (B to A)			5	8	ns
t <sub>EN</sub>	Enable Time				125	ns
t <sub>DIS</sub>	Disable Time				260	ns
t <sub>SKEW</sub>	Skew				2	ns
MDR	Maximum Data Rate		24			Mbps

**V<sub>CCA</sub> = 2.8 V, V<sub>CCB</sub> = 1.8 V**

t <sub>RB</sub>	B Port Rise Time			13	20	ns
t <sub>FB</sub>	B Port Fall Time			7	10	ns
t <sub>RA</sub>	A Port Rise Time			8	13	ns
t <sub>FA</sub>	A Port Fall Time			9	15	ns
t <sub>PDAB</sub>	Propagation Delay (A to B)			6	9	ns
t <sub>PDBA</sub>	Propagation Delay (B to A)			7	12	ns
t <sub>EN</sub>	Enable Time				125	ns
t <sub>DIS</sub>	Disable Time				260	ns
t <sub>SKEW</sub>	Skew				2	ns
MDR	Maximum Data Rate		24			Mbps

**V<sub>CCA</sub> = 3.6 V, V<sub>CCB</sub> = 2.5 V**

t <sub>RB</sub>	B Port Rise Time			9	12	ns
t <sub>FB</sub>	B Port Fall Time			6	9	ns
t <sub>RA</sub>	A Port Rise Time			6	12	ns
t <sub>FA</sub>	A Port Fall Time			7	12	ns
t <sub>PDAB</sub>	Propagation Delay (A to B)			5	7	ns
t <sub>PDBA</sub>	Propagation Delay (B to A)			6	9	ns
t <sub>EN</sub>	Enable Time				125	ns
t <sub>DIS</sub>	Disable Time				260	ns
t <sub>SKEW</sub>	Skew				2	ns
MDR	Maximum Data Rate		24			Mbps

**V<sub>CCA</sub> = 5.5 V, V<sub>CCB</sub> = 1.65 V**

t <sub>RB</sub>	B Port Rise Time			13	20	ns
t <sub>FB</sub>	B Port Fall Time			6	9	ns
t <sub>RA</sub>	A Port Rise Time			8	10	ns
t <sub>FA</sub>	A Port Fall Time			20	27	ns
t <sub>PDAB</sub>	Propagation Delay (A to B)			5	8	ns
t <sub>PDBA</sub>	Propagation Delay (B to A)			14	24	ns
t <sub>EN</sub>	Enable Time				125	ns
t <sub>DIS</sub>	Disable Time				260	ns
t <sub>SKEW</sub>	Skew				2	ns
MDR	Maximum Data Rate		24			Mbps

# NL5X4002

## TIMING CHARACTERISTICS – RAIL-TO-RAIL DRIVING CONFIGURATION (continued)

(Test circuits of Figures 4, 5, 8, 9, 10 and 11,  $C_{LOAD} = 15 \text{ pF}$ , driver output impedance  $\leq 50 \Omega$ ,  $R_{LOAD} = 1 \text{ M}\Omega$ , unless otherwise specified. (Notes 6, 7 and 8))

Symbol	Parameter	Conditions	-40 °C to +125 °C			Unit
			Min	Typ	Max	
<b><math>V_{CCA} = 5.5 \text{ V}</math>, <math>V_{CCB} = 5.5 \text{ V}</math></b>						
$t_{RB}$	B Port Rise Time			5	7	ns
$t_{FB}$	B Port Fall Time			6	8	ns
$t_{RA}$	A Port Rise Time			5	7	ns
$t_{FA}$	A Port Fall Time			4	7	ns
$t_{PDAB}$	Propagation Delay (A to B)			4	6	ns
$t_{PDBA}$	Propagation Delay (B to A)			4	6	ns
$t_{EN}$	Enable Time				125	ns
$t_{DIS}$	Disable Time				260	ns
$t_{SKEW}$	Skew				2	ns
MDR	Maximum Data Rate		24			Mbps

# NL5X4002

## TIMING CHARACTERISTICS – OPEN DRAIN DRIVING CONFIGURATION

(Test circuits of Figures 6, 7, 8, 9, 10 and 11,  $C_{LOAD} = 15$  pF, driver output impedance  $\leq 50 \Omega$ ,  $R_{LOAD} = 1$  M $\Omega$ , unless otherwise specified. (Notes 6, 7 and 8))

Symbol	Parameter	Conditions	-40 °C to +125 °C			Unit
			Min	Typ	Max	

**$V_{CCA} = 1.65$  V,  $V_{CCB} = 5.5$  V**

$t_{RB}$	B Port Rise Time			8	40	ns
$t_{FB}$	B Port Fall Time			20	30	ns
$t_{RA}$	A Port Rise Time			80	110	ns
$t_{FA}$	A Port Fall Time			3	7	ns
$t_{PDAB}$	Propagation Delay (A to B)			27	45	ns
$t_{PDBA}$	Propagation Delay (B to A)			9	17	ns
$t_{EN}$	Enable Time				125	ns
$t_{DIS}$	Disable Time				260	ns
$t_{SKEW}$	Skew			2		ns
MDR	Maximum Data Rate		4			Mbps

**$V_{CCA} = 1.8$  V,  $V_{CCB} = 3.3$  V**

$t_{RB}$	B Port Rise Time			34	60	ns
$t_{FB}$	B Port Fall Time			8	15	ns
$t_{RA}$	A Port Rise Time			100	110	ns
$t_{FA}$	A Port Fall Time			5	8	ns
$t_{PDAB}$	Propagation Delay (A to B)			33	40	ns
$t_{PDBA}$	Propagation Delay (B to A)			6	11	ns
$t_{EN}$	Enable Time				125	ns
$t_{DIS}$	Disable Time				260	ns
$t_{SKEW}$	Skew			2		ns
MDR	Maximum Data Rate		4			Mbps

**$V_{CCA} = 5.5$  V,  $V_{CCB} = 1.65$  V**

$t_{RB}$	B Port Rise Time			80	110	ns
$t_{FB}$	B Port Fall Time			6	9	ns
$t_{RA}$	A Port Rise Time			7	40	ns
$t_{FA}$	A Port Fall Time			17	27	ns
$t_{PDAB}$	Propagation Delay (A to B)			10	17	ns
$t_{PDBA}$	Propagation Delay (B to A)			27	45	ns
$t_{EN}$	Enable Time				125	ns
$t_{DIS}$	Disable Time				260	ns
$t_{SKEW}$	Skew			2		ns
MDR	Maximum Data Rate		4			Mbps

**$V_{CCA} = 5.5$  V,  $V_{CCB} = 5.5$  V**

$t_{RB}$	B Port Rise Time			61	70	ns
$t_{FB}$	B Port Fall Time			6	8	ns
$t_{RA}$	A Port Rise Time			61	70	ns
$t_{FA}$	A Port Fall Time			4	7	ns
$t_{PDAB}$	Propagation Delay (A to B)			4	6	ns

# NL5X4002

## TIMING CHARACTERISTICS – OPEN DRAIN DRIVING CONFIGURATION (continued)

(Test circuits of Figures 6, 7, 8, 9, 10 and 11,  $C_{LOAD} = 15 \text{ pF}$ , driver output impedance  $\leq 50 \Omega$ ,  $R_{LOAD} = 1 \text{ M}\Omega$ , unless otherwise specified. (Notes 6, 7 and 8))

Symbol	Parameter	Conditions	-40 °C to +125 °C			Unit
			Min	Typ	Max	
<b><math>V_{CCA} = 5.5 \text{ V}</math>, <math>V_{CCB} = 5.5 \text{ V}</math></b>						
$t_{PDBA}$	Propagation Delay (B to A)			6	9	ns
$t_{EN}$	Enable Time				125	ns
$t_{DIS}$	Disable Time				260	ns
$t_{SKEW}$	Skew			2		ns
MDR	Maximum Data Rate		5			Mbps

6. Typical values are for  $V_{CCA}$  and  $V_{CCB}$  at  $T_A = +25 \text{ }^\circ\text{C}$ .

7. Limits over the operating temperature range are guaranteed by design.

8. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (A or B) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW). Skew is defined by applying a single input to the two input channels and measuring the difference in propagation delays between the output channels.

TEST SETUPS AND TIMING MEASUREMENTS

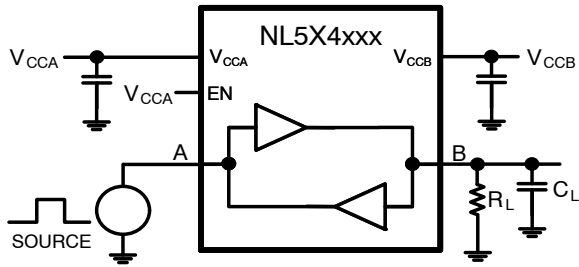


Figure 4. Rail-to-Rail Driving, A to B

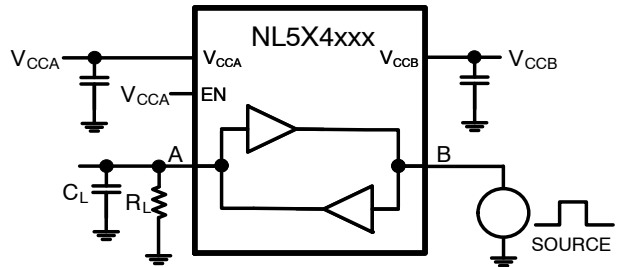


Figure 5. Rail-to-Rail Driving, B to A

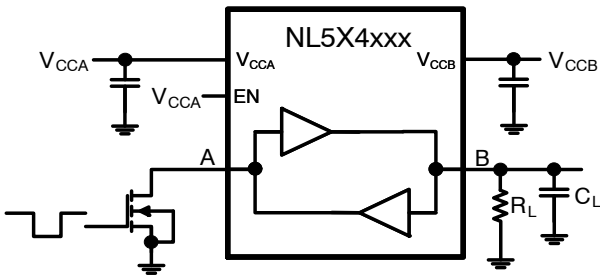


Figure 6. Open-Drain Driving, A to B

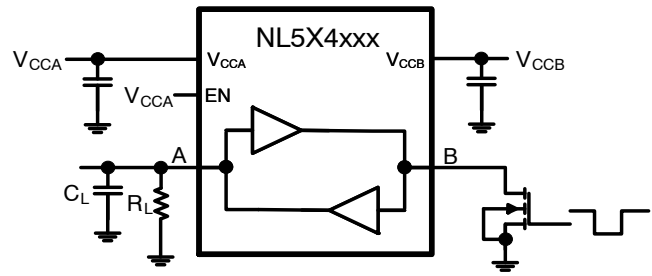


Figure 7. Open-Drain Driving, B to A

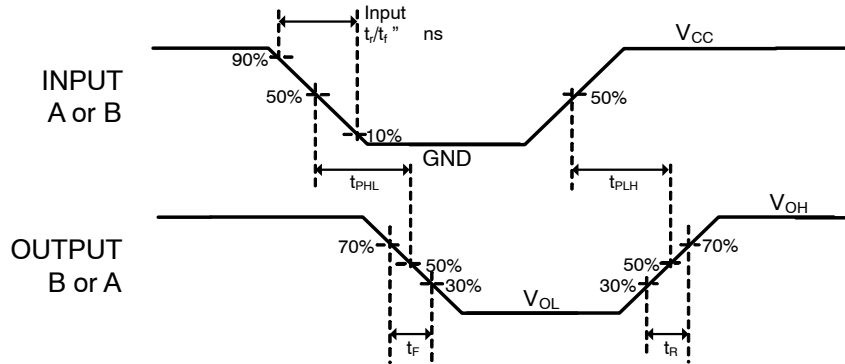


Figure 8.  $t_{PD}$  ( $t_{PHL}$ ,  $t_{PLH}$ ) and Output  $t_R$  /  $t_F$  Timing

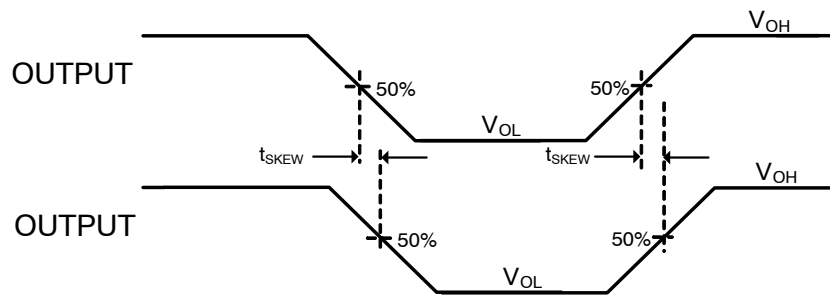


Figure 9.  $t_{SKEW}$  Timing

## NL5X4002

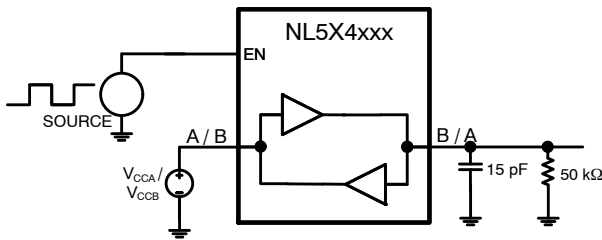


Figure 10.  $t_{EN}/t_{DIS}$  Setup for  $t_{PZH}$ ,  $t_{PHZ}$

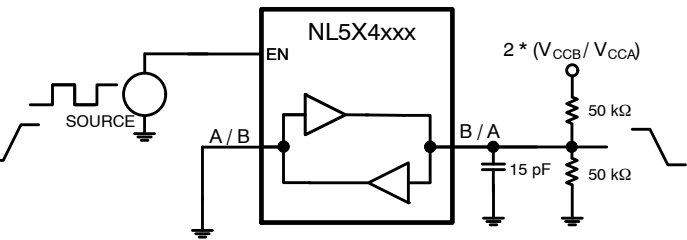


Figure 11.  $t_{EN}/t_{DIS}$  Setup for  $t_{PLZ}$ ,  $t_{PLZ}$

## APPLICATIONS INFORMATION

### Level Translator Architecture

The NL5X4002 auto sense translator provides bi-directional voltage level shifting to transfer data in multiple supply voltage systems. These devices have two supply voltages,  $V_{CCA}$  and  $V_{CCB}$ , which set the logic levels on the input and output sides of the translator. When used to transfer data from the A to the B ports, input signals referenced to the  $V_{CCA}$  supply are translated to output signals with a logic level matched to  $V_{CCB}$ . In a similar manner, the B to A translation shifts input signals with a logic level compatible to  $V_{CCB}$  to an output signal matched to  $V_{CCA}$ .

These devices consist of two bi-directional channels that independently determine the direction of the data flow without requiring a directional pin. The one-shot circuits detect rising input signals and then decrease the rise times of the output signal for low-to-high transitions.

Each input/output channel of the NL5X4002 translator has an internal 10 k $\Omega$  pull-up resistor. The magnitude of the pullup resistors can be reduced by connecting external resistors in parallel with the internal 10 k $\Omega$  resistors.

### Output Performance

The rise ( $t_R$ ) and fall ( $t_F$ ) timing parameters of the open drain outputs depend on the magnitude of the pull-up resistors. In addition, the propagation times ( $t_{PD}$ ), skew

( $t_{SKEW}$ ) and maximum data rate depend on the impedance of the device that is connected to the translator.

### Enable Input

These devices have Enable pins (EN) that provide tri-state operation at the I/O pins. Driving the EN pin to a low logic level minimizes the power consumption of the device and drives the A and B ports to high impedance states. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the  $V_{CCA}$  supply and has Overvoltage Tolerant (OVT) protection.

### Power Supply Guidelines

During normal operation, supply voltage  $V_{CCA}$  can be greater than, less than or equal to  $V_{CCB}$ . The sequencing of the power supplies will not damage the device during the power up operation.

For optimal performance, 0.01  $\mu$ F to 0.1  $\mu$ F decoupling capacitors should be used on the  $V_{CCA}$  and  $V_{CCB}$  power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

# NL5X4002

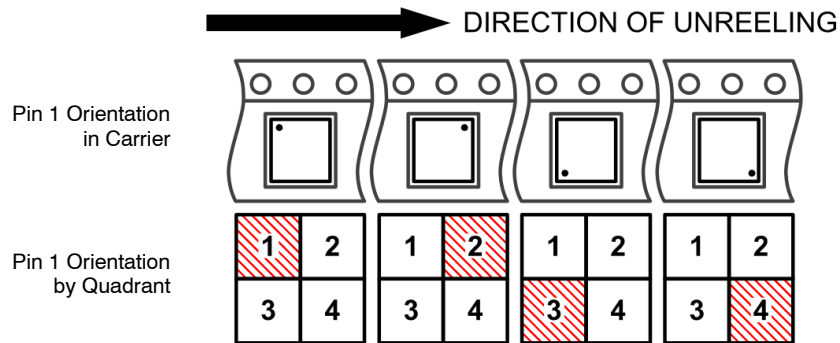
## DEVICE ORDERING INFORMATION

Device Order Number	Device Marking	Package Type	Pin 1 Quadrant	Tape & Reel Size <sup>†</sup>
NL5X4002DR2G	5X4002	SO-8	1	2500 / Tape & Reel
NL5X4002DR2G-Q*	5X4002	SO-8	1	2500 / Tape & Reel
NL5X4002DMR2G	4002	Micro8	1	4000 / Tape & Reel
NL5X4002MUTAG	AF	UDFN-8, 1.8x.1.2	1	3000 / Tape & Reel
NL5X4002MUTAG-Q*	AF	UDFN-8, 1.8x.1.2	1	3000 / Tape & Reel

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

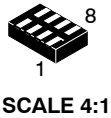
\* -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

### Pin 1 Orientation in Tape and Reel



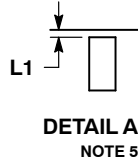
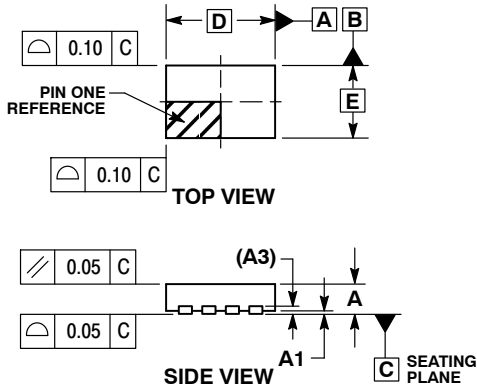
## REVISION HISTORY

Revision	Description of Changes	Date
0	Initial release.	06/24/2025
1	Added AEC-Q100 Qualified note under ordering table.	07/25/2025
2	Revision to remove one package order option and three OPNs	02/02/2026



**UDFN8 1.8x1.2, 0.4P**  
CASE 517AJ  
ISSUE O

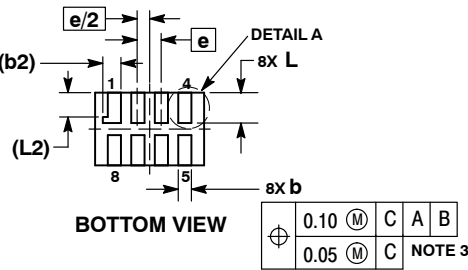
DATE 08 NOV 2006



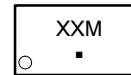
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127	REF
b	0.15	0.25
b2	0.30	REF
D	1.80	BSC
E	1.20	BSC
e	0.40	BSC
L	0.45	0.55
L1	0.00	0.03
L2	0.40	REF

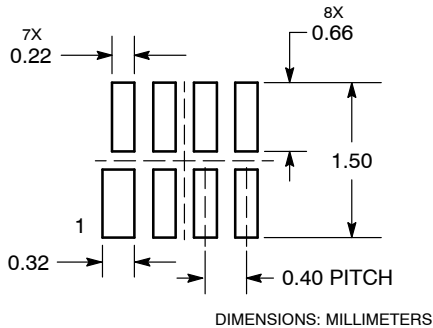


**GENERIC MARKING DIAGRAM\***



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

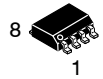
**MOUNTING FOOTPRINT SOLDERMASK DEFINED**



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

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<b>DESCRIPTION:</b>	<b>UDFN8 1.8X1.2, 0.4P</b>	<b>PAGE 1 OF 1</b>

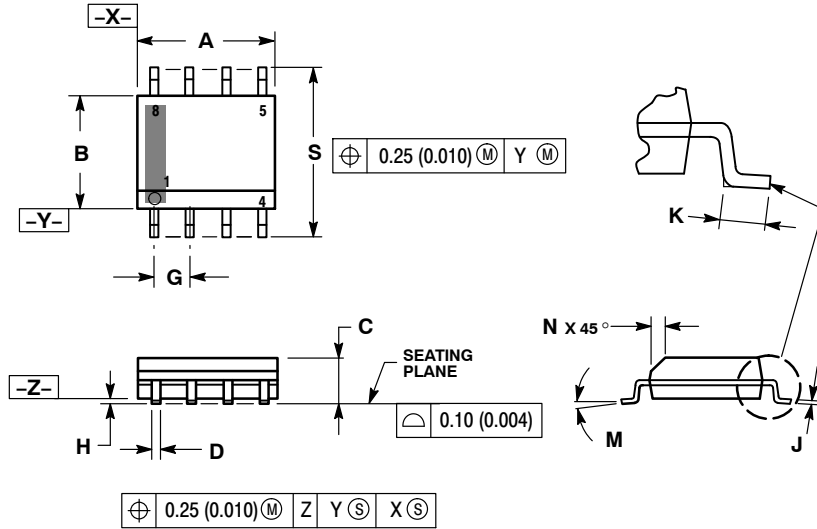
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SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/> PIN 1. EMITTER<br/> 2. COLLECTOR<br/> 3. COLLECTOR<br/> 4. EMITTER<br/> 5. EMITTER<br/> 6. BASE<br/> 7. BASE<br/> 8. EMITTER</p>   | <p>STYLE 2:<br/> PIN 1. COLLECTOR, DIE, #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. BASE, #2<br/> 6. EMITTER, #2<br/> 7. BASE, #1<br/> 8. EMITTER, #1</p>               | <p>STYLE 3:<br/> PIN 1. DRAIN, DIE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. GATE, #2<br/> 6. SOURCE, #2<br/> 7. GATE, #1<br/> 8. SOURCE, #1</p>                            | <p>STYLE 4:<br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. ANODE<br/> 4. ANODE<br/> 5. ANODE<br/> 6. ANODE<br/> 7. ANODE<br/> 8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/> PIN 1. DRAIN<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. DRAIN<br/> 5. GATE<br/> 6. GATE<br/> 7. SOURCE<br/> 8. SOURCE</p>   | <p>STYLE 6:<br/> PIN 1. SOURCE<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. SOURCE<br/> 5. SOURCE<br/> 6. GATE<br/> 7. GATE<br/> 8. SOURCE</p>  | <p>STYLE 7:<br/> PIN 1. INPUT<br/> 2. EXTERNAL BYPASS<br/> 3. THIRD STAGE SOURCE<br/> 4. GROUND<br/> 5. DRAIN<br/> 6. GATE 3<br/> 7. SECOND STAGE Vd<br/> 8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/> PIN 1. COLLECTOR, DIE #1<br/> 2. BASE, #1<br/> 3. BASE, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #2<br/> 6. EMITTER, #2<br/> 7. EMITTER, #1<br/> 8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/> PIN 1. EMITTER, COMMON<br/> 2. COLLECTOR, DIE #1<br/> 3. COLLECTOR, DIE #2<br/> 4. EMITTER, COMMON<br/> 5. EMITTER, COMMON<br/> 6. BASE, DIE #2<br/> 7. BASE, DIE #1<br/> 8. EMITTER, COMMON</p> | <p>STYLE 10:<br/> PIN 1. GROUND<br/> 2. BIAS 1<br/> 3. OUTPUT<br/> 4. GROUND<br/> 5. GROUND<br/> 6. BIAS 2<br/> 7. INPUT<br/> 8. GROUND</p>  | <p>STYLE 11:<br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. DRAIN 2<br/> 7. DRAIN 1<br/> 8. DRAIN 1</p>   | <p>STYLE 12:<br/> PIN 1. SOURCE<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p>STYLE 13:<br/> PIN 1. N.C.<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>  | <p>STYLE 14:<br/> PIN 1. N-SOURCE<br/> 2. N-GATE<br/> 3. P-SOURCE<br/> 4. P-GATE<br/> 5. P-DRAIN<br/> 6. P-DRAIN<br/> 7. N-DRAIN<br/> 8. N-DRAIN</p>   | <p>STYLE 15:<br/> PIN 1. ANODE 1<br/> 2. ANODE 1<br/> 3. ANODE 1<br/> 4. ANODE 1<br/> 5. CATHODE, COMMON<br/> 6. CATHODE, COMMON<br/> 7. CATHODE, COMMON<br/> 8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/> PIN 1. EMITTER, DIE #1<br/> 2. BASE, DIE #1<br/> 3. EMITTER, DIE #2<br/> 4. BASE, DIE #2<br/> 5. COLLECTOR, DIE #2<br/> 6. COLLECTOR, DIE #2<br/> 7. COLLECTOR, DIE #1<br/> 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/> PIN 1. VCC<br/> 2. V2OUT<br/> 3. V1OUT<br/> 4. TXE<br/> 5. RXE<br/> 6. VEE<br/> 7. GND<br/> 8. ACC</p>  | <p>STYLE 18:<br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. CATHODE<br/> 8. CATHODE</p>   | <p>STYLE 19:<br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. MIRROR 2<br/> 7. DRAIN 1<br/> 8. MIRROR 1</p>   | <p>STYLE 20:<br/> PIN 1. SOURCE (N)<br/> 2. GATE (N)<br/> 3. SOURCE (P)<br/> 4. GATE (P)<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p>STYLE 21:<br/> PIN 1. CATHODE 1<br/> 2. CATHODE 2<br/> 3. CATHODE 3<br/> 4. CATHODE 4<br/> 5. CATHODE 5<br/> 6. COMMON ANODE<br/> 7. COMMON ANODE<br/> 8. CATHODE 6</p>  | <p>STYLE 22:<br/> PIN 1. I/O LINE 1<br/> 2. COMMON CATHODE/VCC<br/> 3. COMMON CATHODE/VCC<br/> 4. I/O LINE 3<br/> 5. COMMON ANODE/GND<br/> 6. I/O LINE 4<br/> 7. I/O LINE 5<br/> 8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/> PIN 1. LINE 1 IN<br/> 2. COMMON ANODE/GND<br/> 3. COMMON ANODE/GND<br/> 4. LINE 2 IN<br/> 5. LINE 2 OUT<br/> 6. COMMON ANODE/GND<br/> 7. COMMON ANODE/GND<br/> 8. LINE 1 OUT</p> | <p>STYLE 24:<br/> PIN 1. BASE<br/> 2. EMITTER<br/> 3. COLLECTOR/ANODE<br/> 4. COLLECTOR/ANODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. COLLECTOR/ANODE<br/> 8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/> PIN 1. VIN<br/> 2. N/C<br/> 3. REXT<br/> 4. GND<br/> 5. IOUT<br/> 6. IOUT<br/> 7. IOUT<br/> 8. IOUT</p>   | <p>STYLE 26:<br/> PIN 1. GND<br/> 2. dv/dt<br/> 3. ENABLE<br/> 4. ILIMIT<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. VCC</p>  | <p>STYLE 27:<br/> PIN 1. ILIMIT<br/> 2. OVLO<br/> 3. UVLO<br/> 4. INPUT+<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. DRAIN</p>  | <p>STYLE 28:<br/> PIN 1. SW_TO_GND<br/> 2. DASIC OFF<br/> 3. DASIC_SW_DET<br/> 4. GND<br/> 5. V_MON<br/> 6. VBULK<br/> 7. VBULK<br/> 8. VIN</p>  |
| <p>STYLE 29:<br/> PIN 1. BASE, DIE #1<br/> 2. EMITTER, #1<br/> 3. BASE, #2<br/> 4. EMITTER, #2<br/> 5. COLLECTOR, #2<br/> 6. COLLECTOR, #2<br/> 7. COLLECTOR, #1<br/> 8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/> PIN 1. DRAIN 1<br/> 2. DRAIN 1<br/> 3. GATE 2<br/> 4. SOURCE 2<br/> 5. SOURCE 1/DRAIN 2<br/> 6. SOURCE 1/DRAIN 2<br/> 7. SOURCE 1/DRAIN 2<br/> 8. GATE 1</p>                           |  |  |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42564B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-8 NB</b>	<b>PAGE 2 OF 2</b>

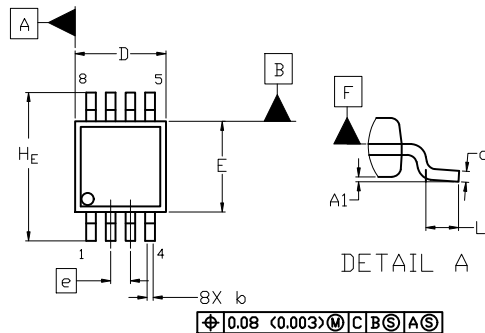
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SCALE 2:1

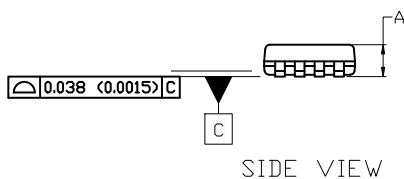
**Micro8  
CASE 846A-02  
ISSUE K**

DATE 16 JUL 2020

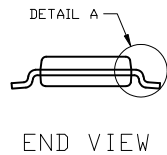


TOP VIEW

NOTE 3



SIDE VIEW



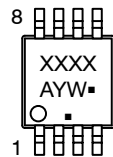
END VIEW

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

$\phi 0.08$  (0.003) M C B S A S

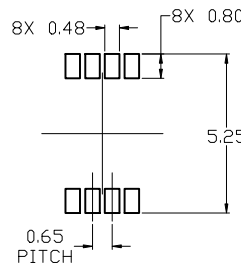
**GENERIC MARKING DIAGRAM\***



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



**RECOMMENDED MOUNTING FOOTPRINT**

For additional information on our Pb-Free strategy and soldering details, please download the [DN Semiconductor Soldering and Mounting Techniques Reference Manual, SLDERRM/D](#).

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
HE	4.75	4.90	5.05
L	0.40	0.55	0.70

**STYLE 1:**

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

**STYLE 2:**

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

**STYLE 3:**

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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