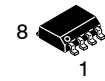


Self Protected High Side Driver with Temperature Shutdown and Current Limit

NCV8461



SOIC-8
 CASE 751
 STYLE 11

The NCV8461 is a fully protected High-Side driver that can be used to switch a wide variety of loads, such as bulbs, solenoids and other activators. The device is internally protected from an overload condition by an active current limit and thermal shutdown. A diagnostic output reports OFF state open load conditions as well as thermal shutdown.

Features

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- CMOS (3 V / 5 V) Compatible Control Input
- Off State Open Load Detection
- Open Drain Diagnostic Output
- Overvoltage Protection
- Undervoltage Shutdown
- Loss of Ground and Loss of V_D Protection
- ESD Protection
- Reverse Battery Protection (with external resistor)
- Very Low Standby Current
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This is a Pb-Free Device

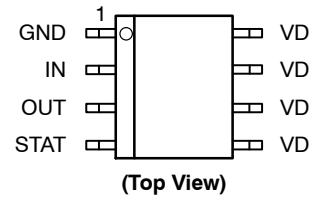
Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

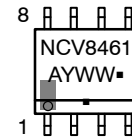
FEATURE SUMMARY

Overvoltage Protection	V_{OV}	41	V
R_{DSon} (max) $T_J = 25\text{ }^\circ\text{C}$	R_{ON}	350	m Ω
Output Current Limit (typ)	I_{lim}	1.2	A
Operating Voltage Range	V_{OP}	5 – 34	V

PIN CONNECTIONS



MARKING DIAGRAM



NCV8461 = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NCV8461DR2G	SOIC-8 (Pb-Free)	2,500 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

NCV8461

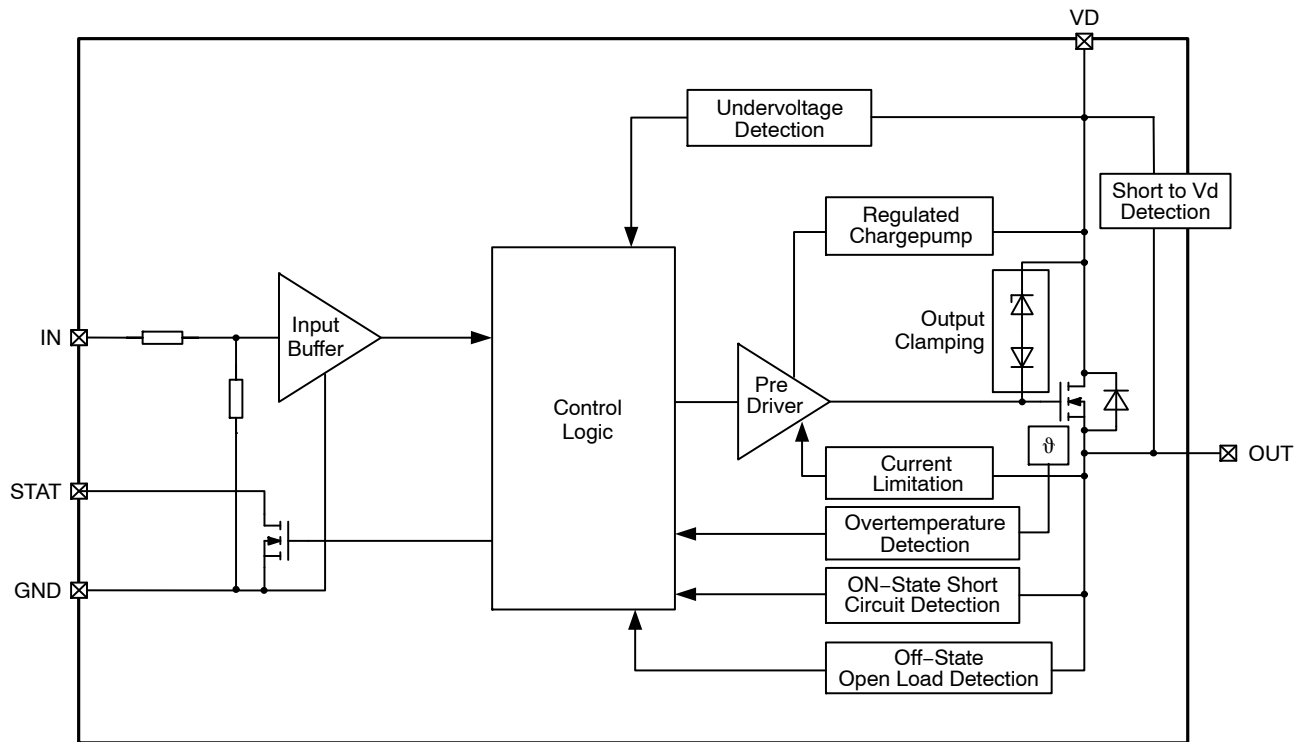


Figure 1. Block Diagram

SO8 PACKAGE PIN DESCRIPTION

Pin #	Symbol	Description
1	GND	Ground
2	IN	Logic Level Input
3	OUT	Output
4	STAT	Status Output
5	V _D	Supply Voltage
6	V _D	Supply Voltage
7	V _D	Supply Voltage
8	V _D	Supply Voltage

Table 1. MAXIMUM RATINGS

Symbol	Rating	Value		Unit
		Min	Max	
V _D	DC Supply Voltage (Note 1)	-16	40	V
V _{peak}	Peak Transient Input Voltage (Note 1) (Load Dump 38 V, V _D = 14 V, ISO7637-2 pulse5)		52	V
V _{in}	Input Voltage	-10	16	V
I _{in}	Input Current	-5	5	mA
I _{out}	Output Current (Note 1)	-	Internally Limited	A
I _{status}	Status Current	-5	5	mA
P _{tot}	Power Dissipation T _c = 25 °C (Note 1)	1.5		W
	Electrostatic Discharge (Note 1) (HBM Model 100 pF / 1500 Ω) Input All Other Pins	±1.5 ±5		DC kV kV
E _{AS}	Single Pulse Inductive Load Switching Energy (Note 1) V _D = 13.5 V; I _L = 0.5 A, T _{Jstart} = 150 °C	-	300	mJ
T _J	Operating Junction Temperature	-40	+150	°C
T _{storage}	Storage Temperature	-55	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Not subjected to production testing

Table 2. THERMAL RESISTANCE RATINGS

Symbol	Parameter	Max. Value	Units
R _{thJS}	Thermal Resistance (Note 2) Junction-to-Soldering Point	31	°C/W
R _{thJA}	Junction-to-Ambient (6 cm square pad size, FR-4, 2 oz Cu)	84	

2. Reverse Output current has to be limited by the load to stay within absolute maximum ratings and thermal performance. See spec table and page 6 for further reverse battery information.

NCV8461

Table 3. ELECTRICAL CHARACTERISTICS ($V_D = 13.5\text{ V}$; $-40\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$ unless otherwise specified)

Symbol	Rating	Conditions	Value			Unit
			Min	Typ	Max	
V_D	Operating Supply Voltage		5	–	34	V
V_{UV}	Undervoltage Shutdown				5	V
V_{UV_Res}	Undervoltage Restart				5.5	V
V_{OV}	Overvoltage Protection	$I_D = 4\text{ mA}$	41			V
R_{ON}	On Resistance	$I_{out} = 0.3\text{ A}$; $6\text{ V} < V_D < 40\text{ V}$, $T_J = 25\text{ }^\circ\text{C}$ $I_{out} = 0.3\text{ A}$; $6\text{ V} < V_D < 40\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$		250 450	350 700	m Ω
I_D	Standby Current	Off State; $V_{in} = V_{out} = 0\text{ V}$ On State; $V_{in} = 5\text{ V}$, $I_{out} = 0\text{ A}$		13 1	35 1.7	μA mA
$I_{L(off)}$	Output Leakage Current				12	μA

INPUT CHARACTERISTICS

V_{in_low}	Input Voltage - Low				0.8	V
V_{in_high}	Input Voltage - High		2.2			V
V_{hyst}	Input Hysteresis Voltage			0.3		V
I_{in_OFF}	Off State Input Current	$V_{in} = 0.7\text{ V}$	1		10	μA
I_{in_ON}	On State Input Current	$V_{in} = 5.0\text{ V}$	1		10	μA
R_I	Input Resistance (Note 3)		1.5	3.5		K Ω
V_{in_cl}	Input Clamp Voltage	$I_{in} = 1\text{ mA}$ $I_{in} = -1\text{ mA}$	14 -18	16 -16	18 -14	V

SWITCHING CHARACTERISTICS

t_{d_on}	Turn-On Delay Time	to 90% V_{out} , $R_L = 47\text{ }^\circ\Omega$			140	μs
t_{d_off}	Turn-Off Delay Time	to 10% V_{out} , $R_L = 47\text{ }^\circ\Omega$			170	μs
dV_{out}/dt_{on}	Slew Rate On	10% to 30% V_{out} , $R_L = 47\text{ }^\circ\Omega$			2	V / μs
dV_{out}/dt_{off}	Slew Rate Off	70% to 40% V_{out} , $R_L = 47\text{ }^\circ\Omega$			2	V / μs

REVERSE BATTERY (Note 3)

$-V_D$	Reverse Battery	Requires a 150 Ω Resistor in GND Connection			32	V
V_F	Forward Voltage	$T_J = 150\text{ }^\circ\text{C}$, $I_S = 200\text{ mA}$		0.6		V

STATUS PIN CHARACTERISTICS

V_{stat_low}	Status Output Voltage Low	$I_{stat} = 1.6\text{ mA}$, $T_J = -40\text{ }^\circ\text{C}$ to $25\text{ }^\circ\text{C}$ $I_{stat} = 1.6\text{ mA}$, $T_J = 150\text{ }^\circ\text{C}$ (Note 3)			0.4 0.6	V
$I_{stat_leakage}$	Status Leakage Current	$V_{stat} = 5\text{ V}$			10	μA
$T_d(\text{STAT})$	Status Invalid Time After Positive Input Slope			300	700	μs
V_{stat_cl}	Status Clamp Voltage	$I_{stat} = 1\text{ mA}$ $I_{stat} = -1\text{ mA}$		10 -1.4		V

PROTECTION FUNCTIONS (Note 4)

T_{SD}	Temperature Shutdown (Note 3)		150	175	200	$^\circ\text{C}$
T_{SD_hyst}	Temperature Shutdown Hysteresis (Note 3)			10		$^\circ\text{C}$
I_{lim}	Output Current Limit Initial Peak	$T_J = -40\text{ }^\circ\text{C}$, $V_D = 20\text{ V}$ (Note 3) $T_J = 25\text{ }^\circ\text{C}$ $T_J = 150\text{ }^\circ\text{C}$ (Note 3)	0.7	1.2	2	A
$I_{lim(SC)}$	Repetitive Short Circuit Current Limit	$T_J = T_{Jt}$ (Note 3)		1		A

NCV8461

Table 3. ELECTRICAL CHARACTERISTICS ($V_D = 13.5\text{ V}$; $-40\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$ unless otherwise specified)

Symbol	Rating	Conditions	Value			Unit
			Min	Typ	Max	

PROTECTION FUNCTIONS (Note 4)

V_{clamp}	Switch Off Output Clamp Voltage	$I_D = 4\text{ mA}$, $V_{\text{in}} = 0\text{ V}$	$V_D - 41$	$V_D - 47$		V
--------------------	---------------------------------	--	------------	------------	--	---

DIAGNOSTICS CHARACTERISTICS

$V_{\text{OUT(SC)}}$	Short Circuit Detection Voltage			2.8		V
V_{OL}	Openload Off State Detection Threshold	$V_{\text{in}} = 0\text{ V}$	1.5		3.5	V
$I_{\text{L(OL)}}$	Openload Detection Current			5		μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Not subjected to production testing

4. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper hardware/software strategy. If the devices operates under abnormal conditions this hardware/software solutions must limit the duration and number of activation cycles. AEC Q100-12 results available upon request.

Table 4. STATUS PIN TRUTH TABLE

Conditions	Input	Output	Status
Normal Operation	L	L	H
	H	H	H
Short Circuit to GND	L	L	H
	H	L*	L
Short to V_D (OFF State)	L	H	L
	H	H	H
Current Limitation	L	L	H
	H	H**	H
Overtemperature	L	L	H
	H	L	L
OFF State Open Load	L	H	L
	H	H	H

* Output = "L"; $V_{\text{OUT}} < 2\text{ V}$ typ.

* * Output = "H"; $V_{\text{OUT}} > 2\text{ V}$ typ.

NCV8461

REVERSE BATTERY PROTECTION

The NCV8461 provides reverse battery protection up to 32 V. This protection requires a Resistor in the GND path. The recommended GND resistor is 150 Ω , but a variety of resistor values can be chosen for this purpose. The graph below shows the considerations and constraints for selection of the GND resistor. Figure 2 shows the power dissipation in the GND resistor during a 32 V reverse battery event on the left axis, while the right axis shows the voltage drop

across the GND resistor while in normal operation. The far right side of the graph is grayed out to indicate that the voltage drop across the resistor is too high, and the part will not be able to turn on with a standard 5 V on the input pin. Selection of the optimal GND resistor requires balancing the power dissipation considerations while in a reverse battery event, with the turn on capability of the input signal during normal operation.

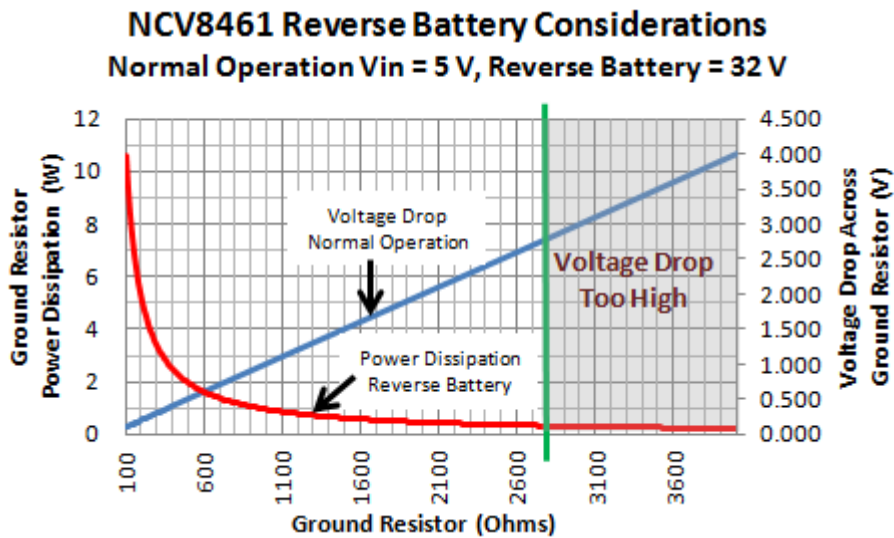


Figure 2. Reverse Battery Considerations

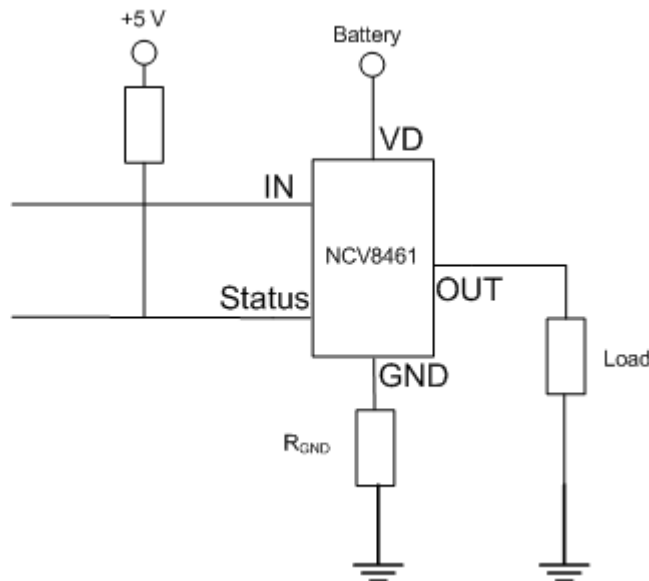


Figure 3. Reverse Battery Protection Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

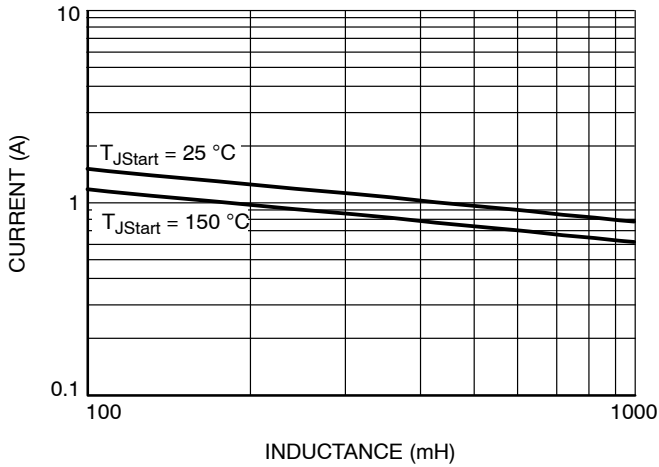


Figure 4. Maximum Single Pulse Switch Off Current vs. Inductance

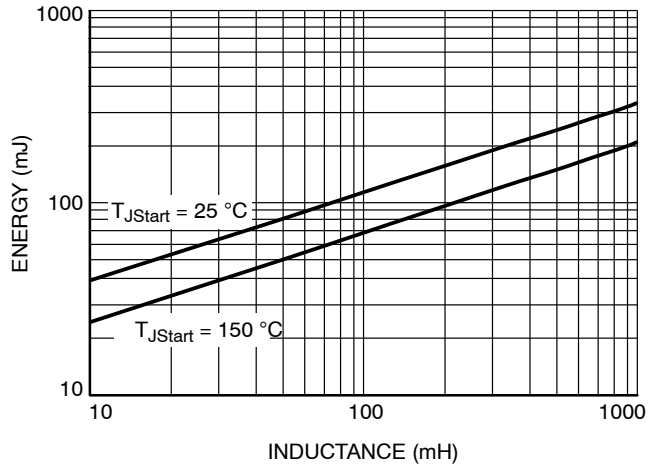


Figure 5. Maximum Single Pulse Switch Off Energy vs. Inductance

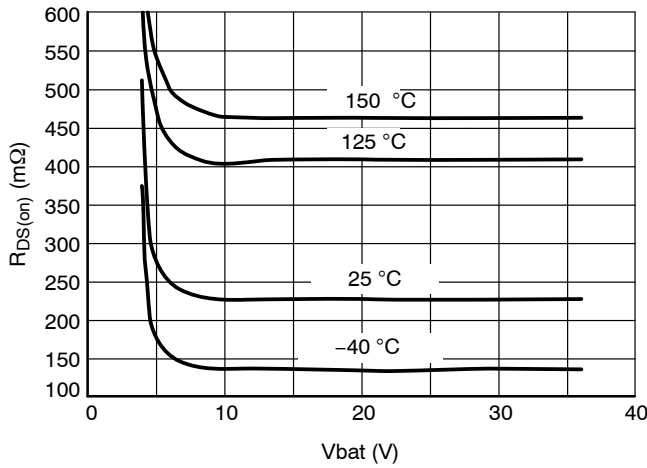


Figure 6. $R_{DS(on)}$ Over Temp and Battery

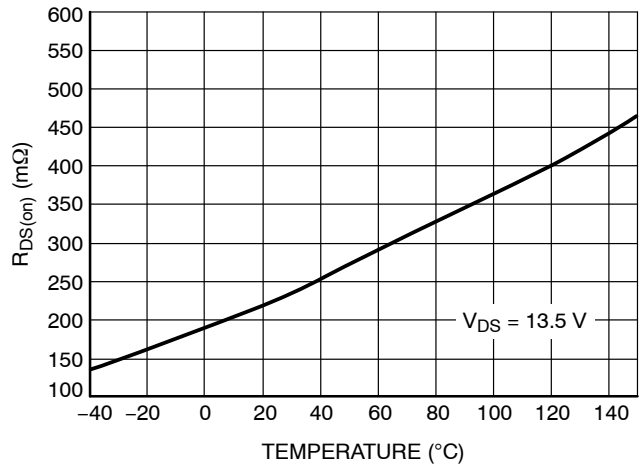


Figure 7. $R_{DS(on)}$ vs. Temperature

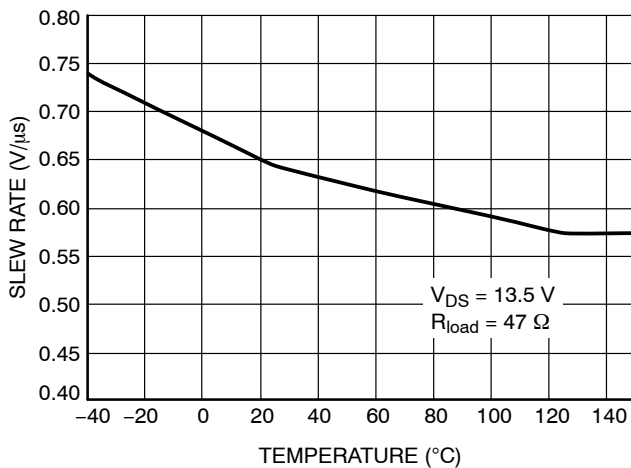


Figure 8. Slew Rate On vs. Temperature

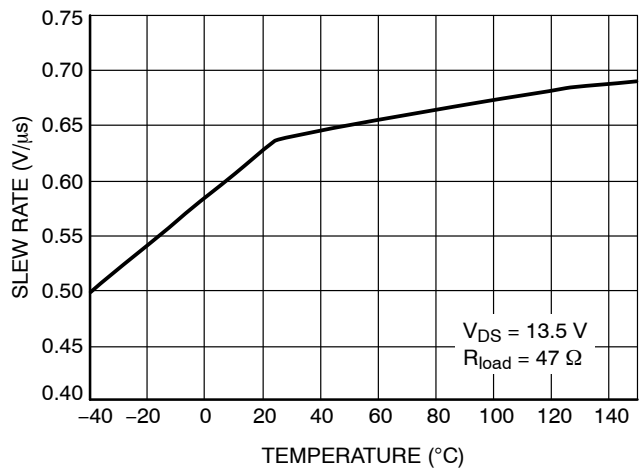


Figure 9. Slew Rate Off vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

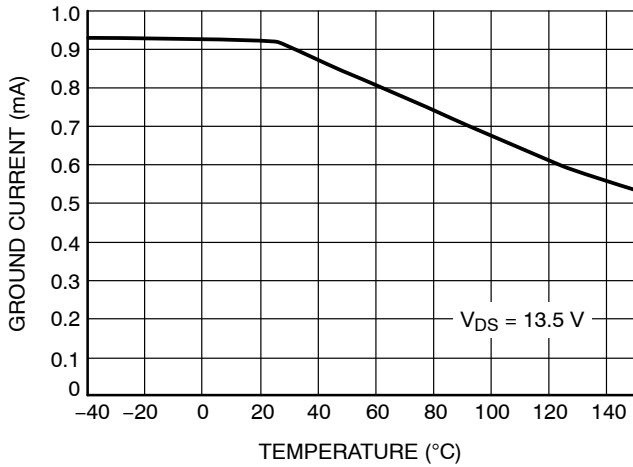


Figure 10. On State Ground Current vs. Temp

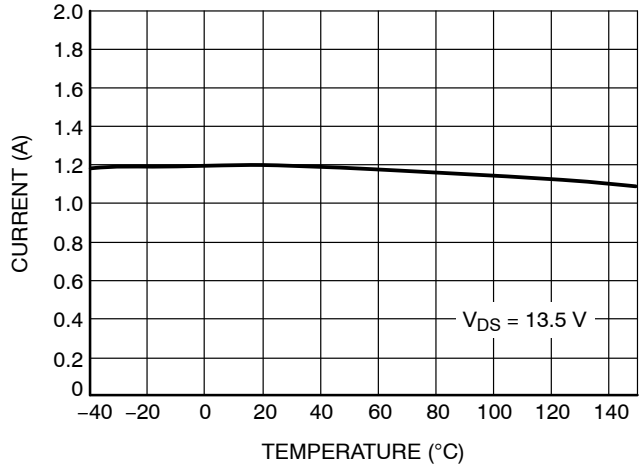


Figure 11. Current Limit vs. Temperature

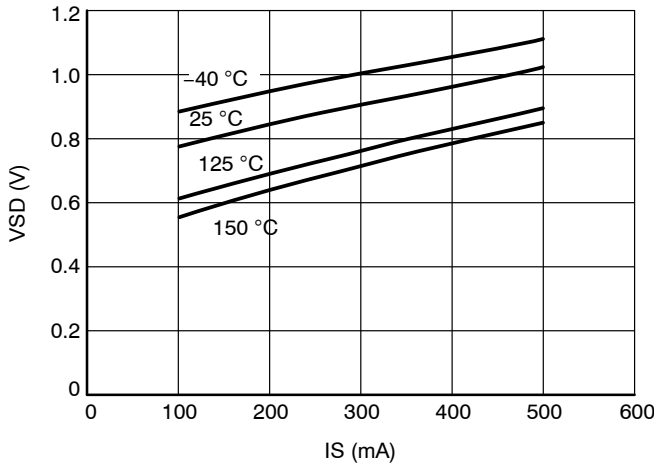


Figure 12. Body Diode

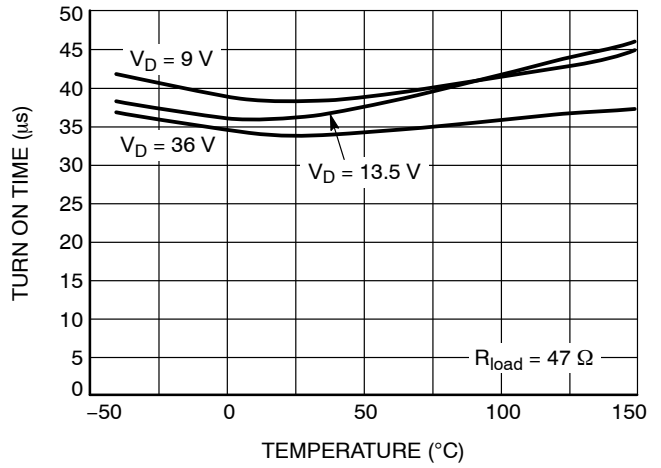


Figure 13. Turn On Time vs. Temperature

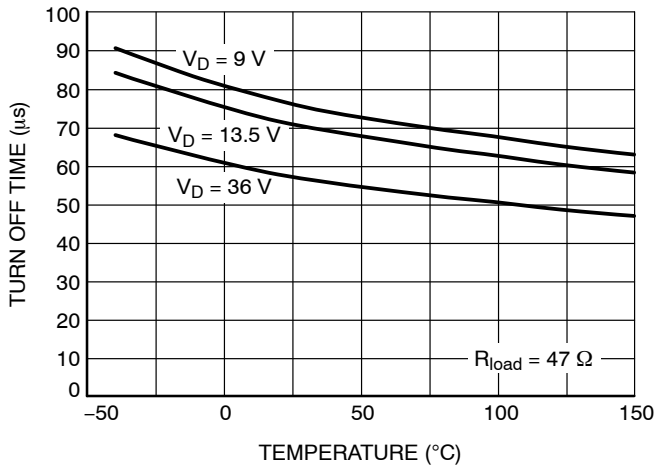


Figure 14. Turn Off Time vs. Temperature

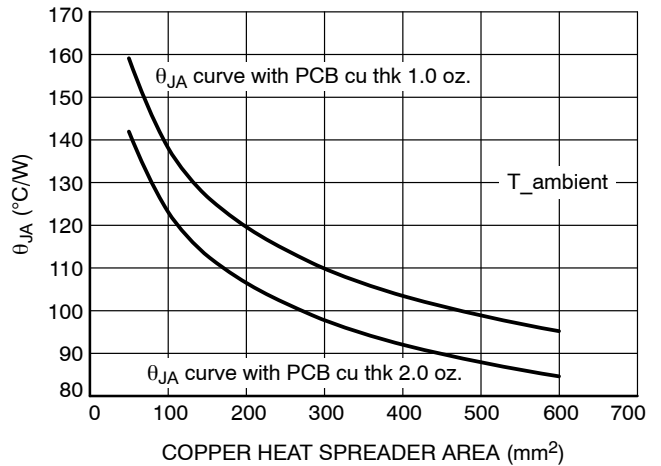


Figure 15. Junction-to-Ambient Thermal Resistance vs. Copper Area

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

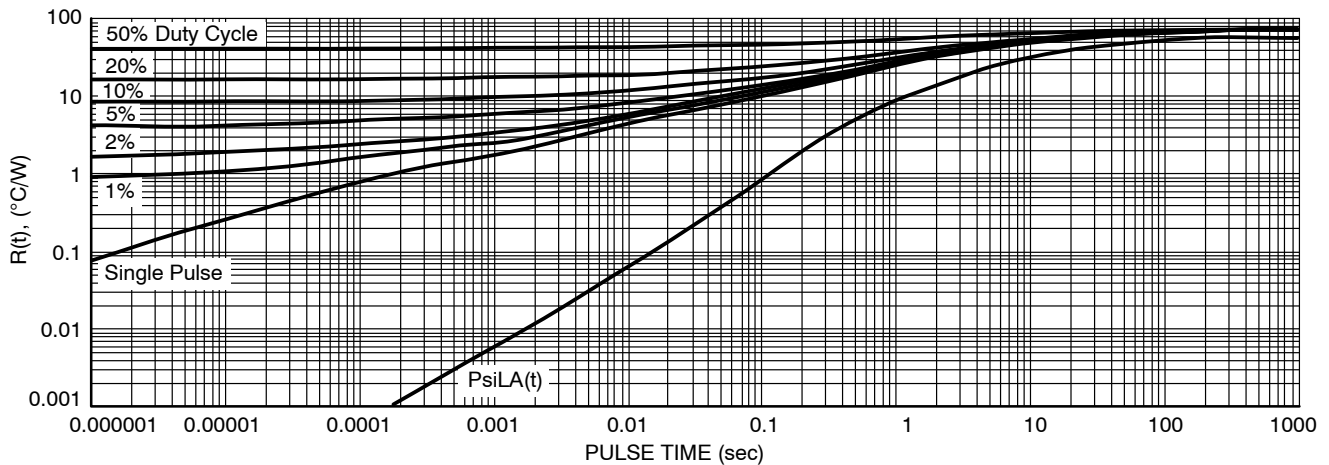


Figure 16. Junction to Ambient Transient Thermal Impedance (600 mm² Copper Area)

ISO 7637-2:2011 (E) PULSE TEST RESULTS

ISO 7637-2:2011(E) Test Pulse	Test Severity Levels, 13.5 V System		Delays and Impedance	# of Pulses or Test Time	Pulse / Burst Rep. Time
	III	IV			
1	-112	-150	2 ms, 10 Ω	500 pulses	0.5 s
2a	+55	+112	0.05 ms, 2 Ω	500 pulses	0.5 s
3a	-165	-220	0.1 μs, 50 Ω	1 h	100 ms
3b	+112	+150	0.1 μs, 50 Ω	1 h	100 ms

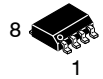
ISO 7637-2:2011(E) Test Pulse	Test Results	
	III	IV
1	C	C
2a	C	E
3a	C	C
3b	C	C

Class	Functional Status
C	One or more functions of a device do not perform as designed during exposure but return automatically to normal operation after exposure is removed.
E	One or more functions of a device do not perform as designed during and after exposure and cannot be returned to proper operation without replacing the device.

NCV8461

REVISION HISTORY

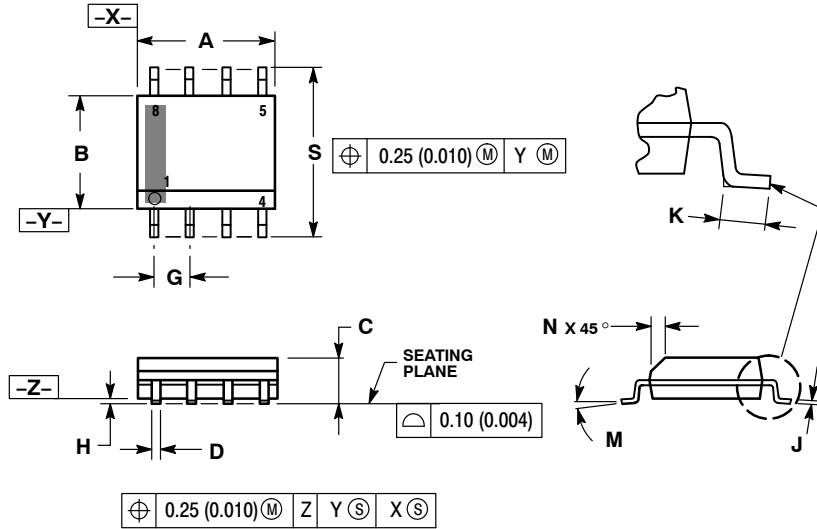
Revision	Description of Changes	Date
5	Rebranded the Data Sheet to onsemi format.	6/23/2025



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|--|---|---|---|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

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