

# Self-Protected Low Side Driver with In-Rush Current Management

## NCV8413

The NCV8413 is a three terminal protected Low-Side Smart Discrete FET. The protection features include Delta Thermal Shutdown, overcurrent, overtemperature, ESD and integrated Drain to Gate clamping for over voltage protection. The device also offers fault indication via the gate pin. This device is suitable for harsh automotive environments.

### Features

- Short Circuit Protection with In-Rush Current Management
- Thermal Shutdown with Automatic Restart
- Delta Thermal Shutdown
- Over Voltage Protection
- Integrated Clamp for Over Voltage Protection and Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Grade 1 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

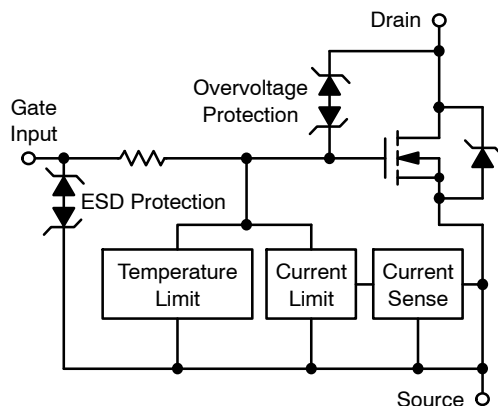


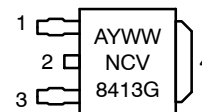
Figure 1. Block Diagram

$V_{DSS}$ (Clamped)	$R_{DS(ON)}$ TYP	$I_D$ MAX (Limited)
42 V	37 mΩ @ 10 V	22 A



DPAK  
CASE 369C  
STYLE 2

### MARKING DIAGRAM



A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

### PIN ASSIGNMENT – Style 2

1 = Gate  
2 = Drain  
3 = Source  
4 = Drain

### ORDERING INFORMATION

Device	Package	Shipping†
NCV8413DTRKG	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. MAXIMUM RATINGS

Rating	Symbol	Value (min)	Unit
Drain-to-Source Voltage Internally Clamped	$V_{DSS}$	42	V
Drain-to-Gate Voltage Internally Clamped	$V_{DG}$	42	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 14$	V
Drain Current – Continuous	$I_D$	Internally Limited	
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 2)	$P_D$	1.30 2.72	W
Thermal Resistance Junction-to-Case (Soldering Point) Junction-to-Case (Top) Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$R_{thJC}$ $R_{thJT}$ $R_{thJA}$ $R_{thJA}$	1.30 54.2 95.7 45.9	$^\circ\text{C/W}$
Single Pulse Inductive Load Switching Energy ( $L = 120\text{ mH}$ , $I_{Lpeak} = 2.8\text{ A}$ , $V_{GS} = 5\text{ V}$ , $R_G = 25\ \Omega$ , $T_{Jstart} = 25^\circ\text{C}$ )	$E_{AS}$	470	mJ
Load Dump Voltage ( $V_{GS} = 0$ and $10\text{ V}$ , $R_L = 4.5\ \Omega$ ) (Note 4)	$U_S^*$	55	V
Operating Junction Temperature	$T_J$	-40 to 150	$^\circ\text{C}$
Storage Temperature	$T_{storage}$	-55 to 150	$^\circ\text{C}$

ESD CHARACTERISTICS (Note 3, 5)

Electro-Static Discharge Capability Human Body Model (HBM) Charged Device Model (CDM)	ESD	4 1	kV
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Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted onto a 2" square FR4 board (100 sq mm, 1 oz. Cu, steady state)
2. Mounted onto a 2" square FR4 board (645 sq mm, 1 oz. Cu, steady state)
3. Not tested in production.
4. Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class C according to ISO16750-1.
5. This device series incorporates ESD protection and is tested by the following methods:  
ESD Human Body Model tested per AEC-Q100-002 (JS-001-2017)  
Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes smaller than 2 x 2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS-002-2018

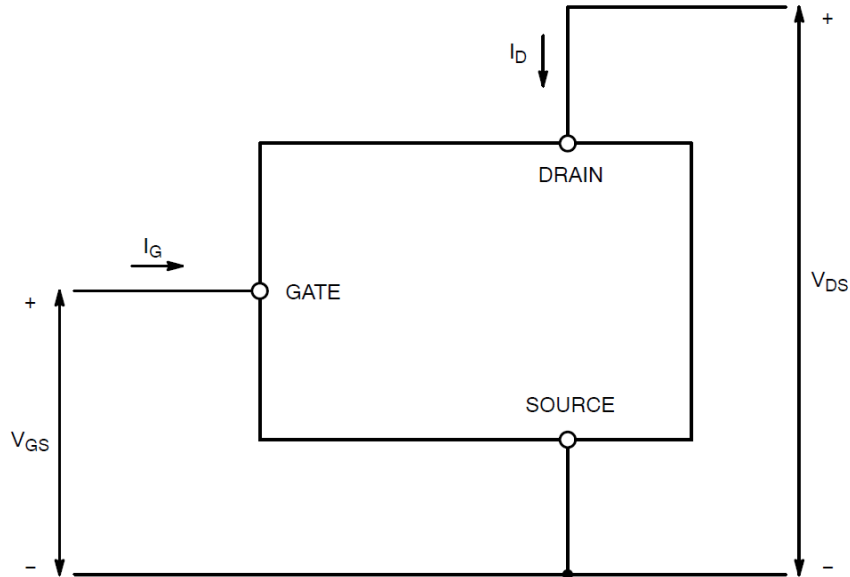


Figure 2. Voltage and Current Convention

# NCV8413

**Table 2. ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Clamped Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	$V_{(BR)DSS}$	42	46	51	V
	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_J = 150^\circ\text{C}$ (Note 6)		40	44	51	
Zero Gate Voltage Drain Current	$V_{DS} = 32\text{ V}, V_{GS} = 0\text{ V}$	$I_{DSS}$		0.6	5	$\mu\text{A}$
	$V_{DS} = 32\text{ V}, V_{GS} = 0\text{ V}, T_J = 150^\circ\text{C}$ (Note 6)			4		
Gate Input Current	$V_{GS} = 5\text{ V}, V_{DS} = 0\text{ V}$	$I_{GSS}$		50	125	$\mu\text{A}$
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1.2\text{ mA}$	$V_{GS(th)}$	1.0	1.7	2.2	V
Threshold Temperature Coefficient					-4	
Static Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}, T_J = 25^\circ\text{C}$	$R_{DS(ON)}$		37	68	$\text{m}\Omega$
	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}, T_J = 150^\circ\text{C}$ (Note 6)			75	123	
	$V_{GS} = 5\text{ V}, I_D = 3\text{ A}, T_J = 25^\circ\text{C}$			47	76	
	$V_{GS} = 5\text{ V}, I_D = 3\text{ A}, T_J = 150^\circ\text{C}$ (Note 6)			90	135	
Source Drain Forward On Voltage	$I_S = 7\text{ A}, V_{GS} = 0\text{ V}$	$V_{SD}$		0.85	1.1	V
<b>SWITCHING CHARACTERISTICS</b> (Note 6)						
Turn-On Time (10% $V_{GS}$ to 90% $I_D$ )	$V_{GS} = 0\text{ V to } 5\text{ V}, V_{DS} = 12\text{ V}, I_D = 1\text{ A}$	$t_{ON}$		25	35	$\mu\text{s}$
Turn-Off Time (90% $V_{GS}$ to 10% $I_D$ )		$t_{OFF}$		44	65	
Turn-On Time (10% $V_{GS}$ to 90% $I_D$ )	$V_{GS} = 0\text{ V to } 10\text{ V}, V_{DS} = 12\text{ V}, I_D = 1\text{ A}$	$t_{ON}$		15	25	$\mu\text{s}$
Turn-Off Time (90% $V_{GS}$ to 10% $I_D$ )		$t_{OFF}$		60	85	
Slew Rate On (80% $V_{DS}$ to 50% $V_{DS}$ )	$V_{GS} = 0\text{ V to } 10\text{ V}, V_{DD} = 12\text{ V}, R_L = 4.7\ \Omega$	$-dV_{DS}/dt_{ON}$	0.75	1.5		$\text{V}/\mu\text{s}$
Slew Rate Off (50% $V_{DS}$ to 80% $V_{DS}$ )		$dV_{DS}/dt_{OFF}$	0.6	0.98		
<b>SELF PROTECTION CHARACTERISTICS</b>						
Current Limit	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}$ (Note 7)	$I_{LIM}$	13	17	20	A
	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}, T_J = 150^\circ\text{C}$ (Notes 6, 7)		13	15.5	18	
	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$ (Notes 6, 7)		12	17	22	
	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}, T_J = 150^\circ\text{C}$ (Notes 6, 7)		11	15.5	20	
Temperature Limit (Turn-Off)	$V_{GS} = 5\text{ V}$ (Notes 6, 7)	$T_{LIM(OFF)}$	150	172	185	$^\circ\text{C}$
Thermal Hysteresis		$\Delta T_{LIM(ON)}$		15		
Temperature Limit (Turn-Off)	$V_{GS} = 10\text{ V}$ (Notes 6, 7)	$T_{LIM(OFF)}$	150	182	200	$^\circ\text{C}$
Thermal Hysteresis		$\Delta T_{LIM(ON)}$		15		
<b>GATE INPUT CHARACTERISTICS</b> (Note 6)						
Device ON Gate Input Current – Normal Operation	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}, I_D = 1\text{ A}$	$I_{GON}$	35	50	70	$\mu\text{A}$
	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}, I_D = 1\text{ A}$		200	310	450	
Device ON Gate Input Current – Thermal Limit	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}, I_D = 0\text{ A}$	$I_{GDTL}$	170	500	900	$\mu\text{A}$
	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}, I_D = 0\text{ A}$		900	1200	1700	
Device ON Gate Input Current – Current Limit	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}$	$I_{GCL}$	70	120	600	$\mu\text{A}$
	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$		710	970	1350	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Not tested in production.

7. Refer to Apps Note AND8202D for dependence of protection features on gate voltage.

TYPICAL CHARACTERISTICS

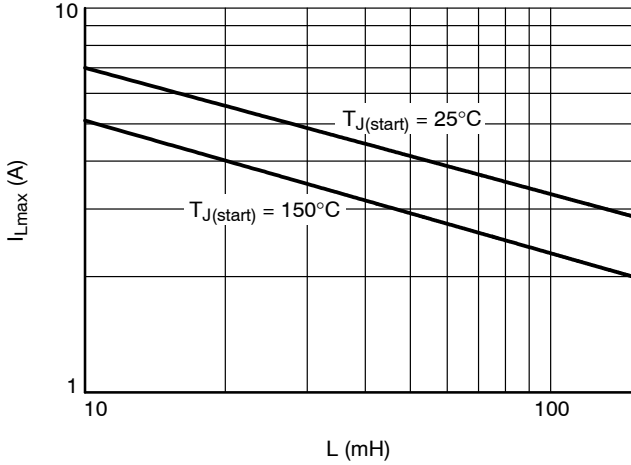


Figure 3. Single Pulse Maximum Switch-off Current vs. Load Inductance

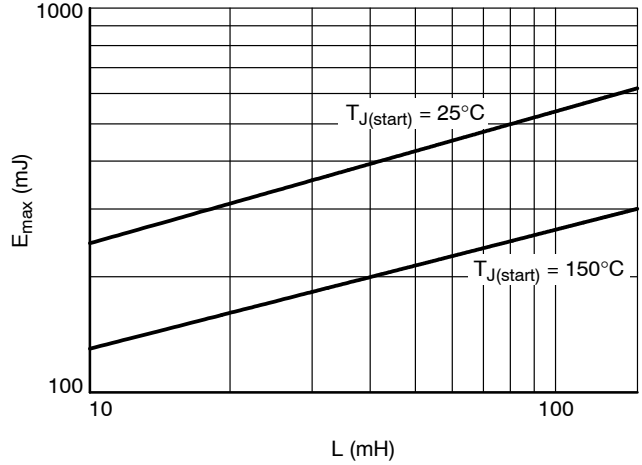


Figure 4. Single Pulse Maximum Switching Energy vs. Load Inductance

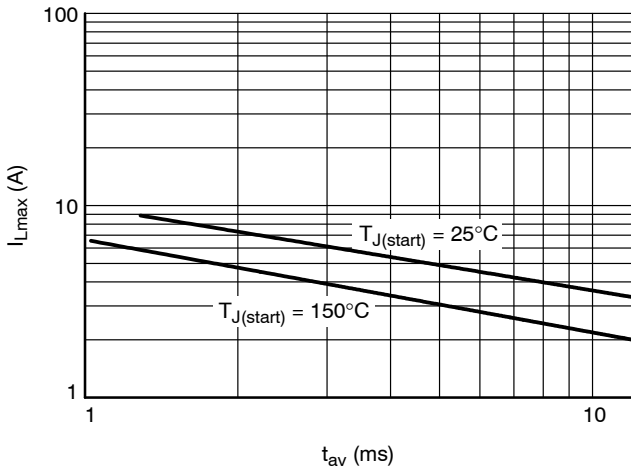


Figure 5. Single Pulse Maximum Inductive Switch-off Current vs. Time in Avalanche

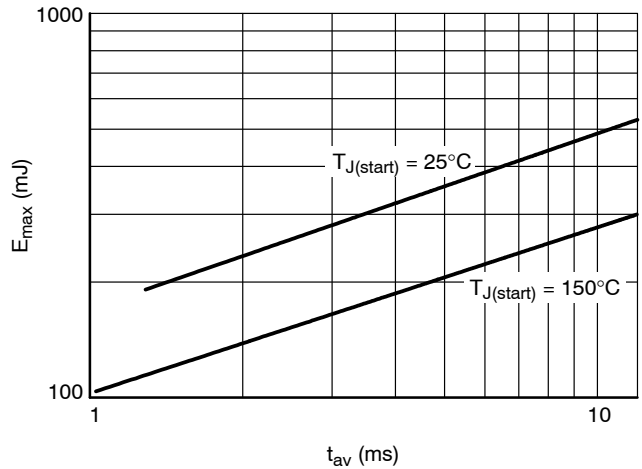


Figure 6. Single Pulse Maximum Inductive Switching Energy vs. Time in Avalanche

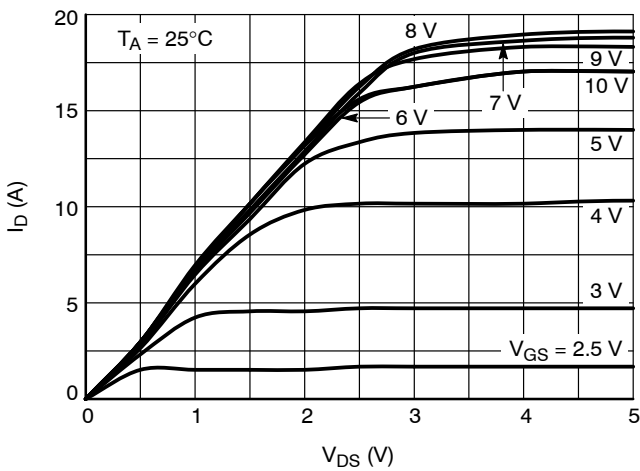


Figure 7. On-State Output Characteristics

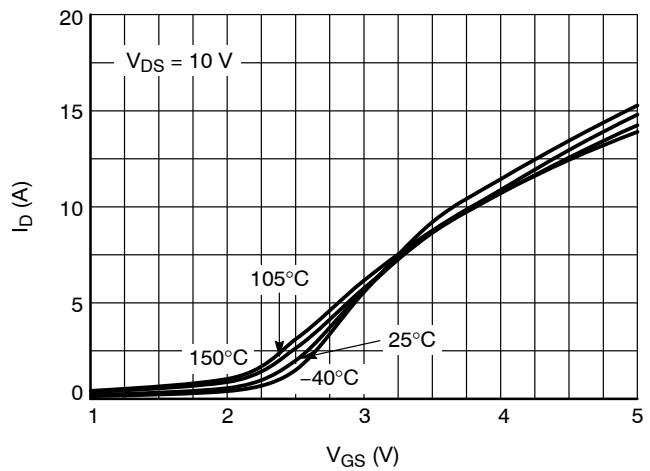


Figure 8. Transfer Characteristics

TYPICAL CHARACTERISTICS

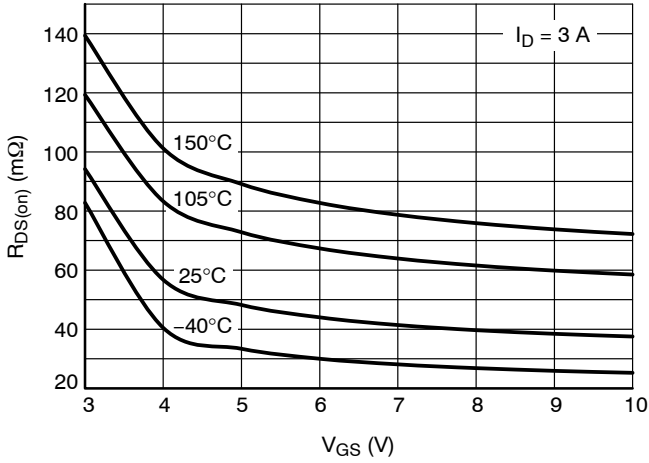


Figure 9.  $R_{DS(on)}$  vs. Gate-Source Voltage

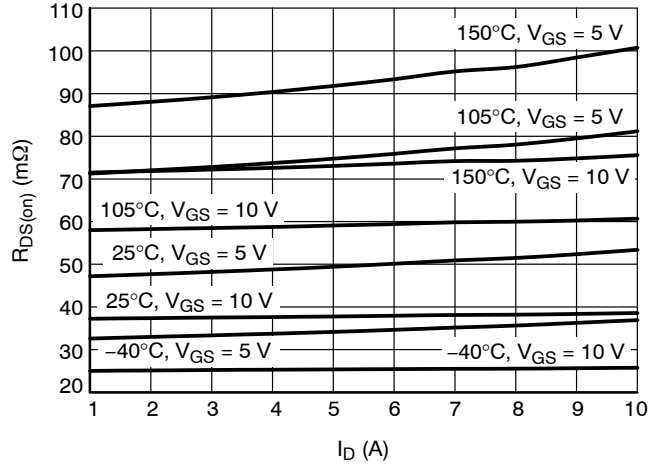


Figure 10.  $R_{DS(on)}$  vs. Drain Current

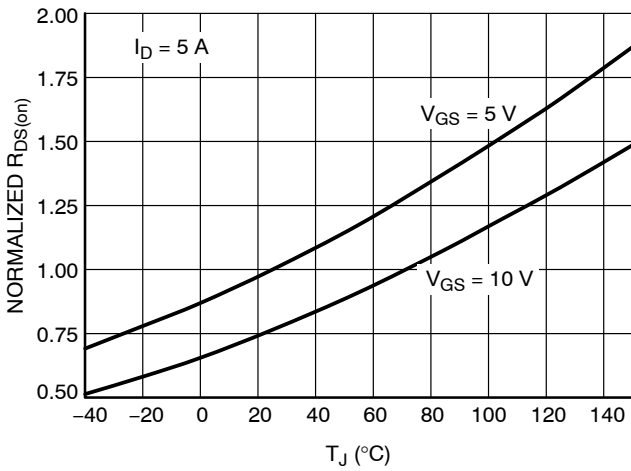


Figure 11. Normalized  $R_{DS(on)}$  vs. Temperature

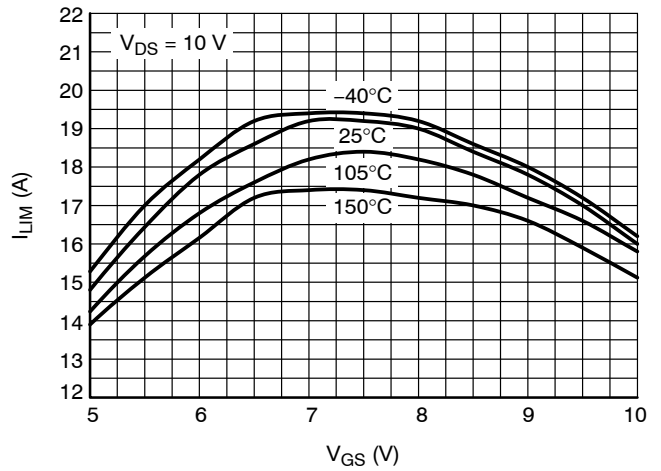


Figure 12. Current Limit vs. Gate-Source Voltage

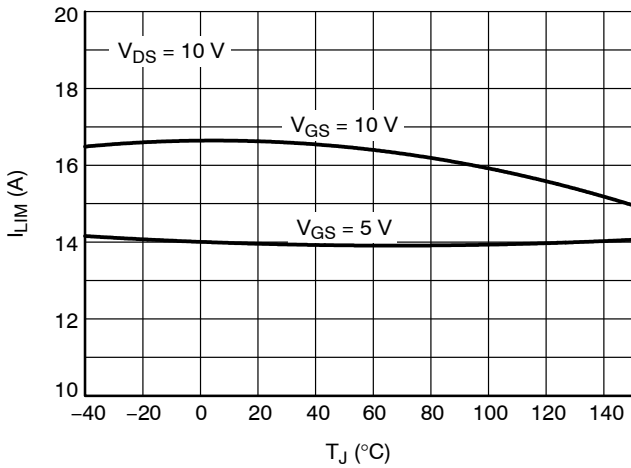


Figure 13. Current Limit vs. Junction Temperature

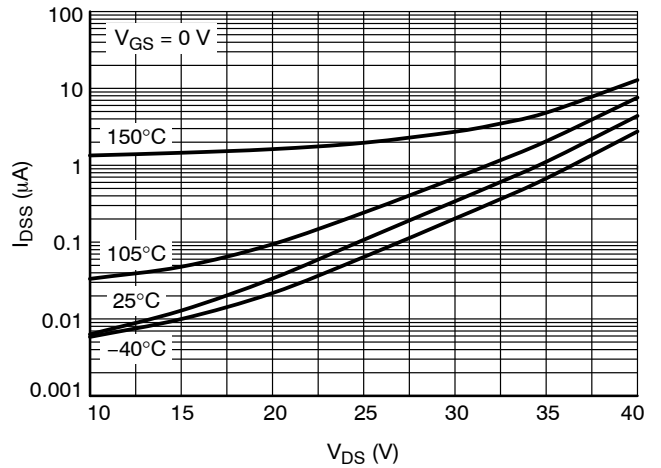


Figure 14. Drain-to-Source Leakage Current

TYPICAL CHARACTERISTICS

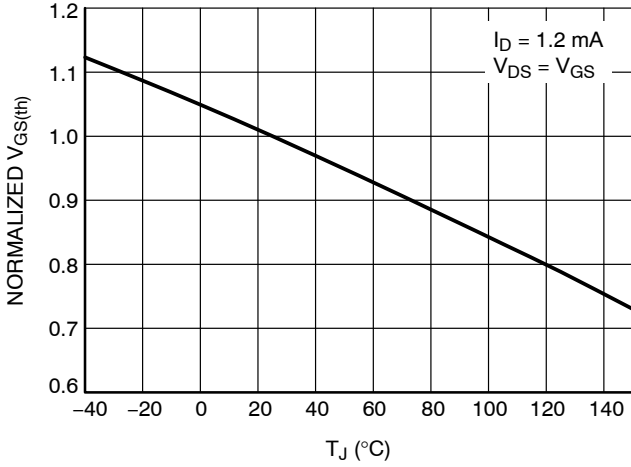


Figure 15. Normalized Threshold Voltage vs. Temperature

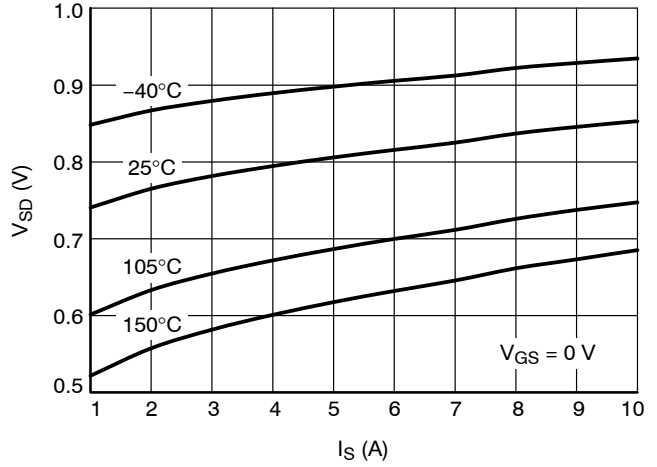


Figure 16. Source-Drain Diode Forward Characteristics

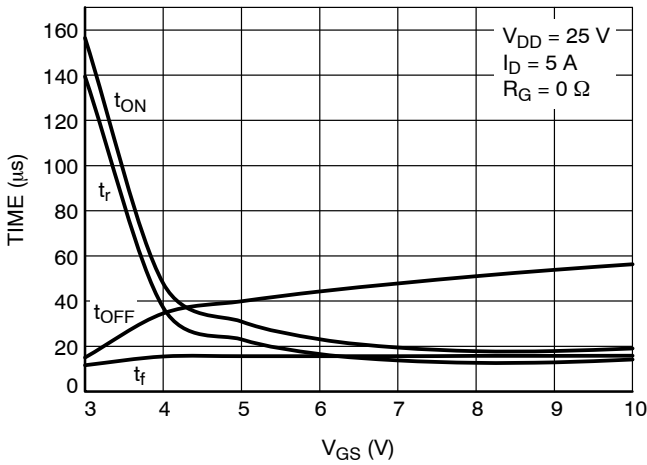


Figure 17. Resistive Load Switching Time vs. Gate-Source Voltage

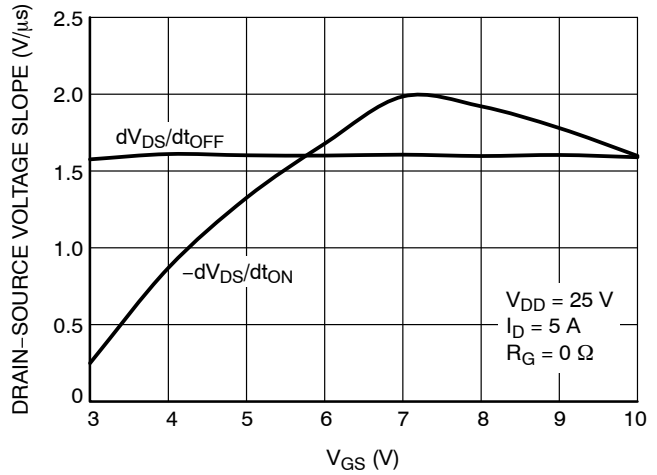


Figure 18. Resistive Load Switching Drain-Source Voltage Slope vs. Gate-Source Voltage

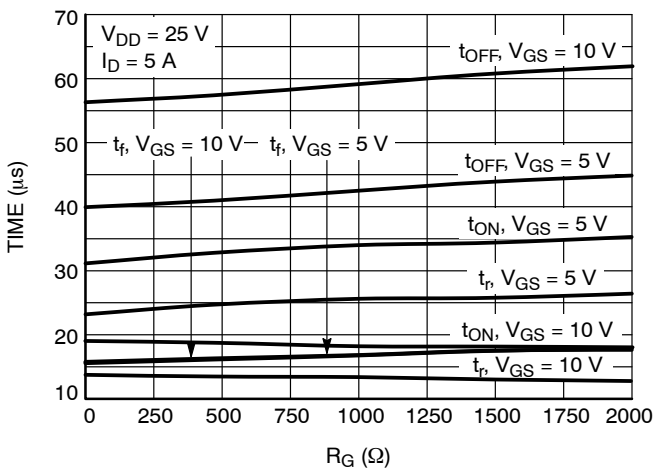


Figure 19. Resistive Load Switching Time vs. Gate Resistance

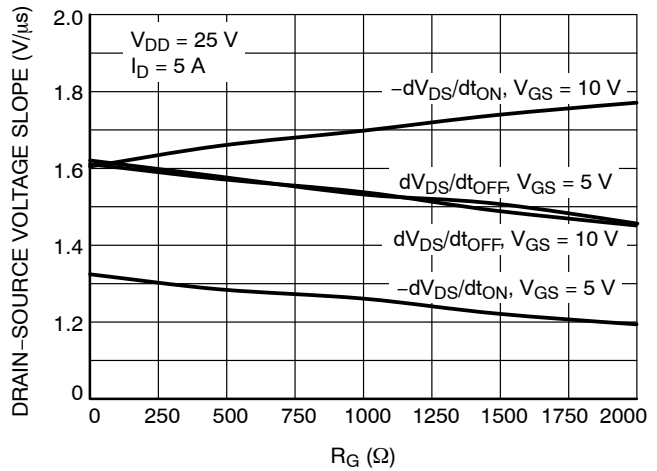


Figure 20. Resistive Load Switching Drain-Source Voltage Slope vs. Gate Resistance

TYPICAL CHARACTERISTICS

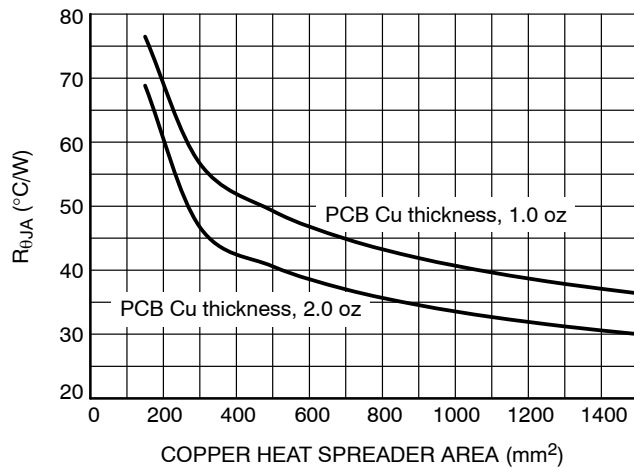


Figure 21.  $R_{\theta JA}$  vs. Copper Area

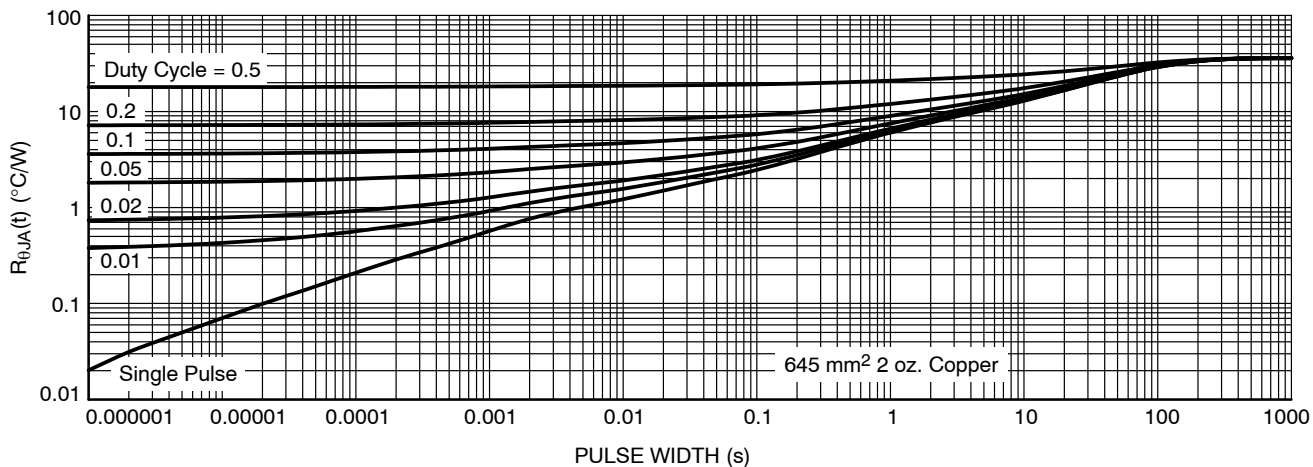


Figure 22. Transient Thermal Resistance

APPLICATION INFORMATION

**Circuit Protection Features**

The NCV8413 has three main protections. Current Limit, Thermal Shutdown and Delta Thermal Shutdown. These protections establish robustness of the NCV8413.

**Current Limit and Short Circuit Protection**

The NCV8413 has current sense element. In the event that the drain current reaches designed current limit level, integrated Current Limit protection establishes its constant level.

**Delta Thermal Shutdown**

Delta Thermal Shutdown (DTSD) Protection increases higher reliability of the NCV8413. DTSD consist of two independent temperature sensors – cold and hot sensors. The NCV8413 establishes a slow junction temperature rise by sensing the difference between the hot and cold sensors. ON/OFF output cycling is designed with hysteresis that results in a controlled saw tooth temperature profile (Figure 24). The die temperature slowly rises (DTSD) until the absolute temperature shutdown (TSD) is reached around 172°C.

**Thermal Shutdown with Automatic Restart**

Internal Thermal Shutdown (TSD) circuitry is provided to protect the NCV8413 in the event that the maximum

junction temperature is exceeded. When activated at typically 172°C, the NCV8413 turns off. This feature is provided to prevent failures from accidental overheating.

**EMC Performance**

If better EMC performance is needed, connect a small ceramic capacitor to the drain pin as close to the device as possible according to Figure 23.

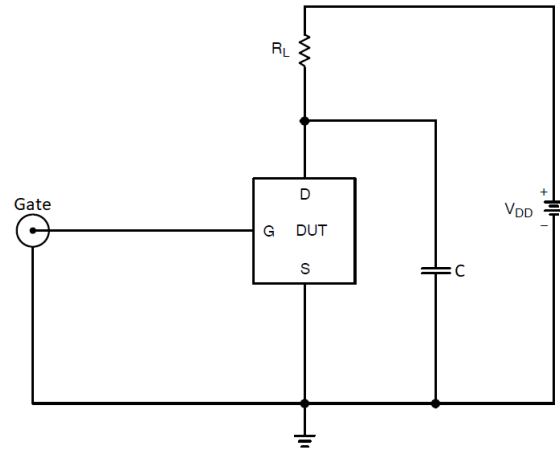


Figure 23. EMC Capacitor Placement

TEST CIRCUITS AND WAVEFORMS

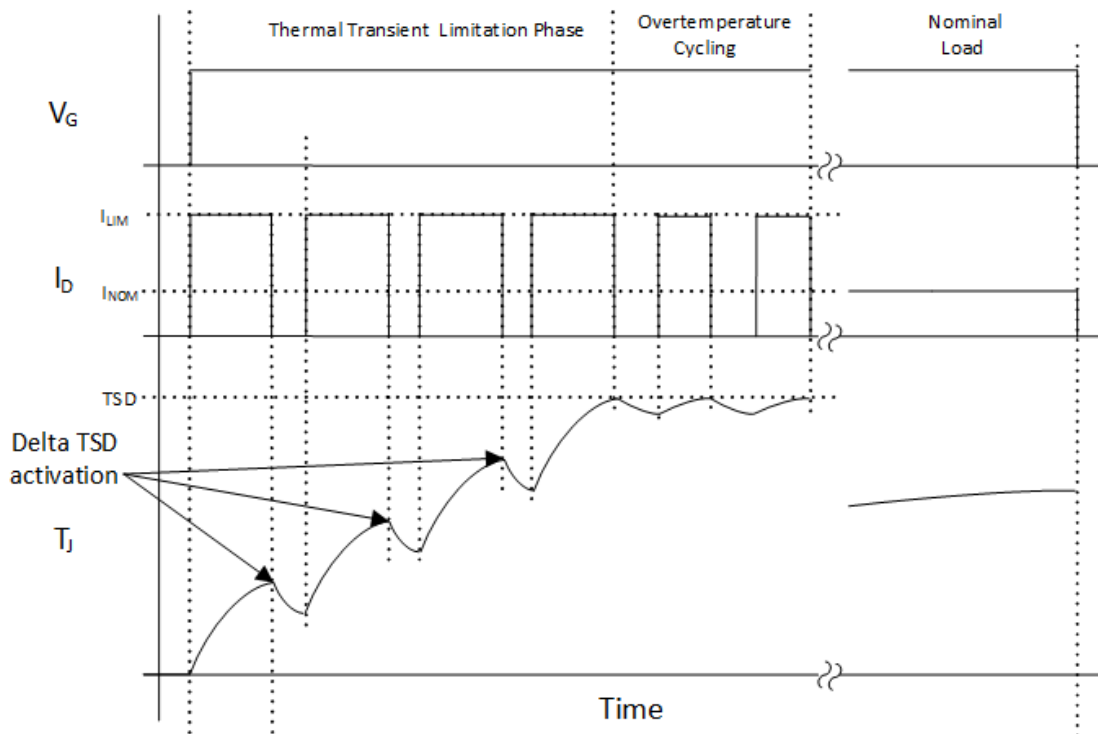


Figure 24. Overload Protection Behavior

TEST CIRCUITS AND WAVEFORMS

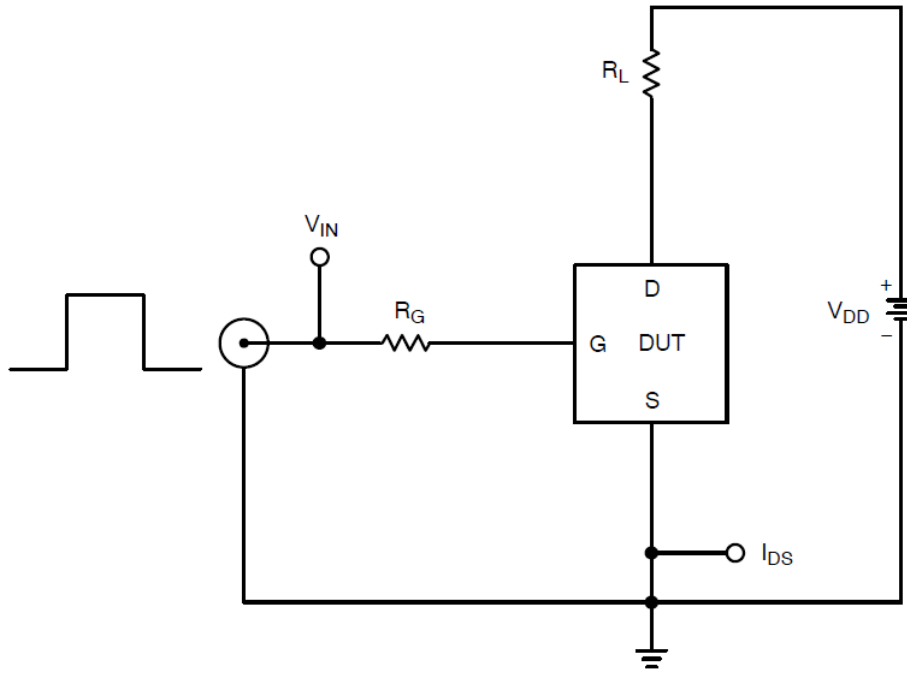


Figure 25. Resistive Load Switching Test Circuit

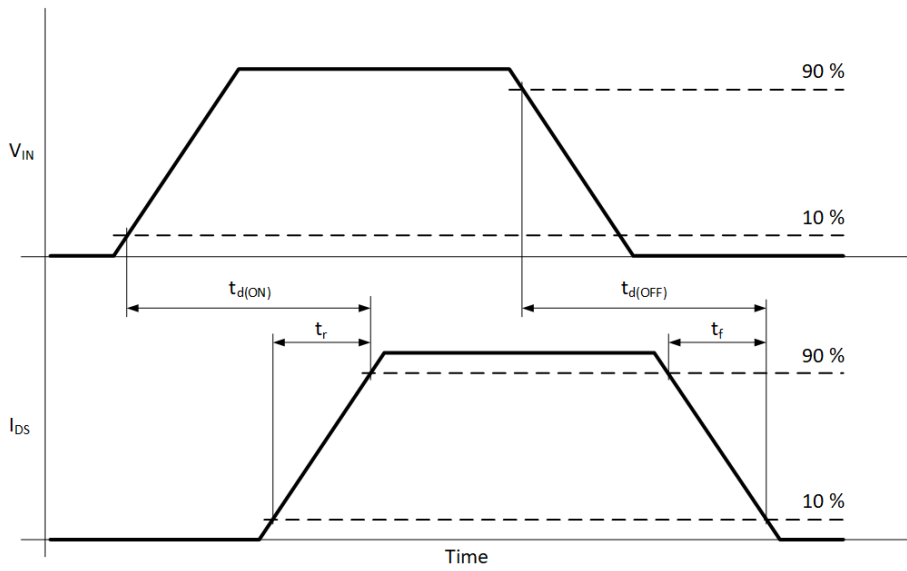


Figure 26. Resistive Load Switching Waveforms

TEST CIRCUITS AND WAVEFORMS

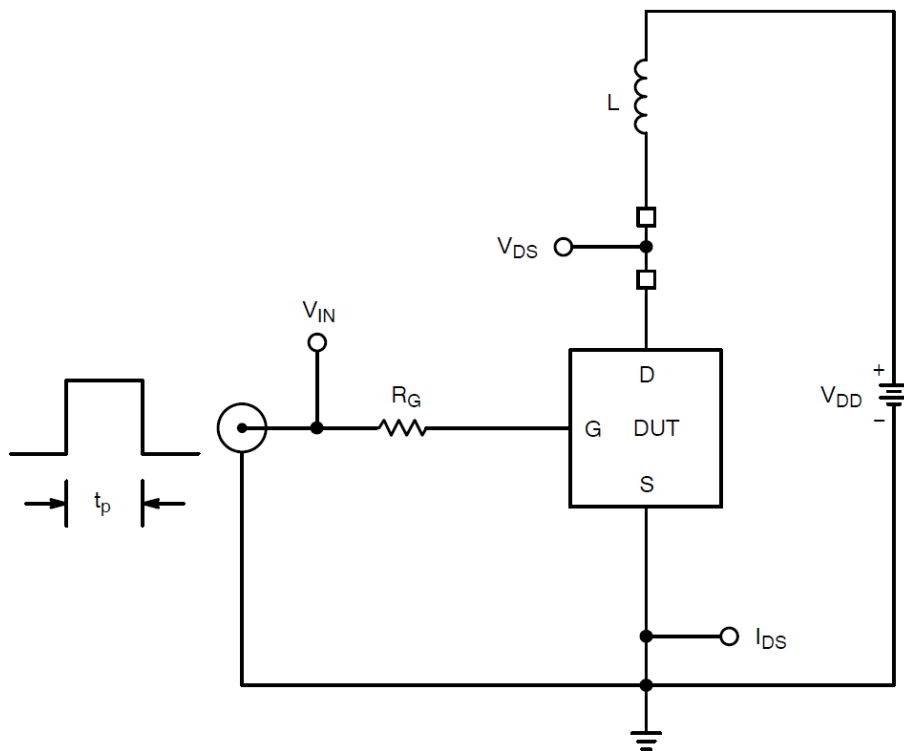


Figure 27. Inductive Load Switching Test Circuit

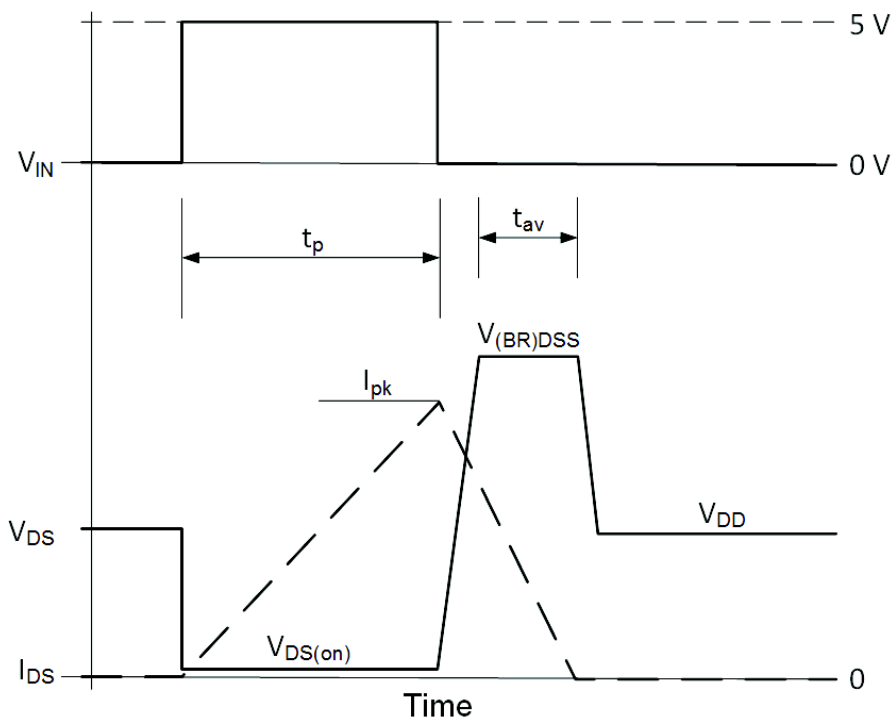
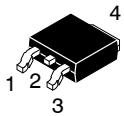


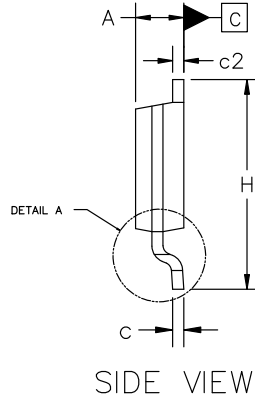
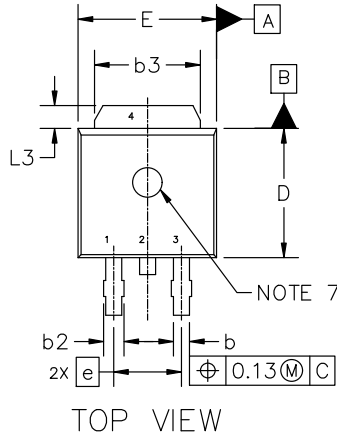
Figure 28. Inductive Load Switching Waveform



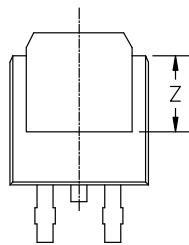
DPAK-3 6.10x6.54x2.28, 2.29P  
CASE 369C  
ISSUE K

DATE 14 MAY 2026

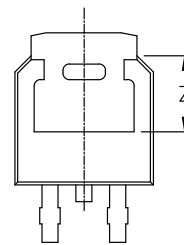
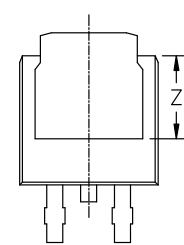
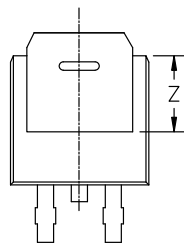
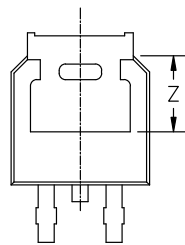
SCALE 1:1



MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



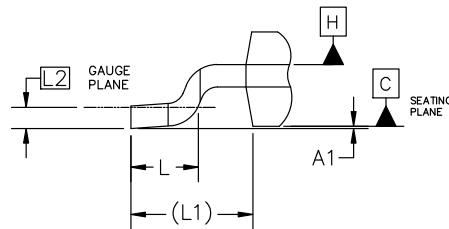
BOTTOM VIEW



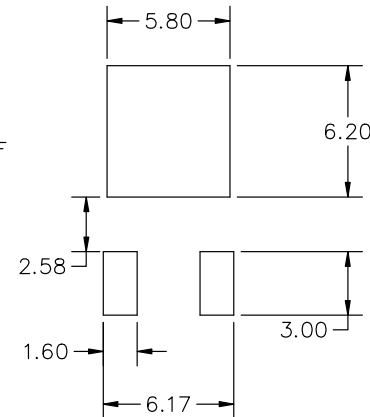
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A  
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

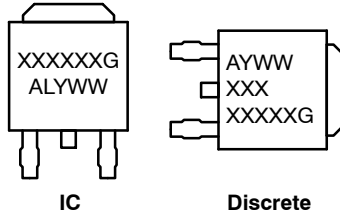
<b>DOCUMENT NUMBER:</b>	<b>98AON10527D</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>DPAK-3 6.10x6.54x2.28, 2.29P</b>	<b>PAGE 1 OF 2</b>

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**DPAK-3 6.10x6.54x2.28, 2.29P**  
**CASE 369C**  
**ISSUE K**

DATE 13 MAY 2026

**GENERIC  
MARKING DIAGRAM\***



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- |  |  |   |   |  |
|--|--|---|---|--|
| <p>STYLE 1:<br/> PIN 1. BASE<br/> 2. COLLECTOR<br/> 3. EMITTER<br/> 4. COLLECTOR</p> | <p>STYLE 2:<br/> PIN 1. GATE<br/> 2. DRAIN<br/> 3. SOURCE<br/> 4. DRAIN</p>          | <p>STYLE 3:<br/> PIN 1. ANODE<br/> 2. CATHODE<br/> 3. ANODE<br/> 4. CATHODE</p> | <p>STYLE 4:<br/> PIN 1. CATHODE<br/> 2. ANODE<br/> 3. GATE<br/> 4. ANODE</p>              | <p>STYLE 5:<br/> PIN 1. GATE<br/> 2. ANODE<br/> 3. CATHODE<br/> 4. ANODE</p>     |
| <p>STYLE 6:<br/> PIN 1. MT1<br/> 2. MT2<br/> 3. GATE<br/> 4. MT2</p>                 | <p>STYLE 7:<br/> PIN 1. GATE<br/> 2. COLLECTOR<br/> 3. EMITTER<br/> 4. COLLECTOR</p> | <p>STYLE 8:<br/> PIN 1. N/C<br/> 2. CATHODE<br/> 3. ANODE<br/> 4. CATHODE</p>   | <p>STYLE 9:<br/> PIN 1. ANODE<br/> 2. CATHODE<br/> 3. RESISTOR ADJUST<br/> 4. CATHODE</p> | <p>STYLE 10:<br/> PIN 1. CATHODE<br/> 2. ANODE<br/> 3. CATHODE<br/> 4. ANODE</p> |

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