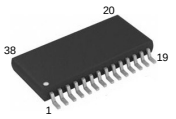
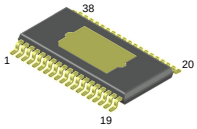
High Efficiency Single-chip 2 Phase Booster and Synchronous Dual Buck LED Driver for Automotive Front Lighting

NCV78964



TSSOP38 EP
CASE 137AB



TSSOP38 TEP
CASE 948BX

The NCV78964 is a single-chip and high efficient 2 phase Booster and Synchronous Dual-Channel Buck LED Driver designed for automotive front lighting applications like high beam, low beam, DRL (daytime running light), turn indicator, fog light, static cornering, etc. The NCV78964 is in particular designed for high current LEDs and provides a complete solution to drive two LED strings of up-to 60 V with minimum of external components.

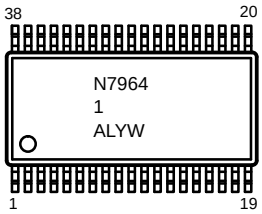
The device integrates a current-mode voltage booster controller, realizing a unique input current filter with a limited BOM. When more than two LED channels are required on one module, then two, three or more NCV78964 devices can be combined, with the possibility for the booster circuits to operate in multiphase-mode. This helps to further optimize the filtering effect of the booster circuit and allows a cost effective dimensioning for mid to high power LED systems.

Thanks to the SPI programmability, one single hardware configuration can support various application platforms.

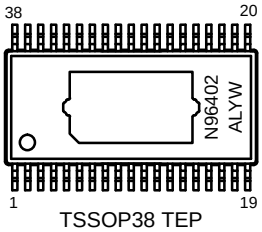
Features

- Single Chip 2 Phase Booster and Synchronous Dual Buck Solution
- Stand-Alone/Limp Home Mode
- 2 LED Strings up-to 60 V, High Current Capability 1.6 A per Output
- Switched Mode Synchronous Bucks with Average Current Regulation through the LEDs, Programmable Buck Frequency
- Independent Supply Voltage for Each Buck Channel
- Buck Constant Voltage Mode Available
- Booster Shunt-less Operation
- Built-in Programmable Booster Soft-Start
- Superior Stability and Response Time
- Designed for Small Booster Output Capacitor
- Low EMC Emission
- High Operating Frequencies to Reduce Inductor Size − up to 2 MHz
- 4 MHz SPI Interface for Dynamic Control of System Parameters
- 48 V Battery System Compliant
- ASIL B Compliant; AEC-Q100 Qualified and PPAP Capable
- These Device are Pb-Free, Halide Free/BFR Free and are RoHS Compliant

MARKING DIAGRAM



TSSOP38 EP



TSSOP38 TEP

N7964, N96402	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week

SAFETY DESIGN – ASIL B

ASIL B Product developed in compliance with ISO 26262 for which a complete safety package is available.

ORDERING INFORMATION

See detailed ordering and shipping information on page 55 of this data sheet.

Typical Applications

- High Beam, Low Beam
- Turn Indicator, DRL
- Position or Park light
- Fog and Static Cornering
- Adaptive Driving Beam, Pixel Applications

TYPICAL APPLICATION SCHEMATIC

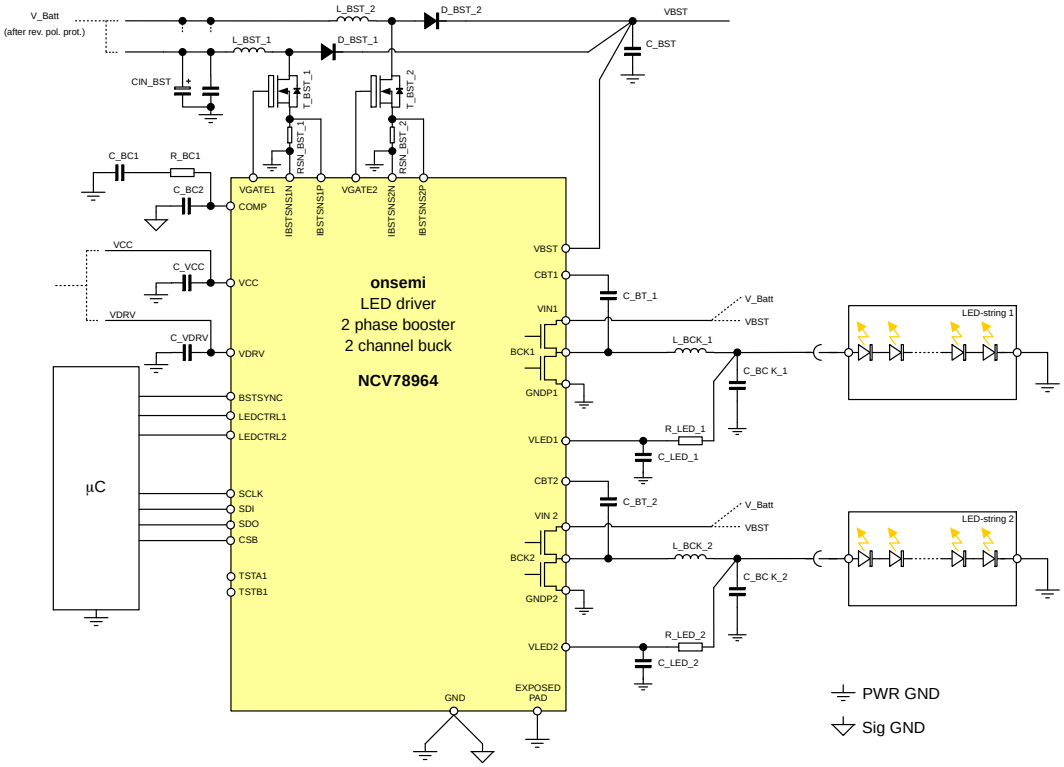


Figure 1. Typical Application Schematic

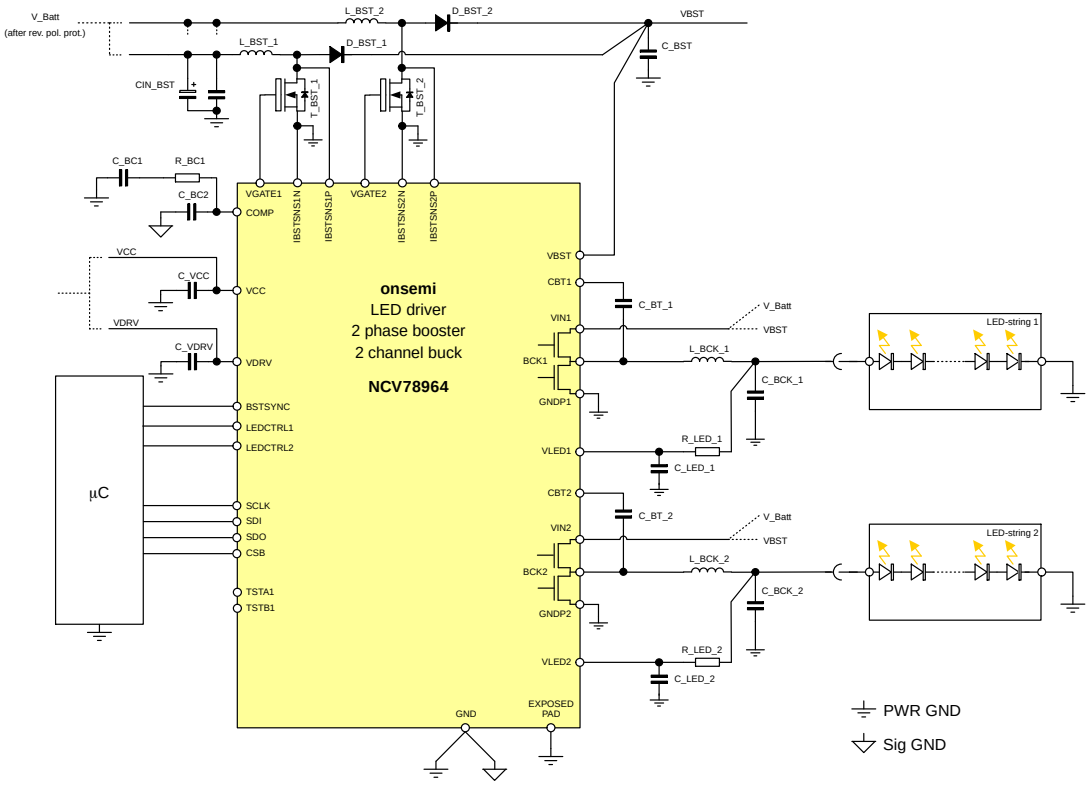


Figure 2. Typical Application Schematic − Current Sensing on Booster MOSFETs

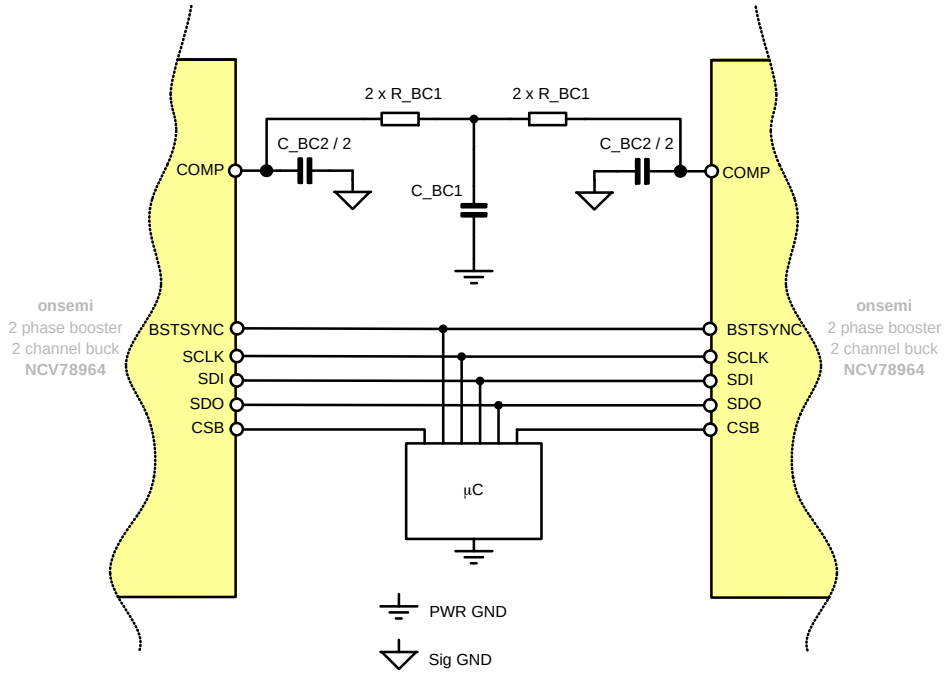


Figure 3. Application Schematic − COMP Connection when Using 4 Phase Booster

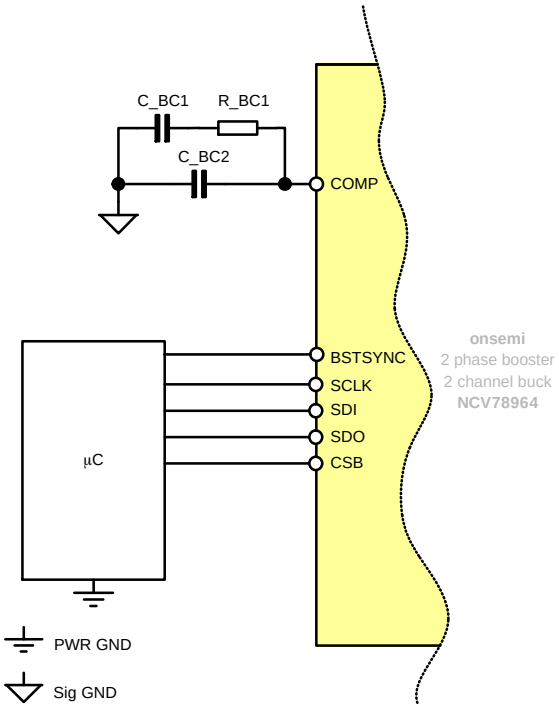


Figure 4. Application Schematic − COMP Connection when Using 2 Phase Booster

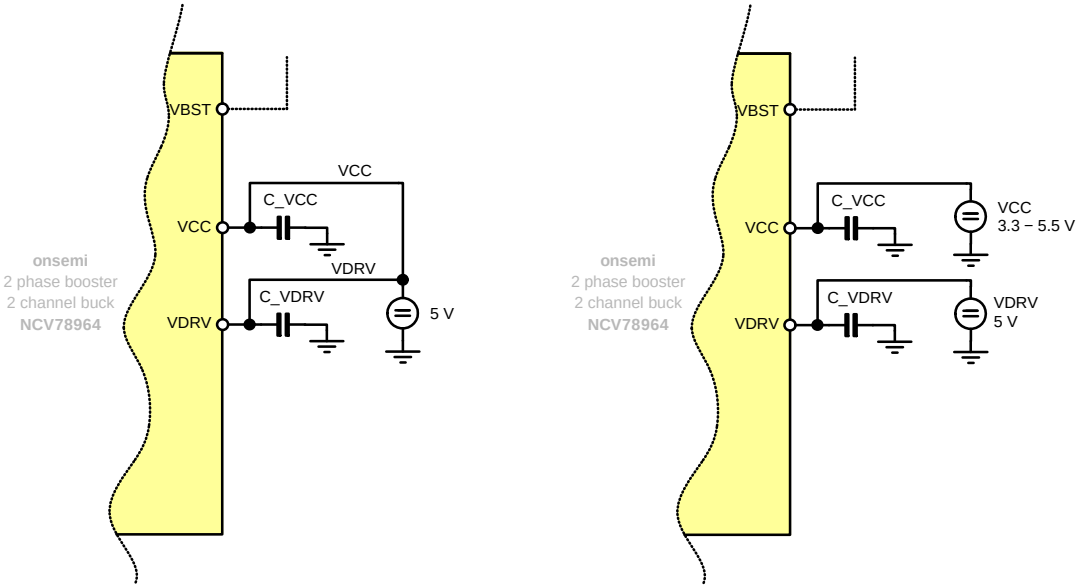


Figure 5. Application Schematic − SUPPLY Connection Possibilities

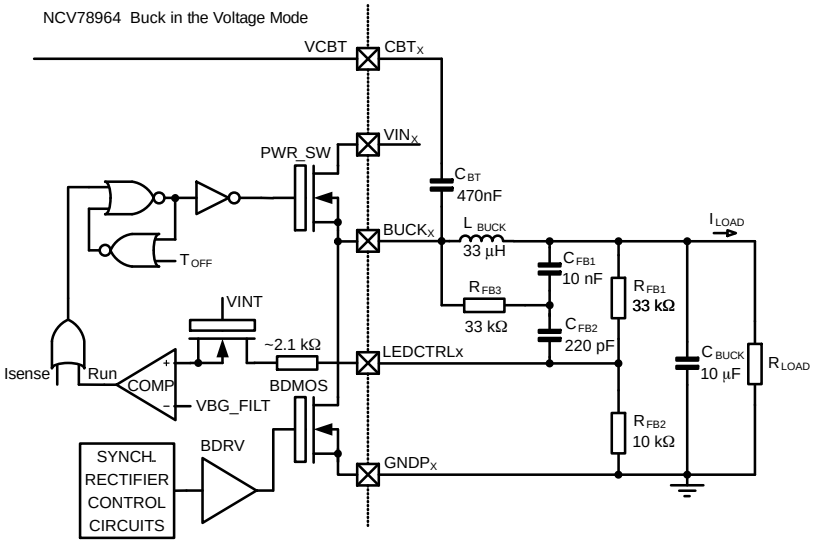


Figure 6. Typical Application Schematic − Buck Voltage Mode

Table 1. EXTERNAL COMPONENTS

Component	Function	Typ. Value	Unit
L_BCK_x	Buck Regulator Coil (See BUCK REGULATOR Chapter for Details)	100	µH
C_BCK_x	Buck Regulator Output Capacitor (See BUCK REGULATOR Chapter for Details)	220	nF
C_BT_x	Bootstrap Capacitor	Min. 300, Typ. 470, Max. 2600	nF
C_VCC	V_{CC} Decoupling Capacitor	470	nF
C_DRV	V_{DRIVE} Decoupling Capacitor	470	nF
R_LED_x	VLEDx Pin Serial Resistor (Notes 1 and 2)	Typ. 1, Max. 2	kΩ
C_LED_x	Optional VLEDx Pin Filter Capacitor (Note 2)	1	nF
T_BST_x	Boost Regulator External Switch (Note 3)	NVMFS6H858NLWFT1G	
D_BST_x	Boost Regulator External Diode	NRVB10100MFST1G	
RSN_BST_x	Booster Shunt Resistor	10	mΩ
L_BST_x	Boost Regulator Inductor	10	µH
C_BST	Booster Ceramic Output Capacitor	22	µF
C_BST_E	Optional Booster Electrolytic Output Capacitor	22	µF
COMP	Booster Compensation Network Components	C_BC1 = 47 nF, R_BC1 = 3.3 kΩ, C_BC2 = 470 pF	

1. R_LED_x is necessary to ensure Absolute maximum ratings of IVLEDx current (see Table 3).
2. C_LED_x is optional. If used, time constant of the C_LED_x and R_LED_x filter has to be lower than minimal LEDCTRLx PWM time for proper VLED measurement.
3. Logic level N-Channel MOSFET.

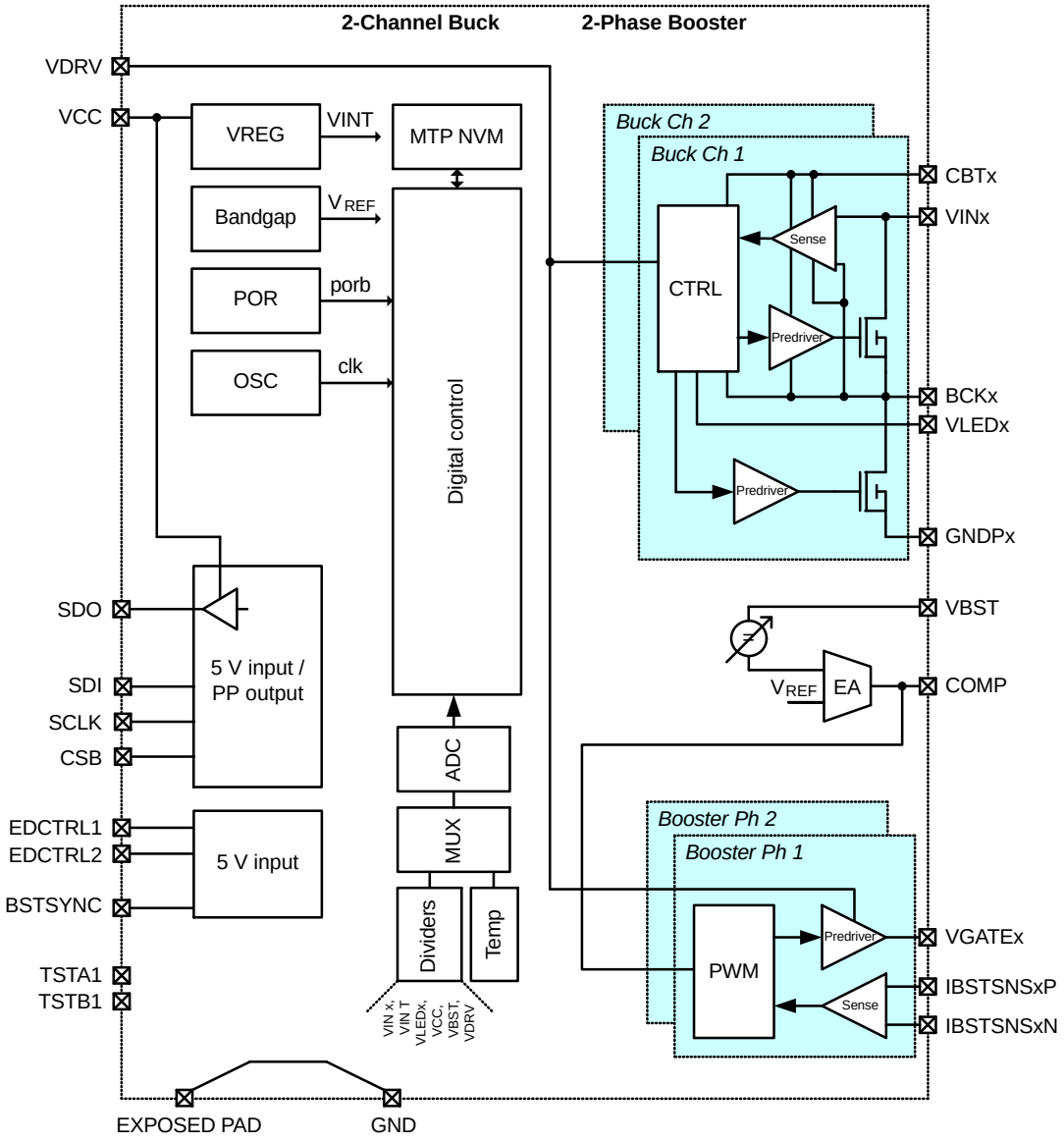


Figure 7. Block Diagram

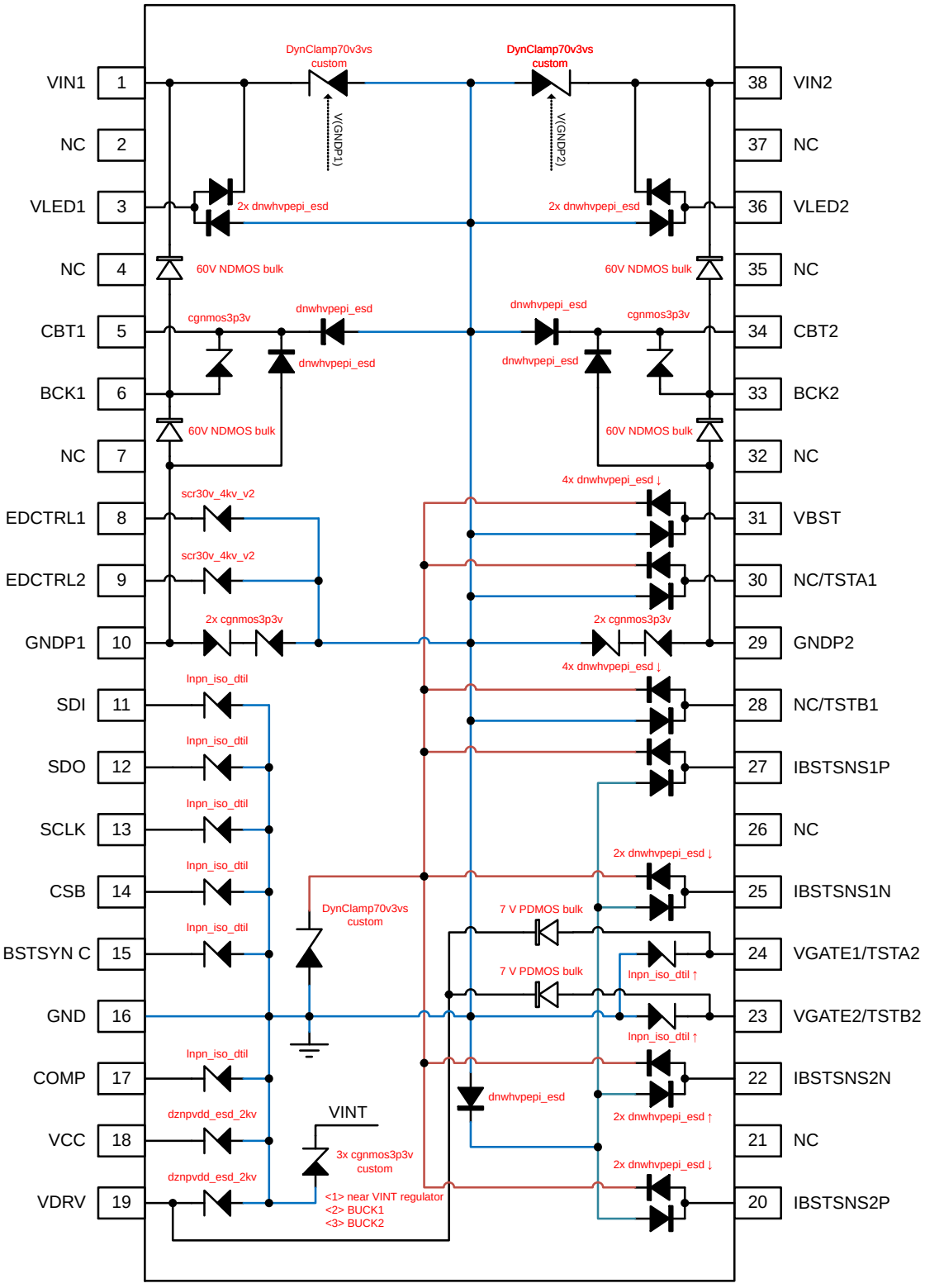


Figure 8. ESD Schematic

PACKAGE AND PIN DESCRIPTION

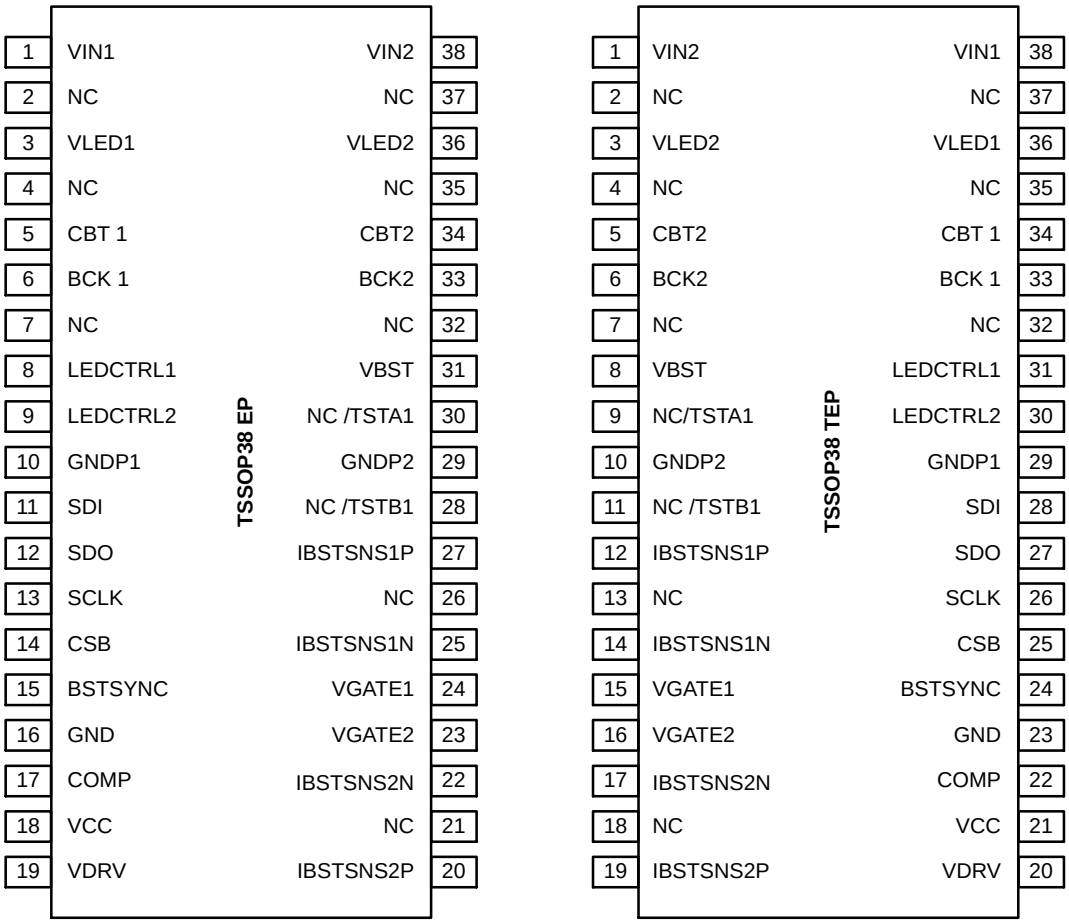


Figure 9. Pin Connections (Top View) − TSSOP38 EP and TSSOP38 TEP (Top Exposed Pad)

Table 2. PIN DESCRIPTION

Pin No. TSSOP38 EP	Pin No. TSSOP38 TEP	Pin Name	Description	I/O Type
1	38	VIN1	Buck1 input pin	HV Analog
2	37	NC	Not Connected (to be left floating)	
3	36	VLED1	VLED1 voltage sense pin	HV Analog
4	35	NC	Not Connected (to be left floating)	
5	34	CBT1	Buck1 bootstrap capacitor pin	HV Analog
6	33	BCK1	Buck1 output pin	HV Analog
7	32	NC	Not Connected (to be left floating)	
8	31	LEDCTRL1	Buck1 control signal	DI, 5V
9	30	LEDCTRL2	Buck2 control signal	DI, 5V
10	29	GNDP1	Buck1 power ground	Ground
11	28	SDI	SPI data in pin	DI, 5V
12	27	SDO	SPI data out pin	DO, 5V
13	26	SCLK	SPI clock pin	DI, 5V
14	25	CSB	SPI chip select pin	DI, 5V
15	24	BSTSYNC	External clock for the booster	DI, 5V
16	23	GND	Ground pin	Ground
17	22	COMP	Compensation for the booster regulator	MV Analog
18	21	VCC	3.3 or 5 V supply pin	MV supply
19	20	VDRV	5V supply pin	MV supply
20	19	IBSTSNS2P	Booster current positive feedback input (phase 2)	HV Analog
21	18	NC	Not Connected (to be left floating)	
22	17	IBSTSNS2N	Booster current negative feedback input (phase 2)	HV Analog
23	16	VGATE2	Booster MOSFET gate pre-driver (phase 2)	MV Analog, DO
24	15	VGATE1	Booster MOSFET gate pre-driver (phase 1)	MV Analog, DO
25	14	IBSTSNS1N	Booster current negative feedback input (phase 1)	HV Analog
26	13	NC	Not Connected (to be left floating)	
27	12	IBSTSNS1P	Booster current positive feedback input (phase 1)	HV Analog
28	11	NC	Not Connected (to be left floating)	DO, HV
29	10	GNDP2	Buck2 power ground	Ground
30	9	NC	Not Connected (to be left floating)	DO, HV
31	8	VBST	Booster voltage feedback input	HV Analog
32	7	NC	Not Connected (to be left floating)	
33	6	BCK2	Buck2 output pin	HV Analog
34	5	CBT2	Buck2 bootstrap capacitor pin	HV Analog
35	4	NC	Not Connected (to be left floating)	
36	3	VLED2	VLED2 voltage sense pin	HV Analog
37	2	NC	Not Connected (to be left floating)	
38	1	VIN2	Buck2 input pin	HV Analog
EP		EXPOSED PAD	To be tied to GND	

Table 3. ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Min	Max	Unit
Buck Input Voltage (Note 4, 5)	VINx	−0.3	66	V
Boost Voltage Feedback Input (Note 4)	VBST	−0.3	66	V
Output Pin to the Buck Coil (Notes 5, 6)	BCKx	VGNDPx − 0.3	VINx + 0.3	V
VCC Supply Voltage	VCC	−0.3	6	V
VDRV Supply Voltage	VDRV	−0.3	6	V
LED Voltage Sense Pin	VLEDx	−0.3	66	V
The Bootstrap Capacitor Pin	CBTx	Max of (BCKx − 0.3, −0.3)	BCKx + 3.6	V
Buck Control Signal (Note 9)	LEDCTRLx	−0.3	6	V
SPI Clock Signal	SCLK	−0.3	6	V
SPI Chip Select Signal	CSB	−0.3	6	V
SPI Data Input Signal	SDI	−0.3	6	V
SPI Data Output Signal	SDO	−0.3	6	V
BSTSYNC Signal	BSTSYNC	−0.3	6	V
Boost Current Sensing Positive Input (Note 4)	IBSTSNSxP	−3	68	V
Boost Current Sensing Negative Input (Note 4)	IBSTSNSxN	−3	68	V
Boost Regulator Stability Compensation	COMP	−0.3	6	V
Boost Switch Gate Driver Output	VGATE	−0.3	VDRV + 0.3	V
Peak Voltage at Buck Power Ground	GNDPD	−2	2	V
Buck Power Ground (Note 10, 11)	GNDP	−0.3	0.3	V
VLED Pin Sink/Source Current	IVLEDx	−30	30	mA
Storage Temperature (Note 7)	T_{STRG}	−50	150	°C
The Exposed Pad (Note 8)	EXPAD	−0.3	0.3	V
Electrostatic Discharge on Component Level Human Body Model (Note 12)	V_{ESD_HBM}	−2	+2	kV
Electrostatic Discharge on Component Level Charge Device Model (Note 12)	V_{ESD_CDM}	−500	+500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Absolute maximum rating for VINx, VBST and IBSTSNSxP pins is 70 V for limited time < 50 ms to comply with ISO21780:2020
5. V(VINx − BCKx) < 68 V
6. The HS switch in OFF state during the test of the rating
7. For limited time up to 100 hours. Otherwise the max storage temperature is 85 °C.
8. The exposed pad must be hard wired to GND pin in the application to ensure both electrical and thermal connection.
9. For ATE max = 30 V
10. Peak voltage after 100 ns single pole low pass filter
11. For ATE max = 3.6 V
12. This device series incorporates ESD protection and is tested by the following methods:
    ESD Human Body Model tested per ANSI/ESDA/JEDEC JS-001
    ESD Charge Device Model tested per EIA-JESD22-C101
    Latch-up Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78

Operating ranges define the limits for functional operation and parametric characteristics of the device. A mission profile (Note 13) is a substantial part of the operation conditions; hence the Customer must contact **onsemi** in order to mutually agree in writing on the allowed missions profile(s) in the application.

Table 4. RECOMMENDED OPERATING RANGES

Characteristic	Symbol	Min	Typ	Max	Unit
Buck Input Voltage with Limited Max. Peak Current (Note 14)	VINxL	6	−	6.7	V
Buck Input Voltage (Note 15)	VINx	6.7	−	65	V
VCC Voltage Supply	VCC	3	3.3/5	5.5	V
VCC Voltage Supply During Memory Programming	VCCM	3.1	−	5.5	V
VDRV Supply Voltage	VDRV	4.5	5	5.5	V
Buck Switch Average Output Current	IAVG_BCKx	−	−	1.6	A
Ambient Temperature Range		−40	−	125	°C
Parametric Operating Junction Temperature Range (Note 17, 20)	T_{JP}	−40	−	150	°C
Functional Operating Junction Temperature Range (Note 18, 20)	T_{JF}	−45	−	160	°C
Junction Temperature Range During Memory Programming (Note 16, 20)	T_{JM}	−40	−	85	°C
The Exposed Pad Connection (Note 19)	EXPOSED_PAD	GND − 0.1	GND	GND + 0.1	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

13. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc.
14. Output peak current is limited to 75% of its maximum value at given range.
15. Max. output peak current is twice the value of maximum average current at given range.
16. Memory programming limited to 100 cycles
17. The parametric characteristics of the circuit are not guaranteed outside the Parametric operating junction temperature range.
18. The circuit functionality is not guaranteed outside the Functional operating junction temperature range. Also please note that the device is verified on bench for operation up to 170 °C.
19. The exposed pad must be hard wired to GND pin in an application to ensure both electrical and thermal connection.
20. Temperature reported by internal temperature sensor.

Table 5. THERMAL RESISTANCE

Characteristic	Package	Symbol	Min	Typ	Max	Unit
Thermal Resistance Junction to Exposed Pad (Note 21)	TSSOP38 EP	Rthjp	−	5	−	°C/W

21. Includes also typical solder thickness under the Exposed Pad (EP).

Table 6. ELECTRICAL CHARACTERISTICS (All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40 °C; 150 °C), unless otherwise specified.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
CURRENT CONSUMPTION						
The VCC Current Consumption	I_VCC		−	14	20	mA
Leakage Current in OFF State (Note 22, 23, 24)	ILEAK_OFF	VCC = 0 V	−	−	10	μA
OSC16M: SYSTEM OSCILLATOR CLOCK						
Oscillator Output Frequency (Trimmed)	OSC_CLK	OSC_CAL[4:0] = 0	14.8	16	17.2	MHz
Oscillator Output Frequency (Untrimmed)	OSC_CLK_0	OSC_CAL[4:0] = 0, TRIMERR = 1	6	11	20	MHz
Oscillator Frequency Calibration Step	OSC_SCAL	Trimmed oscillator. Calibrated via OSC_CAL[4:0] SPI register.	40	100	160	kHz
Oscillator Duty Cycle	OSC_DUTY		40	50	60	%

Table 6. ELECTRICAL CHARACTERISTICS (All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40 °C; 150 °C), unless otherwise specified.) (continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
VINT: 3 V LOW VOLTAGE INTERNAL ANALOG AND DIGITAL SUPPLY						
The VINT Voltage @ VCC = 5.5 V	VINT_VCC5	Iload = 0 to 15 mA	3	3.15	3.3	V
The VINT Voltage @ VCC = 3.0 V	VINT_VCC3	Iload = 15 mA	2.8	−	−	V
VINT POR Threshold, VINT Rising	POR_R		2.5	2.6	2.7	V
VINT POR Threshold, VINT Falling	POR_F		2.4	−	2.6	V
VINT POR Hysteresis	POR_H		−	0.05	−	V
The POR Debounce Time (Both Edges)	POR_DEB		0.5	2	6	μs
VDRIVE: SUPPLY FOR BOOSTER MOSFET GATE DRIVE CIRCUIT AND BUCK LOW SIDE SWITCHES						
VDRV UV Detection Threshold	VDRV_UV7	VDRV_UV_THR[2:0]=111	4.2	4.4	4.6	V
	VDRV_UV6	VDRV_UV_THR[2:0]=110	3.9	4.1	4.3	
	VDRV_UV5	VDRV_UV_THR[2:0]=101	3.6	3.8	4.0	
	VDRV_UV4	VDRV_UV_THR[2:0]=100	3.3	3.5	3.7	
	VDRV_UV3	VDRV_UV_THR[2:0]=011	3.0	3.2	3.4	
	VDRV_UV2	VDRV_UV_THR[2:0]=010	2.8	2.9	3.0	
	VDRV_UV1	VDRV_UV_THR[2:0]=001	2.5	2.6	2.7	
	VDRV_UV0	VDRV_UV_THR[2:0]=000	−	0	−	
VDRV UV Detection Release Threshold	VDRV_NOUV7	VDRV_UV_THR[2:0]=111	4.3	4.5	4.7	V
	VDRV_NOUV6	VDRV_UV_THR[2:0]=110	3.95	4.2	4.4	
	VDRV_NOUV5	VDRV_UV_THR[2:0]=101	3.65	3.9	4.1	
	VDRV_NOUV4	VDRV_UV_THR[2:0]=100	3.25	3.6	3.8	
	VDRV_NOUV3	VDRV_UV_THR[2:0]=011	3.05	3.3	3.5	
	VDRV_NOUV2	VDRV_UV_THR[2:0]=010	2.85	3.0	3.1	
	VDRV_NOUV1	VDRV_UV_THR[2:0]=001	2.55	2.7	2.8	
VDRV UV Voltage Threshold Hysteresis	VDRV_UVHyst		50		200	mV
VDRV UV Detection Delay	VDRV_UVDL	Debouncer at falling edge of VDRV voltage	−	8	−	μs
ADC FOR MEASURING VIN1, VIN2, VBST, VCC, VDRV, VINT, VLED1, VLED2, TEMP						
ADC Resolution	ADC_RES		−	9	−	Bits
Integral Nonlinearity (INL)	ADC_INL	Best fitting straight line method. Between 5% and 95% of input full scale voltage (Note 25)	−2	−	2	LSB
Differential Nonlinearity (DNL)	ADC_DNL	Best fitting straight line method. Between 5% and 95% of input full scale voltage (Note 25)	−2	−	2	LSB
ADC Offset at Output	ADC_OFFS	Best fitting straight line method. Between 5% and 95% of input full scale voltage (Note 25)	−5	−	5	LSB
ADC Gain Error at Output	ADC_GAIN_ERR	Best fitting straight line method. Between 5% and 95% of input full scale voltage (Note 25)	−5	−	5	%
Time for 1 SAR Conversion	ADC_CONV		−	7.5	−	μs
ADC Full Scale for VIN Measurement	ADC_VIN		66.5	70	73.5	V
ADC Full Scale for VBST Measurement	ADC_VBST		66.5	70	73.5	V
ADC Full Scale for VLEDx Measurement	ADC_VLED_L	The VLED range code is “0”	66.5	70	73.5	V
	ADC_VLED_H	The VLED range code is “1”	33.25	35	36.75	V
ADC Full Scale for VCC Measurement	ADC_VCC		5.86	6.18	6.5	V
ADC Full Scale for VDRV Measurement	ADC_VDRV	(Note 25)	5.86	6.18	6.5	V

Table 6. ELECTRICAL CHARACTERISTICS (All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40 °C; 150 °C), unless otherwise specified.) (continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
ADC FOR MEASURING VIN1, VIN2, VBST, VCC, VDRV, VINT, VLED1, VLED2, TEMP						
ADC Full Scale for VINT Measurement	ADC_VINT		4.6	4.8	5.15	V
Temperature Measurement Range	TMP_RG	Typical values	−60	−	195	°C
Temperature Measurement Resolution	TMP_RES	Typical values	−	1.05	−	°C/LSB
VLED Input Impedance	ADC_VLEDR		0.3	0.6	1.2	MΩ
TSD Threshold Level	TSD	Guaranteed by trimming	160	170	180	°C
BUCK Driver Local TSD Level	BUCKTSD	Guaranteed by trimming	180	190	200	°C
BOOST CONTROLLER − VOLTAGE REGULATION PARAMETERS						
Booster Overvoltage Shutdown ΔV to the Reg. Level (Note 26)	BST_OV_07	BST_OV_SD[2:0] = 111	5.3	5.7	6.3	V
	BST_OV_06	BST_OV_SD[2:0] = 110	4.3	4.8	5.3	
	BST_OV_05	BST_OV_SD[2:0] = 101	3.5	3.9	4.3	
	BST_OV_04	BST_OV_SD[2:0] = 100	2.7	3	3.3	
	BST_OV_03	BST_OV_SD[2:0] = 011	2.2	2.5	2.8	
	BST_OV_02	BST_OV_SD[2:0] = 010	1.7	2	2.3	
	BST_OV_01	BST_OV_SD[2:0] = 001	1.2	1.5	1.8	
	BST_OV_00	BST_OV_SD[2:0] = 000	0.8	1	1.2	
Booster Overvoltage Re-activation	BST_RA3	BST_OV_REACT[1:0] = 11	−1.9	−1.5	−1.1	V
	BST_RA2	BST_OV_REACT[1:0] = 10	−1.3	−1	−0.7	
	BST_RA1	BST_OV_REACT[1:0] = 01	−0.65	−0.5	−0.35	
	BST_RA0	BST_OV_REACT[1:0] = 00	−0.15	0	0.15	
Booster Voltage Feedback Fail Detection Threshold	BST_FBFAIL		1.15	1.21	1.27	V
Booster Regulation Level	BST_REG_127		−	62	−	V
	BST_REG_000		−	9.7	−	
Booster Regulation Level Increase per Code	ΔBST_REG	Linear increase, 7 bits	−	0.412	−	V
Booster Regulation Level Error	BST_REGERRH	VBST_NOM > 25 V	−3		3	%
	BST_REGERRL	VBST_NOM < 25 V	−4		4	%
Booster Error Amplifier (EA) Trans-conductance Gain G_m Seen from VBST	EA_GM3	VBST = VBST_REG ±1 V 0.5 V < VCOMP < 2.1 V BST_OTA_GAIN[1:0] = 11	42	60	78	μS
	EA_GM2	BST_OTA_GAIN[1:0] = 10	21	30	39	
	EA_GM1	BST_OTA_GAIN[1:0] = 01	10	15	20	
Error Amplifier High Impedance State	EA_GM0	BST_OTA_GAIN[1:0] = 00	−	0	−	μS
EA Max Output Current (Positive/Sink)	EA_IOUT3P	BST_OTA_GAIN[1:0] = 11	100	130	160	μA
	EA_IOUT2P	BST_OTA_GAIN[1:0] = 10	50	65	80	
	EA_IOUT1P	BST_OTA_GAIN[1:0] = 01	25	32.5	40	
EA Min Output Current (Negative/ Source)	EA_IOUTN		−900	−530	−300	μA
EA Equivalent Output Resistance	EA_BLR	VCOMP = 0.5 V	0.8	2.4	5	MΩ
EA Max Output Leakage Current in Hi Impedance State	EA_BLI_P	VCC present, VCOMP = 2.1 V	0.15	0.4	1	μA
	EA_BLI	VCC = 0 V, VCOMP = 2.1 V	0.5	1.7	5	
COMP Short Circuit Current	EA_INLIM	BST_OTA_GAIN[1:0] = 11 VBST = 0 V, VCOMP = 0 V	−1.5	−	−	mA
EA Low Clamp Voltage	COMP_CLL		−	−	0.45	V
EA Low Clamp Current Limitation	COMP_CLL_ILIM		−0.5	−	−0.1	mA

Table 6. ELECTRICAL CHARACTERISTICS (All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40 °C; 150 °C), unless otherwise specified.) (continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
BOOST CONTROLLER − VOLTAGE REGULATION PARAMETERS						
EA High Clamp Offset Voltage	COMP_CLH	Current limitation mode	60	−	300	mV
Booster Skip Cycle for Low Currents (Booster Disabled for Lower VCOMP)	BST_SKCL0	BST_SKCL[1:0] = 00	0.50	0.55	0.60	V
	BST_SKCL1	BST_SKCL[1:0] = 01	0.56	0.6	0.64	
	BST_SKCL2	BST_SKCL[1:0] = 10	0.66	0.7	0.75	
	BST_SKCL3	BST_SKCL[1:0] = 11	0.75	0.8	0.85	
Accuracy of Timer for BST_TOFF_MIN and BST_TON_MIN	BST_OSC_ERR		−15	−	15	%
BOOST CONTROLLER − CURRENT REGULATION PARAMETERS						
COMP Buffer Offset	BST_CBUF_OFFS		−20	−	20	mV
COMP Buffer Step	BST_CBUF_STEP		6	10	14	mV
Division Factor of VCOMP Voltage Towards the Current Comparator Input	COMP_DIV0	BST_COMP_DIV[2:0] = 000	1.88	2	2.12	
	COMP_DIV1	BST_COMP_DIV[2:0] = 001	2.63	2.8	2.96	
	COMP_DIV2	BST_COMP_DIV[2:0] = 010	3.72	4	4.19	
	COMP_DIV3	BST_COMP_DIV[2:0] = 011	5.23	5.7	5.90	
	COMP_DIV4	BST_COMP_DIV[2:0] = 100	7.39	8	8.34	
	COMP_DIV5	BST_COMP_DIV[2:0] = 101	10.46	11.3	11.79	
	COMP_DIV6	BST_COMP_DIV[2:0] = 110	14.74	16	16.63	
	COMP_DIV7	BST_COMP_DIV[2:0] = 111	20.82	22.6	23.47	
Voltage Shift (Offset) on VCOMP on Current Comparator Input	COMP_VSF		0.46	0.5	0.54	V
Current Comparator for Imax Detection	BST_VLIMTH255	BST_VLIM_THR[7:0] = 11111111	570	600	630	mV
	BST_VLIMTH0	BST_VLIM_THR[7:0] = 00000000	−4	2	8	
Imax Detection Increase per Code	ΔBST_VLIMTH	Linear increase, 8 bits		2.35	−	mV
Current Comparator for Imax Detection Error	BST_VLIMTHERR		−5 & −4	−	5 & 8	% & mV
Current Regulation Comparator Offset Voltage	BST_OFFS		−10	−	10	mV
	BST_SLCTR7	BST_SLP_CTRL[2:0] = 111	1035	1210	1355	mV/µs
	BST_SLCTR6	BST_SLP_CTRL[2:0] = 110	695	790	885	
	BST_SLCTR5	BST_SLP_CTRL[2:0] = 101	430	500	570	
	BST_SLCTR4	BST_SLP_CTRL[2:0] = 100	306	360	414	
	BST_SLCTR3	BST_SLP_CTRL[2:0] = 011	187	220	253	
	BST_SLCTR2	BST_SLP_CTRL[2:0] = 010	120	150	180	
	BST_SLCTR1	BST_SLP_CTRL[2:0] = 001	57	75	93	
	BST_SLCTR0	BST_SLP_CTRL[2:0] = 000	−	0	−	
BOOST CONTROLLER − MOSFET GATE DRIVER						
High-side Switch Impedance	FETDRV_RONH		−	4	7	Ω
Low-side Switch Impedance	FETDRV_RONL		−	4	7	Ω
Pull-down Resistor	FETDRV_RPD		4	10	18	kΩ
BUCK REGULATOR − HIGH SIDE SWITCH AND CURRENT REGULATION						
On Resistance, Range 1	RON1	At room-temperature	−	−	2.00	Ω
On Resistance at Hot, Range 1	RON1H	At Tj = 150 °C	−	3.44	4.20	Ω
On Resistance, Range 2	RON2	At room-temperature	−	−	1.00	Ω

Table 6. ELECTRICAL CHARACTERISTICS (All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40 °C; 150 °C), unless otherwise specified.) (continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
BUCK REGULATOR − HIGH SIDE SWITCH AND CURRENT REGULATION						
On Resistance at Hot, Range 2	RON2H	At Tj = 150 °C	−	1.72	2.10	Ω
On Resistance, Range 3	RON3	At room-temperature	−	−	0.50	Ω
On Resistance at Hot, Range 3	RON3H	At Tj = 150 °C	−	0.86	1.05	Ω
On Resistance, Range 4	RON4	At room-temperature	−	−	0.26	Ω
On Resistance at Hot, Range 4	RON4H	At Tj = 150 °C	−	0.43	0.53	Ω
Avg. Current Full Scale, Range 1	IAVG1_H	BUCKx_IRNG[1:0] = 0, BUCKx_IAVG[7:0] = 511	−	200	−	mA
Avg. Current Full Scale, Range 2	IAVG2_H	BUCKx_IRNG[1:0] = 0, BUCKx_IAVG[7:0] = 511	−	400	−	mA
Avg. Current Full Scale, Range 3	IAVG3_H	BUCKx_IRNG[1:0] = 0, BUCKx_IAVG[7:0] = 511	−	800	−	mA
Avg. Current Full Scale, Range 4	IAVG4_H	BUCKx_IRNG[1:0] = 0, BUCKx_IAVG[7:0] = 511	−	1600	−	mA
Avg. and Rip. Current Sense Threshold Increase per Code, Range 1	D_IAVG1	Linear increase	−	0.78	−	mA
Avg. and Rip. Current Sense Threshold Increase per Code, Range 2	D_IAVG2	Linear increase	−	1.57	−	mA
Avg. and Rip. Current Sense Threshold Increase per Code, Range 3	D_IAVG3	Linear increase	−	3.12	−	mA
Avg. and Rip. Current Sense Threshold Increase per Code, Range 4	D_IAVG4	Linear increase	−	6.26	−	mA
Current Threshold Accuracy in 50% FS to 100% FS (Note 27)	IERR		−3	−	3	%
Current Threshold Accuracy in 12.5% FS to 50% FS (Note 27)	IERR_LRNG		−15	−	15	%
Average Current Accuracy in Application in 50% FS to 100% FS in CCM (Note 28)	IERR_APP		−5	−	5	%
The Rise Edge Slope, Normal Mode	TRISE		−	3	−	V/ns
Falling Slope	TFALL	When the driver steers the slope	−	6	−	V/ns
BUCK REGULATOR − SYNCHRONOUS RECTIFIER SWITCH						
On Resistance of the Switch MOS	SRRON	Typ. at room-temperature	−	0.17	−	Ω
	SRRONH	Max. at hot	−	−	0.35	
BUCK REGULATOR − TOFF GENERATOR						
Minimum Possible Vcoil-Toff Setting (Note 29)	TOFFMIN	Valid is the one representing a longer Toff time	−	−	5	µs·V
Minimum Possible Vcoil-Toff Setting (Note 29)	TOFFABSMIN	Valid is the one representing a longer Toff time	−	−	100	ns
Maximum Possible Vcoil-Toff Setting (Note 29)	TOFFMAX		50	−	−	µs·V
Relative Vcoil-Toff Adjustment Step	TOFFSTEP	Relative step in Toff adjustment, defined as (Toff(n+1) − Toff(n))/Toff(n)	−	$\sqrt[16]{2}-1$	−	
Relative Error of the Vcoil-Toff Setting (Note 30)	TOFFERRREL		−25	−	+25	%
BUCK REGULATOR − TIMING COMPARATOR FOR AVERAGE CURRENT DETECTION						
Timing Ratio Error (Note 31)	TONCMPERR	For on times from 100 ns to 50 µs	−1	−	2.5	%
Timing Ratio T2/T1 for Time Out Comparator	TONTOUT	For on times > 0.3 µs	1.05	1.25	1.5	

Table 6. ELECTRICAL CHARACTERISTICS (All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40 °C; 150 °C), unless otherwise specified.) (continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
BUCK REGULATOR − COMPARATORS						
VLED_LOW Comparator (Detection of Shorted LED Output)						
Detection Level of VLED to Be Too Low	VLEDLOW		0.8	1.0	1.2	V
VLED_LOW Hysteresis	VLEDLOW_H		−	50	−	mV
VLED_LOW Detection Filter Time	VLEDLOW_F		0.1	−	2	μs
LEDCTRL Comparator for Buck Voltage Mode						
LEDCTRL Comparator Threshold	LCCMP_THR	Rising edge at LEDCTRLx pin	1.16	1.21	1.26	V
LEDCTRL Comparator Hysteresis	LCCMP_HYST		−	−	5	mV
LEDCTRL Comparator Delay	LCCMP_DEL		−	−	30	ns
BUCK REGULATOR − CBT RECHARGE CIRCUIT						
Startup Precharge Current	IPRECH		0.1	−	1	mA
TON Termination (Forced Recharge) Threshold	VRECH	Shall exhibit no hysteresis, UVS signal	2.4	2.7	2.9	V
Under-voltage Monitor Threshold −V(CBT,BCK) Rising	VPORON		3	3.3	3.55	V
Under-voltage Monitor Threshold −V(CBT,BCK) Falling	VPOROFF		2.2	−	2.7	V
Over-voltage Monitor Threshold	CBTOV		3.65	−	−	V
Delay of the PORB Release after PD	TDUVRES		5	−	−	μs
Regulated Voltage Level	VVBT	VDRV > 4 V, Toff > 400 ns, Ton = 10 μs	3	3.3	3.6	V
Current Limitation	VVBTILIM	VDRV > 4.5 V, VCBT = 2.2 V	70	−	200	mA
5 V TOLERANT DIGITAL INPUTS (SCLK, CSB, SDI, LEDCTRL1, LEDCTRL2, BSTSYNC)						
High Level Input Voltage	DI5_VINH	VINT = 2.7 V to 3.6 V	2	−	−	V
Low Level Input Voltage	DI5_VINL	VINT = 2.7 V to 3.6 V	−	−	0.8	V
Input Threshold Hysteresis	DI5_VINHyst		0.1	−	0.9	V
The Pull-up/down Resistance (Note 32)	DI5_RP		40	100	180	kΩ
Input Leakage Current	DI5_ILIN	Pull resistance disabled	−1		1	μA
LEDCTRLx PWM Propagation Delay	DI5_SWDEL	Activation time of the BUCKx switch from the LEDCTRLx pin	−	4	−	μs
LEDCTRLx Sampling Resolution	DI5_SR	Resynchronization 1−2 clock periods	−	62	−	ns
5 V DIGITAL OUTPUT (SDO)						
High Level Output Voltage	DO5_VOH	Iout = −2 mA (current flows into the pin)	VCC − 0.5	−	VCC	V
Low Level Output Voltage	DO5_VOL	Iout = 2 mA	0	−	0.5	V
Output Delay; Both Edges	DO5_DEL	I = −10 mA or Cload = 50 pF	−	7	30	ns
SPI INTERFACE						
CSB Setup Time	csb_setup	CSB setup time before first SCLK rising edge	375	−	−	ns
CSB Hold Time	csb_hold	CSB hold time after last SCLK rising edge	150	−	−	ns
CSB High Time	csb_gap	Gap between two CSB low pulses	500	−	−	ns
SCLK Clock Period	sclk_per		250	−	−	ns
SCLK Low Time	sclk_lo		0.4 x sclk_per	−	0.6 x sclk_per	ns

Table 6. ELECTRICAL CHARACTERISTICS (All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40 °C; 150 °C), unless otherwise specified.) (continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
SPI INTERFACE						
SCLK High Time	sclk_hi		0.4 x sclk_per	−	0.6 x sclk_per	ns
SDI Setup Time before Each SCLK Rising Edge	sdi_setup		45	−	−	ns
SDI Hold Time after Each SCLK Rising Edge	sdi_hold		45	−	−	ns
SDO Hold Time	sdo_hold	Depends on parasitic capacitance of SDO line	0	−	62.5 + Max (DO5_DEL)	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

22. Sum of currents from VDRV, VINx, VBST, IBSTSNSxP, SDI, SCLK, CSB, LEDCTRLx and BSTSYNC pin.
23. Conditions: V(VCC) = V(LEDCTRLx) = V(IBSTSNSxN) = 0 V; V(VINx) = V(VBST) = V(IBSTSNSxP) = 16 V; V(VDRV) = V(SDI) = V(SCLK) = V(CSB) = V(BSTSYNC) = 5 V.
24. Temperature range −40 °C to 85 °C.
25. For VDRV minimum measured voltage is 2.5 V
26. User has to take care that sum of selected Booster regulation level BST_REG and Booster overvoltage shutdown BST_OV including accuracy and overshoots does not to exceed Absolute Maximum ratings 66 V for Buck Input voltage VINx and Boost voltage feedback input VBST.
27. Accuracy calculated based on calibration data and IDAC measurement (IDAC is the source of nonlinearities). This parameter only represents precision of current comparator (ICMP) threshold across IDAC code.

    Maximum possible system IAVG error with ideal coil is $\sqrt{IERR^2 + TONCMPERR^2}$. Valid for CCM only.
28. The average current accuracy in application is tested with: L_{BUCK} = 47 μH (Panasonic ETQP4M470YFN), C_{BUCK} = 1 μF (generic ceramic capacitor X7R, 100V, 1 μF) and f_{BUCK} = 2 MHz for Buck current ranges 1 and 2 and f_{BUCK} = 400 kHz for Buck current ranges 3 and 4.
29. Limits of the Toff adjustment (with respect to the calibration procedure), which are possible to reach and where the functionality is guaranteed. Setting beyond these limits may lead to an erratic functionality and so such setting is not allowed.
30. For any given condition and setting, valid is the one leading to the widest tolerance. VLED > 2 V.
31. For any condition, the limit yielding wider tolerance applies. For definition of Time offset and Timing ratio error please see Average Current Accuracy chapter.
32. Pull-down resistance for LEDCTRLx and BSTSYNC, pull-up resistance to VINT for CSB and LEDCTRLx. LEDCTRL1 and LEDCTRL2 have pull-down or pull-up resistor connected according to LEDCTRLx_MD[1:0] SPI register. Valid only in active mode when VCC supply is present.

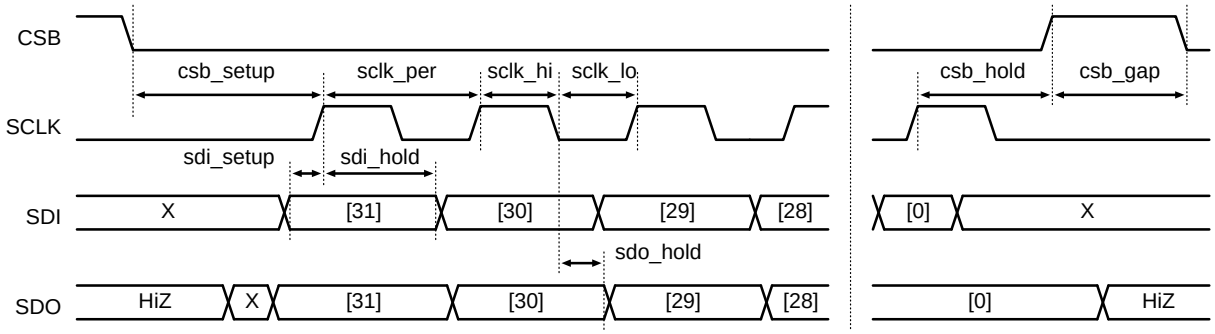


Figure 10. SPI Communication Timing

TYPICAL CHARACTERISTICS

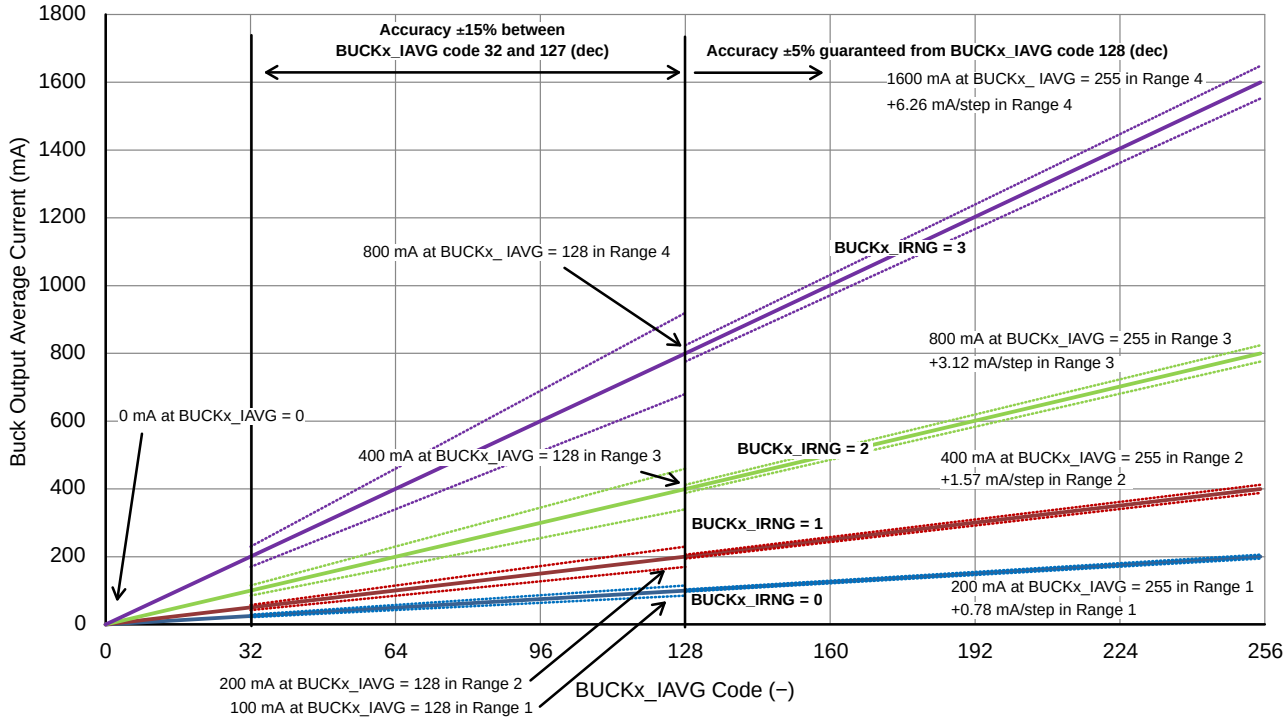


Figure 11. Buck Average Current vs. BUCKx_IRNG Range and BUCKx_IAVG Code

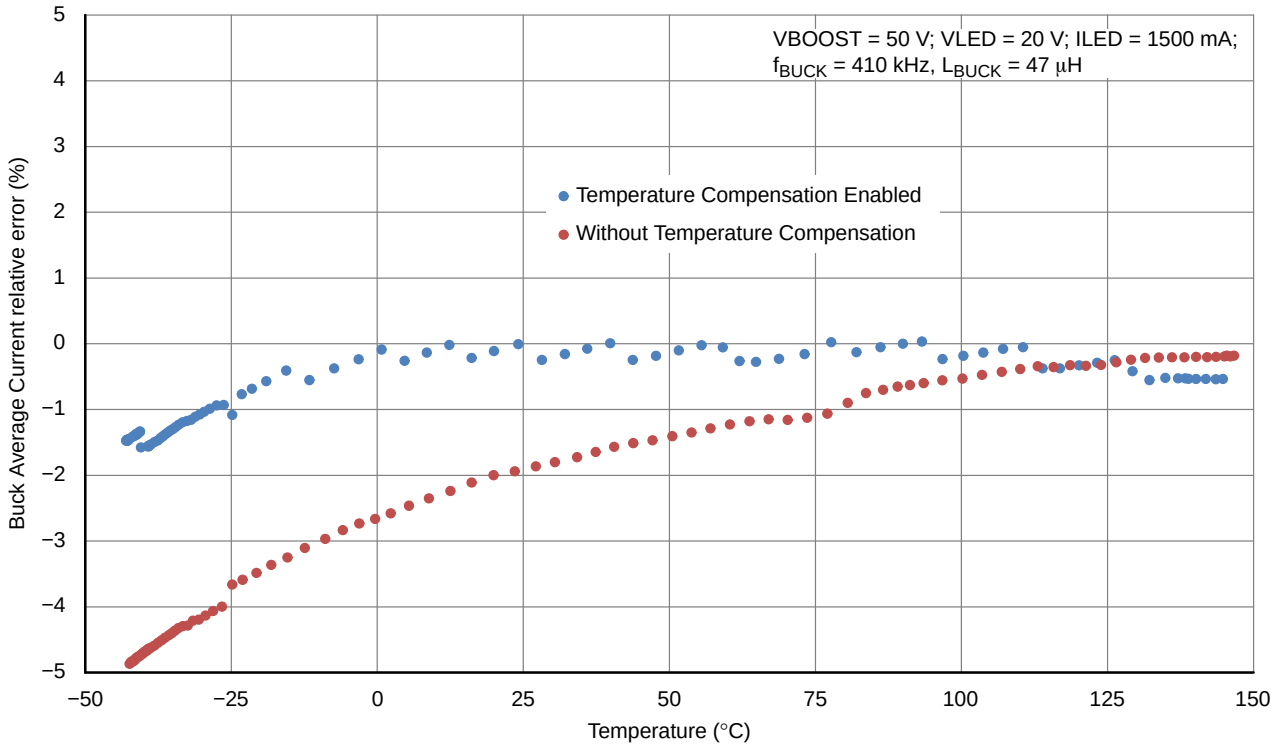


Figure 12. Typical Buck Average Current Accuracy and Stability over Temperature in CCM

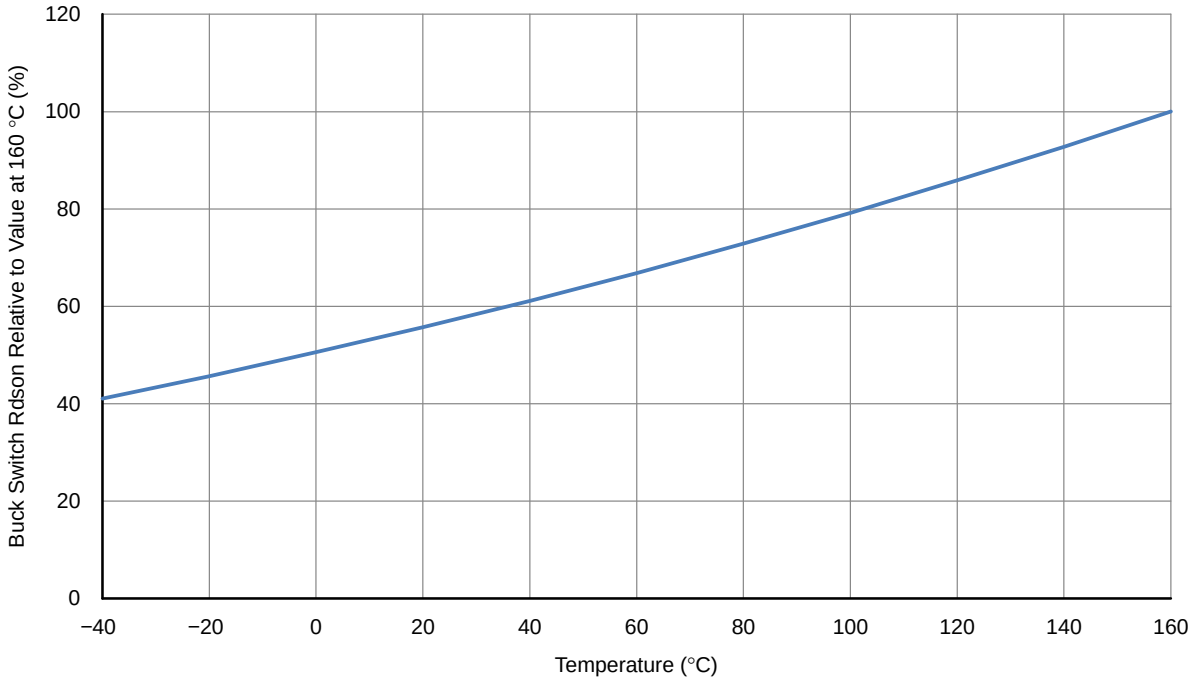


Figure 13. Typical Temperature Behavior of Buck HS Switch Rdson Relative to the Value at 160 °C

DETAILED OPERATING DESCRIPTION

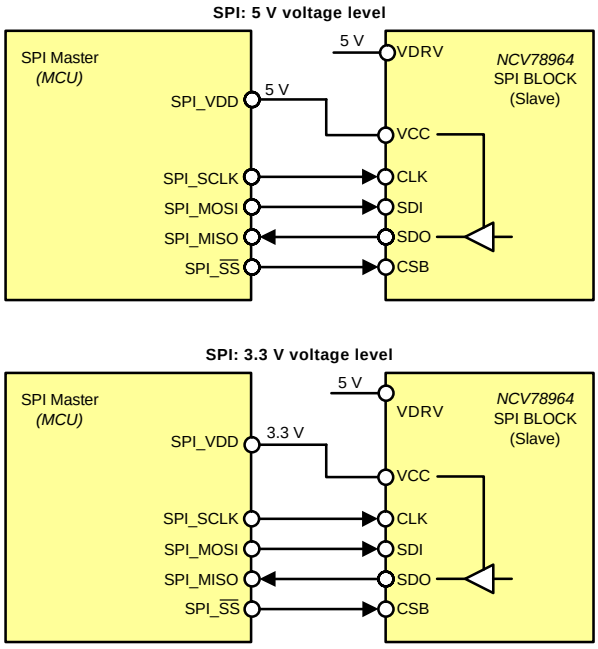


Figure 14. SPI Connection Scenarios and Power Supply Strategy

SUPPLY CONCEPT IN GENERAL

Two types of voltages have to be brought to the NCV78964 chip − low voltage VCC and VDRV supply and high voltages to each VINx for providing energy to the Buck regulators. More detailed description follows.

VDRV Supply

The VDRV supply voltage represents the power for:

- Booster pre-driver block which generates the VGATE, used to switch external booster MOSFET,
- Buck internal synchronous rectifier switches,
- Buck bootstrap capacitors (C_BTx).

This supply is separated from the VCC to limit the noise on sensitive circuitries. 5 V is required for reliable operation over wide operating conditions.

VDRV Undervoltage Lockout safety mechanism monitors sufficient voltage for booster MOSFETs and protects them by switching off the booster when VDRV voltage is too low. Detection level is set by VDRV_UV_THR[2:0] register (see Table 6 “VDRIVE: SUPPLY FOR BOOSTER MOSFET GATE DRIVE CIRCUIT AND BUCK LOW SIDE SWITCHES” for more details). When VDRV_UV_THR[2:0] = 0, the function is disabled. VDRV_UV (latched, reg. 0x36) flag indicates that protection has acted.

VCC Supply

The VCC supply voltage represents power for the internal supply VINT. It also defines interface voltage with the microcontroller on push-pull SDO pin and shall be selected accordingly (3.3 or 5 V).

By disconnecting the VCC supply, the Low power mode can be entered. In typically setup small external switch can be placed into VCC supply line.

VINT Supply

The internal regulator generates the main low voltage digital and analog supply VINT for the chip.

The Power-On-Reset circuit (POR) monitors the VINT voltage to control the out-of-reset and reset entering state. At power-up, the chip will exit from reset state when VINT > POR_R. No SPI communication is possible in reset state.

VINx Supply

The VIN1 and VIN2 supply voltages are the main high voltage supply for the Buck outputs. The voltage is supposed to be provided either by NCV78964 Booster circuit or by battery voltage in the application. Each buck input can be supplied from different voltage supply if needed. All input pins VINx have to be connected by low impedance track to ensure proper buck performance.

Internal Clock Generation

An internal RC clock generator is used to run all the digital functions in the chip. The clock is trimmed in the factory prior to delivery. Its accuracy is guaranteed under full operating conditions and is independent from external component selection. All timings depend on OSC_CLK accuracy (refer to Table 6 “OSC16M: SYSTEM OSCILLATOR CLOCK” for details).

In the application, the oscillator can be further calibrated via OSC_CAL[4:0] SPI register.

For this purpose the CSB_DUR[19:0] register is introduced, which allows to measure duration of CSB signal, precisely generated by MCU, and by this way indirectly check the oscillator frequency.

ADC

General

The built-in analog to digital converter (ADC) is an 9-bit capacitor based successive approximation register (SAR). This embedded peripheral can be used to provide the following measurements to the external Micro Controller Unit (MCU):

- VCC voltage: sampled at the VCC pin;
- VDRV voltage: sampled at the VDRV pin;
- VINT voltage;
- VTEMP measurement (chip temperature);
- VBST booster voltage: sampled at VBST pin;
- VINx [1;2] voltages: sampled at the VINx pins;
- VLEDx [1;2] voltages: measured during on and off state;
- VLEDxON [1;2] voltages: measured during on state (just before LEDCTRLx falling edge);

- VLEDxOFF [1;2] voltages: measured during off state (just before LEDCTRLx rising edge).

The internal NCV78964 ADC state machine samples all the above channels automatically, taking care for setting the analog MUX and storing the converted values in memory. The external MCU can readout all ADC measured values via the SPI interface, in order to take application specific decisions. Please note that none of the MCU SPI commands interfere with the internal ADC state machine sample and conversion operations: the MCU will always get the last available data at the moment of the register read.

Basic measurement cycle consists from the measurements in shown order:

VDRV → VIN1 → VLED1 → VCC → VIN2 → VLED2 → VINT → VIN3 → VBST → VTEMP

VLEDxON measurement request is triggered when BUCKx_EN is 1 and LEDCTRLx falling edge (or corresponding internal signal when internal pwm dimming is used) is detected.

VLEDxOFF measurement request is triggered when BUCKx_EN is 1 and LEDCTRLx rising edge (or corresponding internal signal when internal pwm dimming is used) is detected.

Current ADC measurement is interrupted when the request for measurement of VLEDxON/VLEDxOFF with higher priority than current measurement comes. VTEMP priority is used for priority comparison. After inserted VLEDxON/OFF measurement is finished, measurement cycle continuous at interrupted place.

After measurement of VLEDxON/OFF or VTEMP, priorities are updated in the following way:

- Every channel with higher priority than measured channel keeps its priority unchanged;
- Every channel with lower priority than measured channel increases its priority by 1;
- Measured channel have its priority set to the lowest.

After POR, measurement channel priorities are (from the highest to the lowest): LED1ON, LED1OFF, LED2ON, LED2OFF, VTEMP.

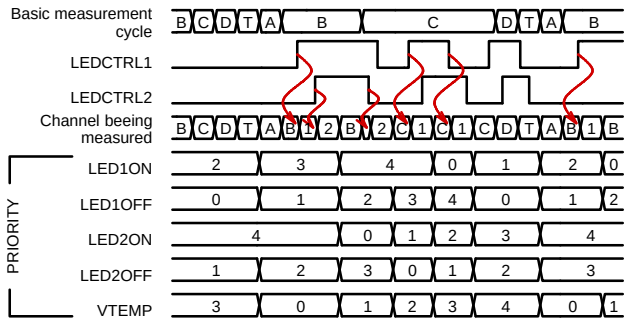


Figure 15. Measurement Priority Example

Supply Voltage ADC: V_{CC}

The supply voltage is sampled at VCC pin. The (9-bit) conversion ratio is 6.2/511 (V/dec) = 12.3 (mV/dec) typical. The converted value can be found in the SPI register VCC[8:0].

Supply Voltage ADC: V_{DRV}

The supply voltage is sampled at VDRV pin. The (9-bit) conversion ratio is 6.2/511 (V/dec) = 12.3 (mV/dec) typical. The converted value can be found in the SPI register VDRV[8:0].

Logic Supply Voltage ADC: V_{INT}

The logic supply voltage is sampled internaly. The (9-bit) conversion ratio is 4.8/511 (V/dec) = 9.4 (mV/dec) typical. The converted value can be found in the SPI register VINT[8:0].

Booster Voltage ADC: V_{BST}

The booster voltage is sampled at VBST pin. The (9-bit) conversion ratio is 70/511 (V/dec) = 0.137 (V/dec) typical. The converted value can be found in the SPI register VBST[8:0]. There is internal RC filter consisting of 10 MΩ and 5 pF on VBST pin filtering out the booster voltage ripple. This measurement can be used by the MCU for diagnostics and booster control loop monitoring.

Buck Input Voltages ADC: V_{IN1}, V_{IN2}

These measurements refer to the buck input voltages at the VINx [1;2] pins, with an 9-bit conversion ratio of 70/511 (V/dec) = 0.137 (V/dec) typical, with conversion results inside the SPI registers VINx[8:0].

Device Temperature ADC: V_{TEMP}

By means of the VTEMP measurement, the MCU can monitor the device junction temperature (T_J) over time. The conversion formula is:

$$T_J = 1.05 \cdot (VTEMP[8:0] - 248) \quad \text{(eq. 1)}$$

VTEMP[8:0] is the value read out directly from the related SPI register. The value is also used internally by the device for the *thermal warning* and *thermal shutdown* functions. More details on these diagnostic flags can be found in the dedicated sections in this document.

LED String Voltages ADC: V_{LEDx}, V_{LEDxON}, $V_{LEDxOFF}$

The voltage at the pins VLEDx [1;2] is measured. There are 2 ranges available, that can be selected by means of VLEDx_RNG register, to obtain higher resolution for LED voltage measurement.

Conversion ratios in dependency on selected range are:

0x0: 70/511 (V/dec) = 137.0 (mV/dec);
0x1: 35/511 (V/dec) = 68.5 (mV/dec);

This information, found in registers VLEDx[8:0], VLEDxON[8:0] and VLEDxOFF[8:0] can be used by the MCU to infer about the LED string status, for example, individual shorted LEDs.

BOOSTER REGULATOR

General

The NCV78964 features one two-phase booster stage for two high-current integrated buck current regulators. In addition, optional external buck regulators, belonging to other NCV78xxx devices, can be cascaded to the same boost voltage source.

The booster stage provides the required voltage source for the LED string voltages out of the available battery voltage. Moreover, it filters out the variations in the battery input current in case of LED strings PWM dimming.

For nominal loads, the boost controller will regulate in *continuous* mode of operation, thus maximizing the system power efficiency at the same time having the lowest possible input ripple current (with “continuous mode” it is meant that the supply current does not go to zero while the load is activated). Only in case of very low loads or low dimming duty cycle values, *discontinuous* mode can occur: this means the supply current can swing from zero when the load is off, to the required peak value when the load is on, while keeping the required input average current through the cycle. In such situations, the total efficiency ratio may be lower than the theoretical optimal. However, as also the total losses will at the same time be lower, there will be no impact on the thermal design.

On top of the cascaded configuration, the booster can be operated in *multi-phase* mode by combining more NCV78964 in the application. More details about the multiphase mode can be found in the dedicated section.

Booster Regulation Principles

The NCV78964 features *current-mode* voltage controller, which regulates the VBST line used by the buck converters. The regulation loop principle is shown in the following picture. The loop compares the reference voltage (BST_VSETPOINT[6:0]) with the actual measured voltage at the VBST pin, thus generating an error signal which is treated internally by the error trans-conductance amplifier (block A1). This amplifier transforms the error voltage into current by means of the trans-conductance gain Gm. The amplifier’s output current is then fed into the external compensation network impedance (A2), so that it originates a voltage at the COMP pin, this last used as a reference by the current control block (B).

The current controller regulates the duty cycle as a consequence of the COMP reference, the sensed inductor peak current via the external resistor RSENSE and the slope compensation used. The power converter (block C) represents the circuit formed by the boost converter externals (inductor, capacitors, MOSFET and forward diode). The load power (usually the LED power going via the buck converters) is applied to the converter. The controlled variable is the boost voltage, measured directly at the device VBST pin with a unity gain feedback (block F). The picture highlights as block G all the elements contained inside the device. The regulation parameters are flexibly set by a series of SPI commands. A detailed internal boost controller block diagram is presented in the next section.

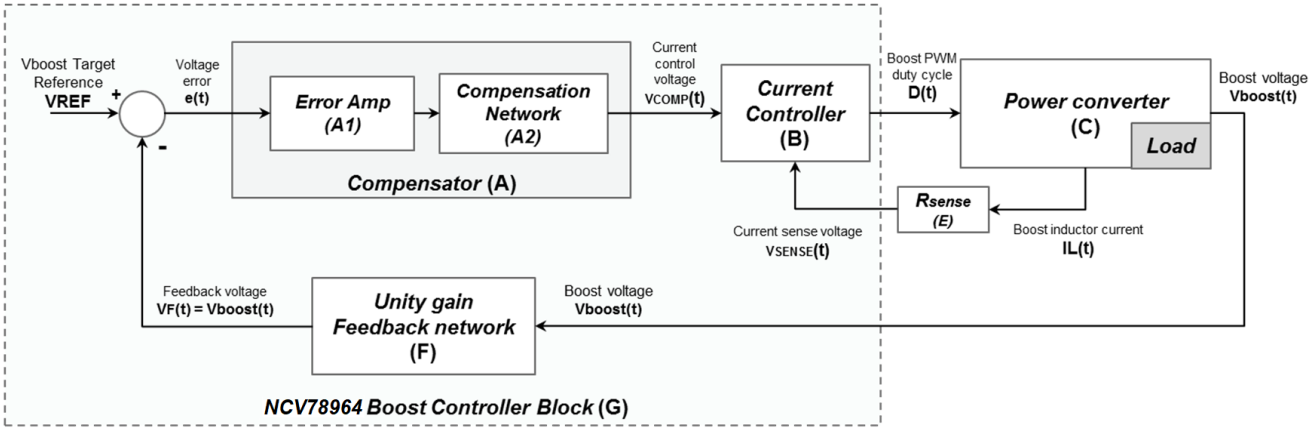


Figure 16. NCV78964 Boost Control Loop − Principle Block Diagram

Boost Controller Detailed Internal Block Diagram

A detailed NCV78964 boost controller block diagram is provided in this section. The main signals involved are indicated, with a particular highlight on the SPI programmable parameters.

The blocks referring to the principle block diagram are also indicated. In addition, the protection specific blocks can be found (see dedicated sections for details).

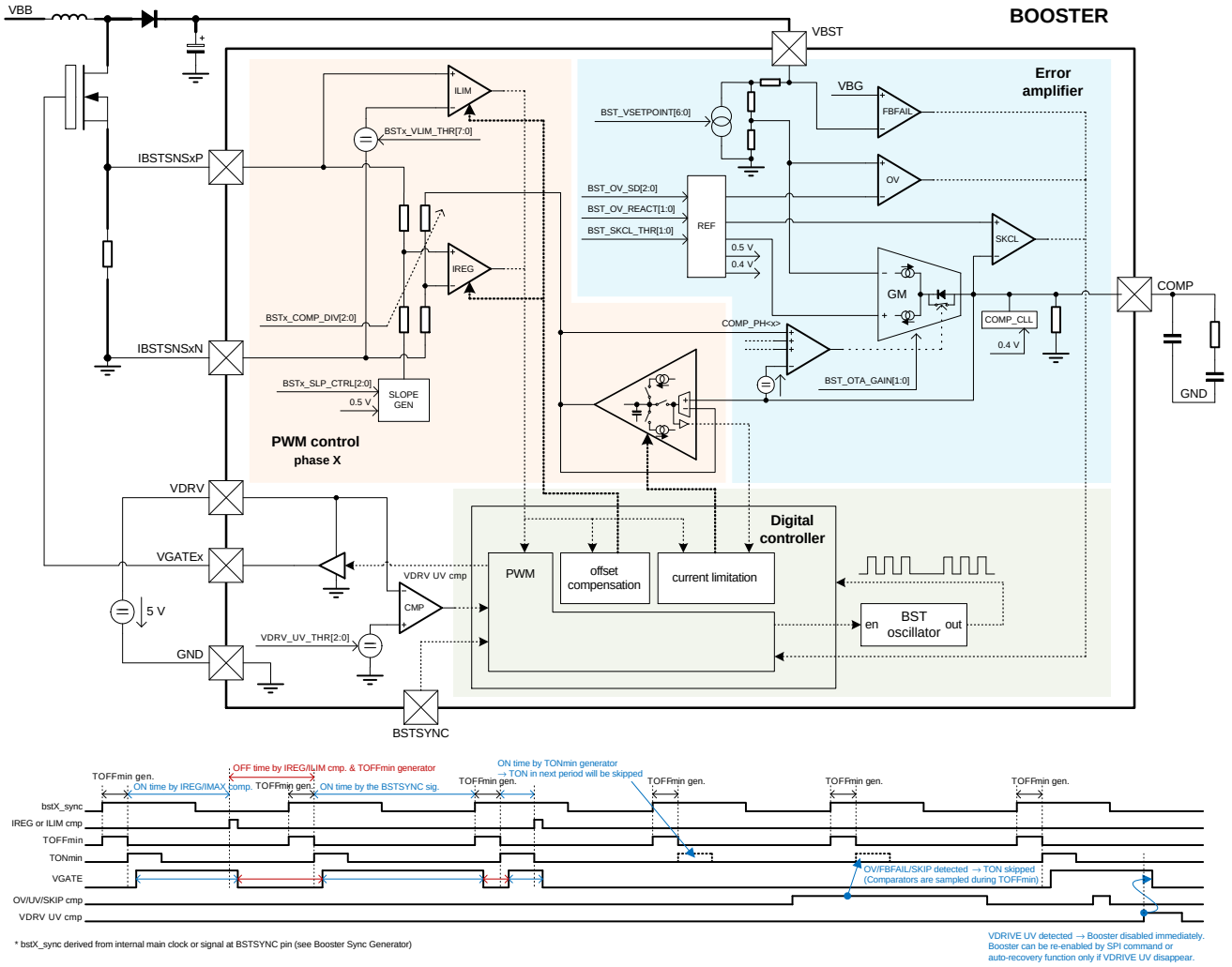


Figure 17. Boost Controller Internal Block Diagram

Booster Regulator Setpoint (BST_VSETPOINT)

The booster voltage VBST is regulated around the target programmable by the 7-bit SPI setting BST_VSETPOINT[6:0], ranging from a minimum of 9.7 V to a maximum of typical 62 V (please refer to Table 6 “BOOST CONTROLLER − VOLTAGE REGULATION PARAMETERS” for details) according to the following equation:

$$V_{BST\_NOM} = 9.7 + BST\_VSETPOINT[6:0] \times \left(\frac{52.3}{123}\right) (V) \quad \text{(eq. 2)}$$

Due to the step-up only characteristic of any boost converter, the boost voltage cannot obviously be lower than the supply battery voltage provided. Therefore a target of 9.7 V would be used only for systems that require the activation of the booster in case of battery drops below the nominal level. At power-up, the booster is disabled and the setpoint is per default the minimum (all zeroes).

Booster Overvoltage Shutdown Protection

An integrated comparator monitors VBST in order to protect the external booster components from overvoltage. When the voltage rises above the threshold defined by the sum of the booster voltage setpoint (BST_VSETPOINT[6:0]) and the overvoltage shutdown value (BST_OV_SD[2:0]), the MOSFET gate is switched-off at least for the current PWM cycle and at the same time, the boost overvoltage flag in the status register will be set (BST_OV = ‘1’), together with the BSTx_RUNNING flags equal to zero. The PWM runs again as from the moment the VBST will fall below the reactivation hysteresis defined by the BST_OV_REACT[1:0] SPI

parameter. Therefore, depending on the voltage drop and the PWM frequency, it might be that more than one cycle will be skipped. A graphical interpretation of the protection levels is given in the figure below.

User has to take care that sum of selected Booster regulation level BST_REG and Booster overvoltage shutdown BST_OV including accuracy and overshoots does not to exceed Absolute Maximum ratings 66 V for Buck Input voltage VINx and Boost voltage feedback input VBST. For highest settings of Booster regulation level BST_REG, the lowest settings of Booster overvoltage shutdown threshold BST_OV should be selected.

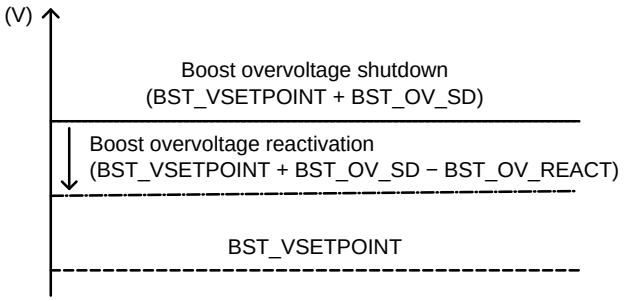


Figure 18. Booster Voltage Protection Levels with Respect to the Setpoint

After POR, the BST_OV flag may be set at first read out. Please note that the booster overvoltage detection is also active when Booster is OFF (booster disabled by SPI related bit). Please note that the tolerances of the booster setpoint level and the booster overvoltage and reactivation are given in Table 6 “BOOST CONTROLLER − VOLTAGE REGULATION PARAMETERS”.

Booster Current Regulation Loop

The peak-current level of the booster is set by the voltage of the compensation pin COMP, which is output of the trans-conductance error amplifier, “block B” of Figure 16. This reference voltage is fed to the current comparator via a divider (divider ratio of which can be set by register BSTx_COMP_DIV[2:0] for each phase independently, see Table 6 “BOOST CONTROLLER − CURRENT REGULATION PARAMETERS” for more details). The comparator compares this reference voltage with voltage VSENSE sensed on the external sense resistor RSENSE or over the booster MOSFET, connected to the pins IBSTSNSxP and IBSTSNSxN. The sense voltage is created by the booster inductor coil current when the MOSFET is switched on and is summed up to an additional offset of +0.5 V (see COMP_VSF in Table 6 “BOOST CONTROLLER − CURRENT REGULATION PARAMETERS”) and on top of that, a slope compensation voltage ramp is added. The slope compensation is programmable by SPI via the BSTx_SLP_CTRL[2:0] register for each phase independently and can also be disabled. Due to the offset, current can start flowing in the circuit when VCOMP > COMP_VSF.

When booster is active, voltage at COMP pin is clamped from bottom side to 0.45 V (see Table 6 “BOOST CONTROLLER − VOLTAGE REGULATION PARAMETERS”), from the top side no clamp is present and internally there is a circuitry with functionality ensuring quick recovery and fast reaction of the system to load changes. Working range of the COMP pin is from 0.5 V to 2.1 V.

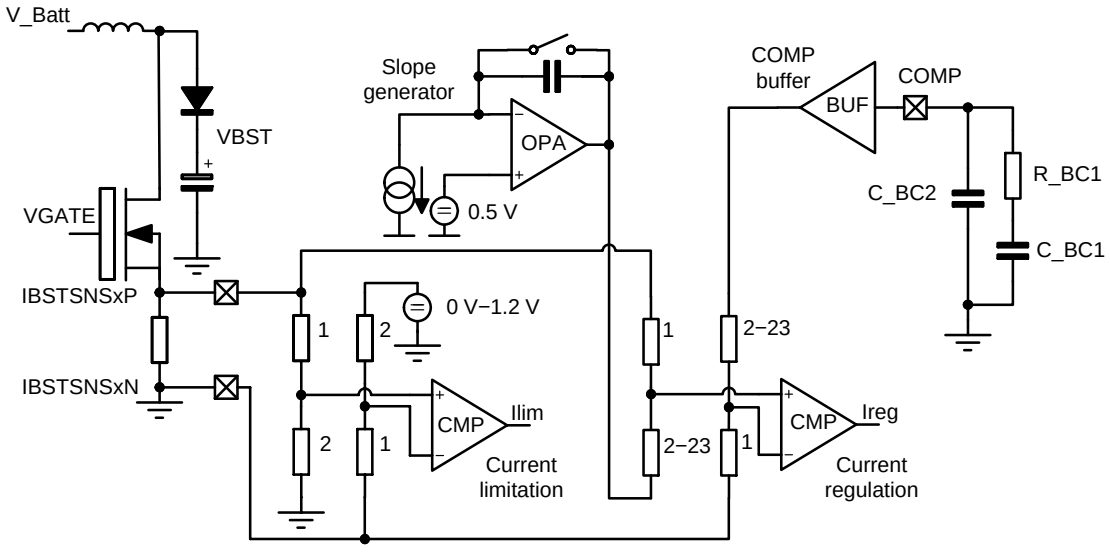


Figure 19. Booster Peak Current Regulator Involved in the Current Control Loop

Booster Current Limitation Protection

On top of the normal current regulation loop comparator, an additional comparator clamps the maximum physical current that can flow in the booster input circuit while the MOSFET is driven. The aim is to protect all the external components involved (boost inductor from saturation, boost diode and boost MOSFET from overcurrent, etc...). The protection is active PWM cycle-by-cycle and switches off the MOSFET gate when VSENSE reaches its maximum threshold defined by the BSTx_VLIM_THR[7:0] register (see Table 6 “BOOST CONTROLLER − CURRENT REGULATION PARAMETERS” for more details). Therefore, the maximum allowed peak current will be defined by the ratio

IPEAK_MAX = BSTx_VLIM_THR[7:0]/RSENSE or in case of sensing over booster MOSFET IPEAK_MAX = BSTx_VLIM_THR[7:0]/RDSon.

The maximum current must be set in order to allow the total desired booster power for the lowest battery voltage. Warning: setting the current limit too low may generate unwanted system behavior as uncontrolled de-rating of the LED light due to insufficient power.

Current limitation mode is mostly stable operating mode without subharmonic oscillations what allows to deliver maximum power to the load. Stable operation is achieved by regulating and tracking current limit threshold by dedicated algorithm. When booster phase regulates in this mode, ripple corresponding to regulation step BST_CBUF_STEP can be observed at inductor peak current. In certain border conditions some instabilities can occur, in such situation programming of longer PWM minimum on-time (BST_MIN_TON[1:0]) can help.

Booster PWM Internal Generation

This mode activated by BST_SRC = 1, creates the PWM frequency starting from the internal clock FOSC16M. A fine selection of frequencies is enabled by the register BST_SRC_FREQ[4:0], ranging from typical 125 kHz to typical 4 MHz (Table 6 “BUCK REGULATOR − TOFF GENERATOR”).

Maximum frequency per booster phase is supposed to be 2 MHz, so for example internally generated 4 MHz should be split to half between two phases.

Table 7. INTERNAL BOOSTER FREQUENCIES

BST_SRC_FREQ[4:0]	Freq (kHz)	BST_SRC_FREQ[4:0]	Freq (kHz)
0	125	16	727
1	140	17	800
2	160	18	889
3	176	19	1000
4	200	20	1067
5	222	21	1143
6	250	22	1231
7	276	23	1333
8	302	24	1455
9	333	25	1600
10	381	26	1778
11	444	27	2000
12	500	28	2286
13	552	29	2667
14	593	30	3200
15	667	31	4000

Booster PWM External Generation

When BST_SRC = 2, the booster PWM external generation mode is selected and the frequency is taken directly from the BSTSYNC device pin. There is no actual limitation in the resolution, but the same as indicated at PWM Internal Generation chapter is valid also here, the maximum frequency per booster phase should be 2 MHz and this implies maximum allowed frequency on BSTSYNC pin 4 MHz. The gate PWM is synchronized with either the rising or falling edge of the external signal depending on the BST_SRCINV bit value. The default POR value is “0” and corresponds to synchronization to the rising flank. BST_SRCINV equals “1” selects falling edge synchronization. Thanks to the possibility to invert external clock in the chip by SPI, up to 4-phase systems with shifted clock are supported with only 1 external clock.

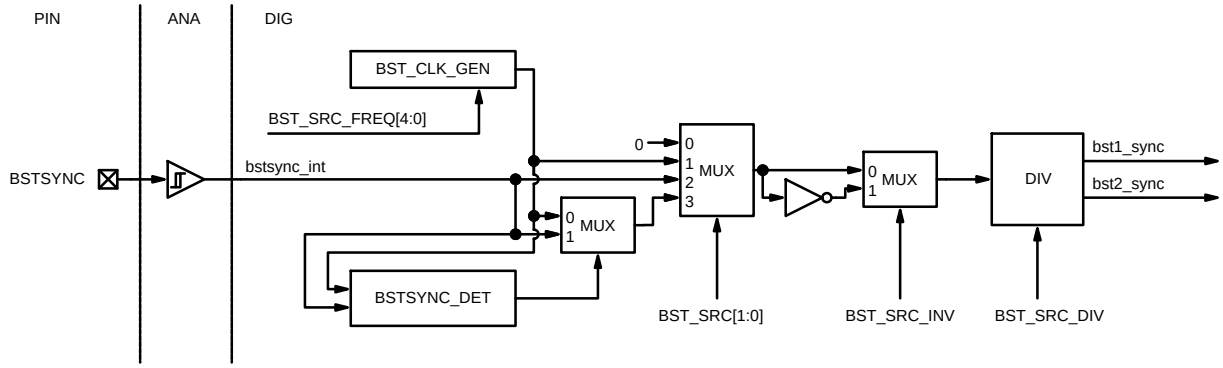


Figure 20. NCV78964 Booster Frequency Generation Block

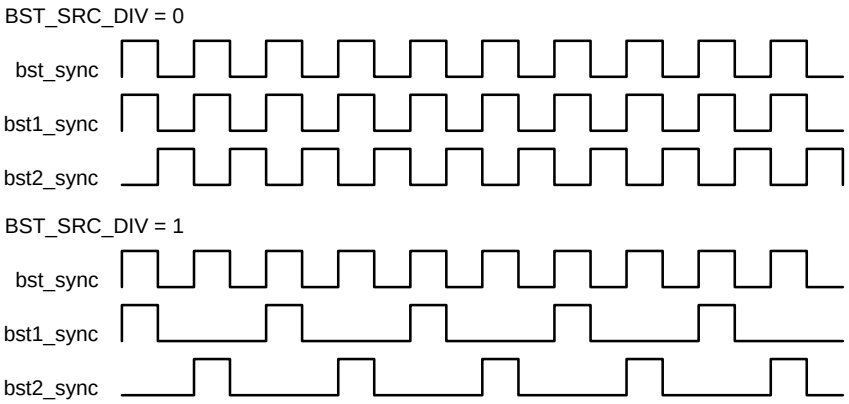


Figure 21. PWM Generator Clock Divider

Booster PWM Source Automatic Selection

When register BST_SRC = 3, the automatic booster PWM clock selection is activated. Switch sequence to internal clock is initialized when no rising edge on external source (bstsync_int on Figure 20) is detected within 3 consecutive rising edges of internal bst_sync clock. For this purpose, internal clock should be set to similar frequency as external source to ensure smooth transitions. Switch sequence to external clock is initialized when rising edge on external source (bstsync_int) is detected.

Table 8. BOOSTER PWM SOURCE SUMMARY

BST_SRC[1:0]	Booster Clock Source
0	Off
1	Internal
2	External
3	Auto External/Internal

Booster PWM Min TOFF and Min TON Protection

As additional protection, the PWM duty cycle is constrained between a minimum and a maximum, defined per means of two parameters available in the device.

The PWM *minimum on-time* is programmable via BST_MIN_TON[1:0]: its purpose is to guarantee a minimum activation interval for the booster MOSFET gate, to insure full drive of the component and avoiding switching in the linear region. Please note that this does not imply that the PWM is always running even when not required by the control loop, but means that whenever the MOSFET should be activated, then its on time would be at least the one specified. At the contrary when no duty cycle at all is required, then it will be zero.

The PWM *minimum off-time* is set via the parameter BST_MIN_TOFF[2:0]: this parameter is limiting the maximum duty cycle that can be used in the regulation loop for a defined period T_{PWM}:

$$Duty_{MAX} = \frac{\left(T_{PWM} - T_{OFFMIN}\right)}{T_{PWM}} \qquad \text{(eq. 3)}$$

The main aim of a maximum duty cycle is preventing MOSFET shoot-through in cases the (transient) duty cycle would get too close to 100% of the MOSFET real switch-off characteristics. In addition, as a secondary effect, a limit on the duty cycle may also be exploited to minimize the inrush current when the load is activated.

WARNING: A wrong setting of the duty cycle constraints may result in unwanted system behavior. In particular, a too big BST_MIN_TOFF[2:0] may prevent the system to regulate the VBOOST with low battery voltages (VBAT). This can be explained by the simplified formula for booster steady state continuous mode:

$$V_{BOOST} \cong \frac{V_{BAT}}{(1 - Duty)} \Leftrightarrow Duty \cong 1 - \frac{V_{BAT}}{V_{BOOST}} \qquad \text{(eq. 4)}$$

So in order to reach a desired VBOOST for a defined supply voltage, a certain duty cycle must be guaranteed.

Table 9. BOOSTER MINIMUM OFF TIME

BST_MIN_TOFF[2:0]	Min OFF Time (ns)
0	50
1	100
2	150
3	200
4	300
5	400
6	600
7	800

Table 10. BOOSTER MINIMUM ON TIME

BST_MIN_TON[1:0]	Min ON Time (ns)
0	100
1	150
2	200
3	300

Booster Compensator Model

A linear model of the booster controller compensator (block “A” Figure 16) is provided in this section. The protection mechanisms around are not taken into account. A type “2” network is taken into account at the VCOMP pin. The equivalent circuit is shown below:

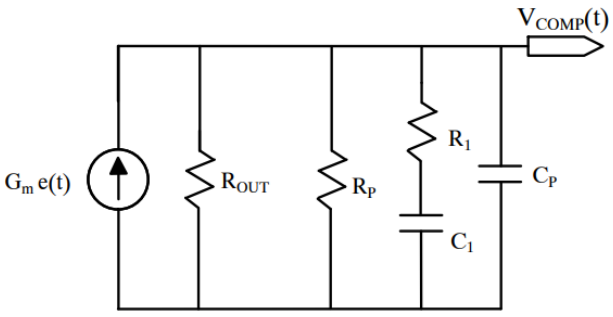


Figure 22. Booster Compensator Circuit with Type “2”

In the Figure, e(t) represents the control error, equals to the difference $V_{BST\_VSETPOINT}(t) - V_{BST}(t)$. “$G_m$” is the trans-conductance error amplifier gain (see Table 6 “BOOST CONTROLLER − VOLTAGE REGULATION PARAMETERS”), while “R_{OUT}” is the amplifier internal output resistance (parameter EA_BLR in Table 6 “BOOST CONTROLLER − VOLTAGE REGULATION PARAMETERS”). By solving the circuit in Laplace domain the following error to V_{COMP} transfer function is obtained:

$$H_{COMP} = \frac{V_{COMP}(s)}{e(s)} = G_m R_{OUT} \frac{\tau_1 s + 1}{\tau_1 \tau_P s^2 + (\tau_P + \tau_{1P}) s + 1} \quad \text{(eq. 5)}$$

The explanation of the parameters stated in the equation above follows:

$\tau_1 = R_1 C_1$
$\tau_P = R_1 C_P$
$\tau_{1P} = (R_1 + R_{OUT})\, C_1$

This transfer function model can be used for closed loop stability calculations.

Booster PWM Skip Cycles

In case of light booster load, it is useful to reduce the number of effective PWM cycles in order to get a decrease of the input current inrush bursts and a less oscillating boost voltage. This can be obtained by using the “skip cycles” feature, programmable by SPI via BST_SKCL_THR[1:0] (see Table 6 “BOOST CONTROLLER − VOLTAGE REGULATION PARAMETERS”).

The selection defines the VCOMP voltage threshold below which the PWM is stopped, thus avoiding VBOOST oscillations in a larger voltage window.

Booster Multiphase Mode Principles

The NCV78964 device supports two booster phases, which are connected together to the same VBST node, sharing the boost capacitor block. Multiphase mode shows to be a cost effective solution in case of mid to high power systems, where bigger external BOM components would be required to bear the total power in one phase only with the same performances and total board size. In particular, the boost inductor could become a critical item for very high power levels, to guarantee the required minimum saturation current and RMS heating current.

Another advantage is the benefit from EMC point of view, due to the reduction in ripple current per phase and ripple voltage on the module input capacitor and boost capacitor. The picture below shows the (very) ideal case of 50% duty cycle, the ripple of the total module current (I_{Lmp_sum} = I_{L1mp} + I_{L2mp}) is reduced to zero. The equivalent single phase current (I_{Lsp}) is provided as a graphical comparison.

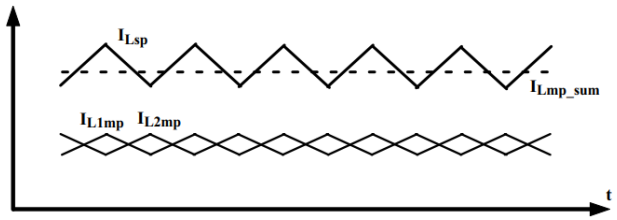


Figure 23. Booster Single Phase vs. Multiphase Example

Booster Multichip Connection Diagram and Programming

For high-power systems more NCV78964 devices can be combined to gain even more synchronized booster phases.

This section describes the steps both from hardware and SPI programming point of view to operate in multichip mode. Example of physical connection of two devices is provided in this section. From a hardware point of view, it is assumed that in multiphase mode (N boosters), each stage has the same external components. The following features have to be considered as well:

1. The compensation network is split between the two boosters’ COMP pins according to Figure 24, to equalize the power distribution of each booster. For the best noise rejection, the compensation network area has to be surrounded by the GND plane. Please refer to the PCB Layout Recommendations section for more general advices.

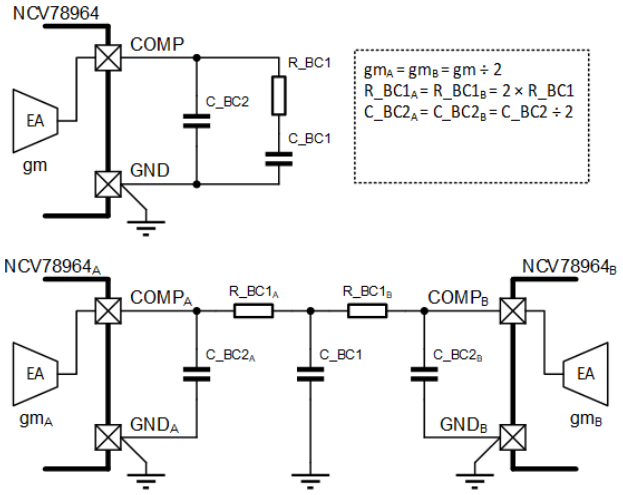


Figure 24. Compensation Network Connection for Single (Top) and Dual (Bottom) Device Operation

2. To synchronize the MOSFET gate PWM clock and needed phase shifts, the boosters must use the external clock generation (BSTSYNC), generated by the board MCU or external logic, according to the user-defined control strategy. The generic number of lines needed is equivalent to the number of devices. When two chips are combined, the slave device shall have BST_SRC_INV bit at '1' (clock polarity internal inversion active), whereas the master device will keep the BST_SRC_INV bit at '0' (= no inversion, default). On top of that, to get four phases with phase shift, the BST_SRC_DIV bit has to be at '1', meaning that gate clock is divided by two (please see Figure 20 and Figure 21 for more details).
3. Both devices should have error amplifier OTA set to the same gain value by means of register BST_OTA_GAIN[1:0]. Please note, that gain of both error amplifiers sums up.
4. Overvoltage settings of both devices should be set to the same level. Each device senses boost voltage via its VBST pin and reacts to the overvoltage situation independently. See also "Booster Overvoltage Shutdown Protection" for more details on the protection mechanism and threshold.

Booster Enable and Disable Control

Each of the NCV78964 booster phases can be enabled/disabled directly by SPI via the corresponding BST1_EN or BST2_EN bit. The enable signal is the transition from "0" to "1"; the disable function is vice-versa. The status of the physical activation is contained in the flag BSTx_RUNNING: whenever the booster is running, the value of the flag is one, otherwise zero. It might in fact happen that despite the user *wanted* activation, the booster is stopped by the device in few cases:

1. Whenever the Thermal Shutdown TSD was triggers. Booster is re-enabled automatically when temperature falls below programmed thermal warning TW level. For more details see dedicated Diagnostic Description chapter.
2. VDRV Undervoltage VDRV_UV was detected. After this error, the booster operation can be automatically resumed when automatic recovery is enabled by VDRV_UV_RCVR bit. For more details see dedicated Diagnostic Description chapter.
3. Booster feedback failure was detected. This situation is indicated by BST_FBFAIL failure flag.
4. Booster internal hardware error was detected. This situation is indicated by BST_OSCFAIL failure flag.

Booster Soft-start

In order to limit inrush current during booster start up, the soft-start feature is available. Soft-start function ramps up booster voltage setpoint with defined step duration. Booster soft-start is controlled by the BST_SOFTSTART[2:0] register.

Table 11. BOOSTER SOFT-START

BST_SOFTSTART[2:0]	Step Duration (µs)
0	Soft-start disabled
1	12
2	20
3	28
4	36
5	44
6	52
7	60

Booster Diagnostic Description

- *Booster skip cycle*: indicates that skip cycle mode has been present in the regulation. BST_SKCL flag (latched) is contained in status register 0x36.
- *Booster overvoltage*: an overvoltage is detected by the booster control circuitry. BST_OV flag (lachted) is contained in status register 0x36.
- *Booster feedback failure*: when voltage at booster voltage feedback pin VBST is lost (detected by VBST voltage drop below BST_FBFAIL threshold, see Table 6 "BOOST CONTROLLER − VOLTAGE REGULATION PARAMETERS"), the booster is switched off. The failure is indicated by BST_FBFAIL status flag (reg. 0x36).
- *Booster oscillator failure*: BST_OSCFAIL fail flag is contained in status register 0x36 and indicates Booster internal hardware error. After detection of this error the Booster is switched off.
- *Booster VDRV undervoltage*: VDRV Undervoltage Lockout safety mechanism monitors sufficient voltage for booster MOSFETs and protects them by switching off the booster when VDRV voltage is too low. Detection level is set by VDRV_UV_THR[2:0] register (see Table 6

"VDRIVE: SUPPLY FOR BOOSTER MOSFET GATE DRIVE CIRCUIT AND BUCK LOW SIDE SWITCHES" for more details). When VDRV_UV_THR[2:0] = 0, the function is disabled. VDRV_UV (latched, reg. 0x36) flag indicates that protection has acted. Automatic reactivation of the booster after VDRV undervoltage can be enabled by VDRV_UV_RCVR bit.

- *Booster regulation status*: indicates for each booster phase individually that it runs in limitation mode. BSTx_REGSTATUS[1:0] registers are contained in status register 0x36. Coding of the register is the following:

Table 12. BOOSTER REGULATION STATUS

Booster Limitation Mode	BSTxREGSTATUS[1:0]
Normal (Ireg comparator)	00
Limitation by current limit (Ilim comparator)	01
Limitation by minimum toff time (BST_MIN_TOFF)	10

- *Booster running*: the physical activation of the booster is displayed by the BSTx_RUNNING flag (non-latched, reg. 0x36). Please note this is different from the BSTx_EN control bits, which reports instead the *willing* to activate the booster. See also section "Booster Enable and Disable Control".

BUCK REGULATOR

General

The NCV78964 contains two high-current integrated buck current regulators, which are the sources for the LED strings. The bucks are powered from the booster regulator or from battery voltage with proper input filter and reverse polarity protection. Each buck channel can be powered from different input voltage.

Buck Current Regulation Principle

Each buck controls the peak current ($I_{BUCK_{peak}}$) and average current ($I_{BUCK_{AVG}}$) and incorporates a constant ripple ($\Delta I_{BUCK_{pkpk}}$) control circuit to ensure stable average current through the LED string, independently from the string voltage. On top of that, constant frequency (f_{BUCK}) mode is available.

The buck average current is in fact described by the formula:

$$I_{BUCK_{AVG}} = I_{PEAK_{peak}} - \frac{\Delta I_{BUCK_{RIP}}}{2} \quad \text{(eq. 6)}$$

This is graphically exemplified by Figure 25.

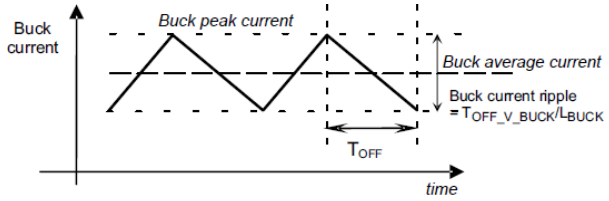


Figure 25. Buck Regulator Controlled Average Current

The average current ($I_{BUCK_{AVG}}$) is programmable through the device by means of the internal registers for range selection BUCKx_IRNG[1:0] and code BUCKx_IAVG[7:0]. The peak current is regulated automatically by internal algorithm.

The LED average current in time (DC) is equal to the buck average current. LED ripple current is defined by the Buck inductor ripple current, the buck capacitor C_{BUCK} and the LED string impedance. A rule of thumb is to target a 50% ripple reduction with the capacitor C_{BUCK} and this is normally obtained with a low cost ceramic component ranging from 100 nF to 470 nF. The following figure reports a typical example waveform:

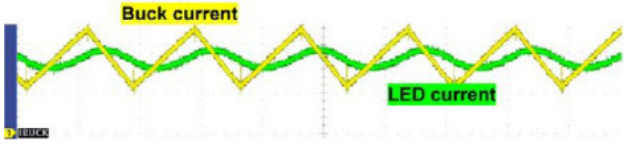


Figure 26. LED Current AC Components Filtered Out by Output Impedance (Oscilloscope Snapshot)

The use of C_{BUCK} is a cost effective way to improve EMC performances without the need to increase the value of L_{BUCK}, which would be certainly a far more expensive solution.

Constant Frequency Regulation Principle

Constant operating frequency of each buck can be programmed by BUCKx_FREQ[5:0] register with values related to Table 13. This regulation loop is able to achieve constant buck frequency by varying the current ripple by dedicated algorithm.

When BUCK_FREQ[5:0] register is 0, the frequency regulation is disabled and buck runs in constant ripple operating mode which is described in the following paragraph.

If there is a requirement to set specific starting frequency for regulation, the following procedure should be followed: Buck disabled (BUCKx_EN = 0) → set LEDCTRL/dimming off → set BUCKx1_TOFF[6:0] to required starting Toff·VLED → Disable frequency reg. by BUCKx_FREQ[5:0] = 0 → enable Buck (BUCKx_EN = 1) → set BUCKx_FREQ[5:0] to required value → set LEDCTRL/dimming on.

Table 13. BUCK FREQUENCY REGULATION

BUCKx_FREQ[5:0]	Freq (kHz)	BUCKx_FREQ[5:0]	Freq (kHz)
0	OFF	32	691
1	180	33	719
2	188	34	753
3	196	35	784
4	205	36	821
5	214	37	857
6	223	38	893
7	233	39	932
8	244	40	975
9	254	41	1016
10	265	42	1061
11	277	43	1110
12	289	44	1157
13	302	45	1208
14	316	46	1263
15	331	47	1324
16	345	48	1381
17	360	49	1438
18	376	50	1506
19	392	51	1567
20	410	52	1641
21	429	53	1714
22	447	54	1786
23	466	55	1864
24	487	56	1949
25	508	57	2032
26	530	58	2122
27	555	59	2220
28	578	60	2313
29	604	61	2415
30	632	62	2526
31	662	63	2648

Summary of SPI Parameters Related to Frequency Regulation:

BUCKx_FREQ[5:0] − control register selecting Buck operating frequency

BUCKx_FREQ_ABOVE − control register defining whether frequency is regulated below (0) or above (1) threshold BUCKx_FREQ

BUCKx_FREQ_FAST_RCVR − control register defining recovery speed of regulation:
0 − Slow: There is always minimal response time (BUCKx_FREQ_RSP[1:0]) between two regulations.
1 − Fast: Regulation is running every regulation cycle after the first minimal response time.

BUCKx_FREQ_RSP[1:0] − control register selecting minimal regulation response time:

Table 14.

BUCKx_FREQ_RSP[1:0]	Minimal Response Time (ms)
0	0.1
1	6.4
2	12.8
3	25.6

BUCKx_FREQ_RATE[1:0] − control register which sets maximum regulation step within one regulation cycle:

Table 15.

BUCKx_FREQ_RATE[1:0]	Max Number of Steps
0	1
1	2
2	4
3	8

BUCKx_FREQ_PAUSE − control register allowing to pause frequency regulation.

BUCKx_TOFF_MON[6:0] − status register monitoring actual TOFF time.

Constant Ripple Regulation Principle

The formula that defines the total ripple current over the buck inductor is also hereby reported:

$$\Delta I_{BUCK_{RIP}} = \frac{T_{OFF} \cdot (V_{LED} + V_{BDRDSON})}{L_{BUCK}} = \frac{T_{OFF} \cdot V_{COIL}}{L_{BUCK}} = \frac{T_{OFF\_}V_{COIL\_}i_{SPI}}{L_{BUCK}} \quad \text{(eq. 7)}$$

In the formula above, T_{OFF} represents the buck switch off time, V_{COIL} is the voltage over the inductor (sensed at VLEDx and BCKx pins) and L_{BUCK} is the buck inductance value. The parameter $T_{OFF\_}V_{COIL\_}i_{SPI}$ is programmable by SPI (BUCKx_TOFF[6:0] register), with values related to Table 6 “BUCK REGULATOR − TOFF GENERATOR”. The device is trimmed in the way that code 32 in BUCKx_TOFF[6:0] register corresponds to 5 µs·V and from this reference value 1 code to each direction corresponds to step of $\sqrt[16]{2}$. In order to achieve a constant ripple current value, the device varies the T_{OFF} time inversely proportional to the V_{COIL} (V_{LED} + V_{DIODE}) according to the selected factor $T_{OFF\_}V_{COIL\_}i_{SPI}$. As a consequence to the constant ripple control and variable off time, the buck switching frequency depends on the boost voltage and LED voltage in the following way:

$$f_{BUCK} = \frac{(V_{BOOST} - V_{LED})}{V_{BOOST}} \cdot \frac{1}{T_{OFF}} = \frac{(V_{BOOST} - V_{LED})}{V_{BOOST}} \cdot \frac{V_{LED}}{T_{OFF\_}V_{COIL}T_{OFF\_}i_{SPI}} \quad \text{(eq. 8)}$$

Average Current Regulation Principle

Required average current ($I_{BUCK_{AVG}}$) is programmable through the device by means of the internal registers for range selection BUCKx_IRNG[1:0] and code BUCKx_IAVG[7:0].

The NCV78964 is able to regulate the average current based on the information obtained during Ton time only. The current is measured during Ton time twice − at $I_{BUCK_{AVG}}$ level and at $I_{BUCK_{peak}}$ level. The time between $I_{BUCK_{valley}}$ and $I_{BUCK_{AVG}}$ is compared to time between $I_{BUCK_{AVG}}$ and $I_{BUCK_{peak}}$ and $I_{BUCK_{peak}}$ (in fact "$I_{BUCK_{peak}}$ − $I_{BUCK_{AVG}}$" value) is regulated by internal algorithm to make both times equal and match the programmed average current.

Information about regulated value of " $I_{BUCK_{peak}}$ − $I_{BUCK_{AVG}}$" is available in BUCKx_IRIP[8:0] status register.

Automatic regulation of buck average current can be paused (meaning BUCKx_IRIP is not updated) when BUCKx_IREG_PAUSE register is written to 1.

Summary of SPI Parameters Related to Current Regulation:

BUCKx_IRNG[1:0] − control register selecting buck current range.

BUCKx_IAVG[7:0] − control register defining buck average current.

BUCKx_TOFF[6:0] − control register defining buck inductor current ripple when frequency regulation is disabled

BUCKx_IREG_PAUSE − control register allowing to pause buck average current regulation.

BUCKx_IRIP[8:0] − status register, read only. Provides information about "$I_{BUCK_{peak}}$ − $I_{BUCK_{AVG}}$" value regulated by internal algorithm.

BUCKx_IRIP_UPD − status bit informing, that BUCKx_IRIP[8:0] register was updated with actual measurement result.

BUCKx_TOFF_MON[6:0] − status register monitoring actual TOFF time.

BUCKx_REGSTATUS[1:0] − reports status of IRIP control algorithm. All statuses are summarized in the following table:

Table 16. IRIP REGULATION STATUS REPORTING

IRIP Regulation Status	BUCKx_REGSTATUS[1:0] Value
Buck regulation is disabled	00
IRIP is settling (buckx_irip increment is larger than 1)	11
IRIP is at target (buckx_irip increment value is 1)	10
IRIP regulation failure (failure detected 5 times in a row or automatic regulation sets buckx_irip to 0 or 511)	01

Buck Operating Modes

Continuous Current Mode (CCM)

T_{OFF} time is generated by TOFF generator and its duration is inversely proportional to V_{COIL} voltage. Current ripple is defined by the following formula:

$$\Delta I_{BUCK_{RIP}} = \frac{T_{OFF} \cdot V_{COIL}}{L_{BUCK}} \quad \text{(eq. 9)}$$

and corresponding peak current is

$$I_{BUCK_{peak}} = I_{BUCK_{AVG}} + \frac{I_{BUCK_{RIP}}}{2} \quad \text{(eq. 10)}$$

This peak value will be found automatically if Average current regulation loop is enabled.

If toff ≥ toff_ZC then operation goes either to BCM or DCM mode.

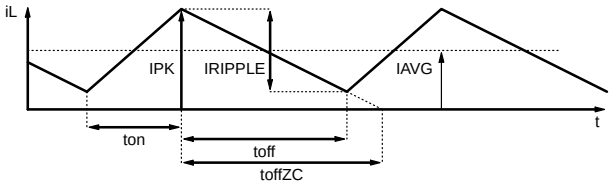


Figure 27. Inductor Current in CCM Mode

Border Continuous Mode (BCM)

If BCM mode is not disabled by buck configuration (BUCKx_ZCD_DIS = 0), the buck starts operation in BCM mode when toff is greater than toff_ZC. In this mode toff is limited to toff_ZC by ZCD (zero cross detection) retrigger controller.

Average current regulation loop will find the following peak value:

$$I_{BUCK_{peak}} = 2 \cdot I_{BUCK_{AVG}} = \Delta I_{BUCK_{RIP}} \quad \text{(eq. 11)}$$

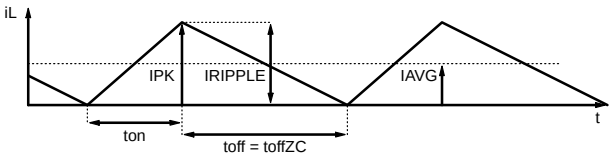


Figure 28. Inductor Current in BCM Mode

Discontinuous Current Mode (DCM)

If BCM mode is disabled by buck configuration (BUCKx_ZCD_DIS = 1), the buck will operate in DCM mode when toff is greater than toff_ZC. In this mode toff is not limited to toff_ZC and full toff is applied.

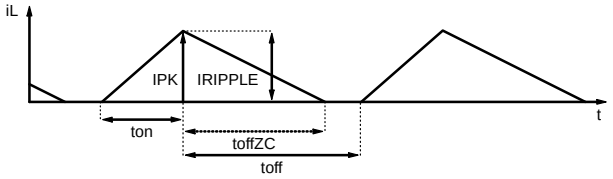


Figure 29. Inductor Current in DCM Mode

When Average current regulation is enabled in DCM mode by BUCKx_DCM_CORR[2:0] register being different from 0, Average current regulation loop will find such peak value of the current $I_{BUCK_{peak}}$ that Average current $I_{BUCK_{AVG}}$ over whole Buck period corresponds to programmed value in BUCKx_IAVG[7:0] and BUCKx_IRNG[1:0] registers.

Please note that in DCM mode accuracy of the Average current is worse and cannot be guaranteed and should be evaluated in specific application conditions.

In DCM mode, the Bootstrap CBT capacitor is recharged only during ToffZC time, not during the rest of toff time (when ringing occurs).

Zero Cross Detector

The zero cross detection (ZCD) comparator is implemented to ensure proper Toff time termination when the coil current drops to zero (boundary conduction mode). The implemented advanced zero cross detector allows to operate the device in semi-resonant mode, providing possibility to reduce switching power losses.

Principle is that after the current in the inductor drops to zero, the circuitry waits until the voltage at BCKx pin rises autonomously (by ringing) and at the point the voltage is the highest (should correspond to 2 x VLED), the high side switch switches on, spending the least amount of energy.

SPI flag BUCKx_ZCDMODE being '1' indicates that Zero Cross event was detected by Zero Cross detector. When BUCKx_ZCD_DIS SPI control bit was 0 during that moment, the Toff time was terminated by Zero Cross circuitry.

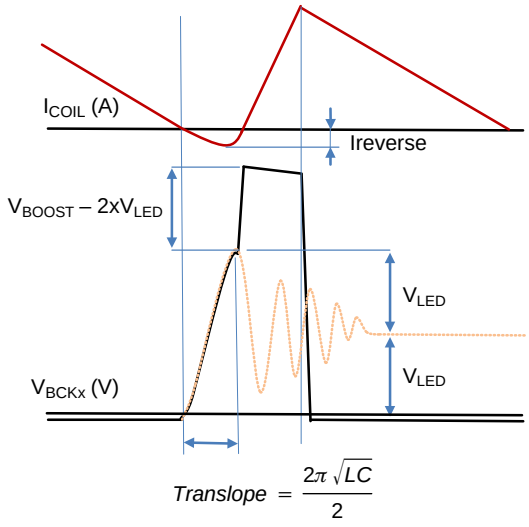


Figure 30. Semi-resonant Mode Principle

Average Current Accuracy

Average current accuracy is determined by the accuracy of the Current sense comparator threshold (see parameters IERR and IERR_LRNG in Table 6 "BUCK REGULATOR − HIGH SIDE SWITCH AND CURRENT REGULATION") and accuracy of Timing comparator for average current detection (see parameters TONCMPOFFS and TONCMPERR in Table 6 "BUCK REGULATOR − TIMING COMPARATOR FOR AVERAGE CURRENT DETECTION") which contributes to final $I_{BUCK_{AVG}}$ error depending on ratio of current ripple $\Delta I_{BUCK_{RIP}}$ to average current $I_{BUCK_{AVG}}$. It is possible to derive that contribution of Timing comparator is total error is:

$$\frac{\Delta I_{BUCK_{RIP}}}{2 \cdot I_{BUCK_{AVG}}} \cdot \text{TONCPERR} \qquad \text{(eq. 12)}$$

(or needs to be calculated with TONCMPOFFS for very short On times).

Please note, that in case when current in the inductor does not have ideal triangle waveform shape, final accuracy of average current will be affected. It usually happens when setup is operated in extreme conditions (extremely low or high frequency, small voltage room over inductor, extremely big ripple). This needs to be evaluated in each specific case in real application.

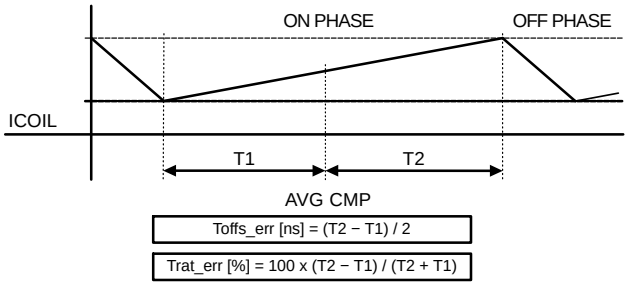


Figure 31. Definition of Time Offset and Time Ratio Error

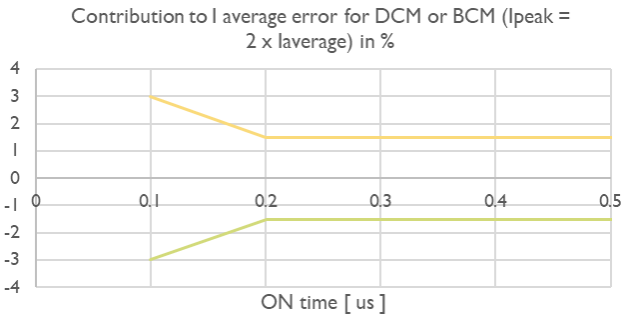


Figure 32. Contribution of Timing Comparator to $I_{BUCK_{AVG}}$ Error

Current Limiter

Buck regulator features current limiter which limits t2 time (corresponding to "$I_{BUCK_{peak}} - I_{BUCK_{AVG}}$") in relation to t1 time (corresponding to "$I_{BUCK_{AVG}} - I_{BUCK_{valley}}$"), meaning Ton time can be stopped sooner than $I_{BUCK_{peak}}$ is reached. Please see parameter TONTOUT in Table 6 "BUCK REGULATOR − TIMING COMPARATOR FOR AVERAGE CURRENT DETECTION". Effect of the limiter can be observed for example during regulation setpoint transitions.

Buck Regulator Control and Start

Buck activation is controlled by LEDCTRLx pin and corresponding SPI bit BUCKx_EN.

Table 17. LEDCTRLx PIN MODES

LEDCTRLx_MD[1:0]	Behavior in Application	LEDCTRL Pull-up/Down Selection
0	Standard behavior of LEDCTRLx pin: LEDCTRLx = '1': Buck activation controlled by corresponding SPI bit BUCKx_EN LEDCTRLx = '0': Buck turned off	Pull-down
1	Inverted behavior of LEDCTRLx pin: LEDCTRLx = '1': Buck turned off LEDCTRLx = '0': Buck activation controlled by corresponding SPI bit BUCKx_EN	Pull-up
2	LEDCTRL used as voltage sense input for voltage mode	HiZ
3	LEDCTRL pin ignored. Buck activation controlled by corresponding SPI bit BUCKx_EN	HiZ

CBT domain stays active app. 12 ms after deactivation of the channel to support minimal dimming frequency 100 Hz ±5%. After that time, CBT domain is deactivated in defined way.

When enabling the Buck channel again after more than 12 ms, the CBT capacitor needs to be charged again and delay after Buck enable signal is introduced before Buck starts its operation. Also there can be observed some transition of up to app. 20 periods until average current is settled at required level. This is caused by internal compensation of comparators offsets and time needed by average current regulation loop to find the correct BUCK_IRIP ($I_{BUCK_{peak}}$) setpoint.

When buck is enabled sooner than app. 12 ms elapses from previous disabling (typical example is PWM dimming off time), the regulation starts from the correct BUCK_IRIP ($I_{BUCK_{peak}}$) setpoint found during previous run and no transition effect is present.

Buck Voltage Mode

NCV78964 Buck controller can also regulate output voltage instead of output current. To operate Buck channel in this mode, additional feedback loop has to be introduced between output voltage node and LEDCTRLx input pin, see Figure 33 for reference. External compensation loop should be designed to ensure stability. Voltage mode can be enabled by writing register LEDCTRLx_MD[1:0] to 2.

When voltage sensed by LEDCTRLx pin rises above comparator threshold, PWM regulator immediately interrupts current TON phase and starts TOFF phase and skips following TON phases until voltage drops below set point threshold (green and yellow sections on Figure 34).

When voltage sensed on LEDCTRLx pin falls below threshold, two possible scenarios can occur:

a. Top switch was turned off longer time than settings of TOFF. In this case top switch is immediately turned on and PWM generation starts again (green section on Figure 34)

b. Top switch was turned off shorter time than settings of TOFF. In this case top switch remains off until full TOFF time expires and then is turned on (yellow section on Figure 34).

Being below threshold, Buck regulator can operate in any of CCM, BCM or DCM modes depending on Buck configuration.

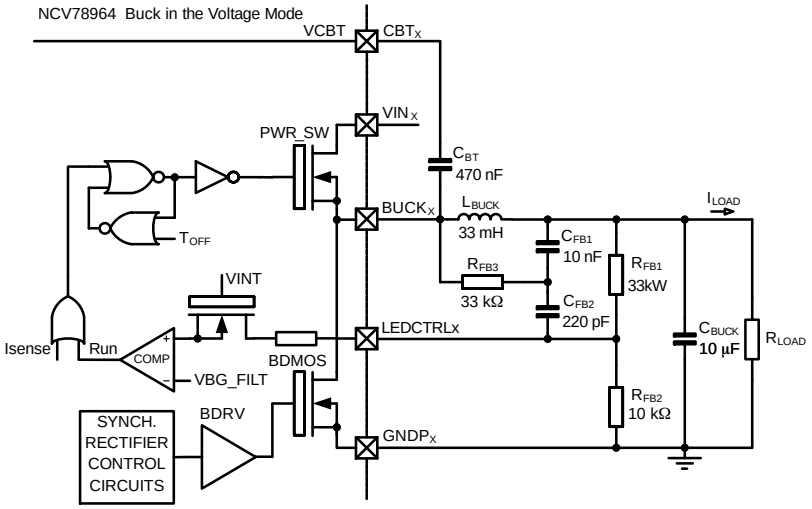


Figure 33. Buck Voltage Mode Feedback Loop

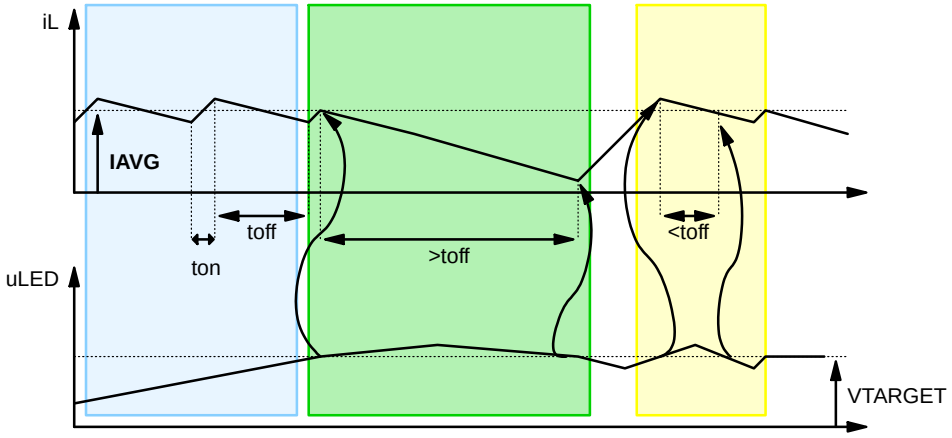


Figure 34. Buck Voltage Mode Regulation Principle

Buck Current and Ripple Calibration Principle

Average current calibration is performed internally by the NCV78964 without interaction of user software. Quadratic approximation, which is basically required to compensate current dependency over full temperature range, is divided into three linear intervals. Actually measured VTEMP temperature is used as input of the algorithm together with array of constants in EEPROM calibrated during ATE test.

Example of bilinear interpolation of quadratic approximation of BUCKx_IAVG is depicted in Figure 35, BUCKx_IAVG = 192 = 75% of current range, BUCKx_IAVGCy_CAL = 350, BUCKx_IAVGHy_CAL = 400, BUCKx_IAVOCy_CAL = 150, BUCKx_IAVOHy_CAL = 100, BUCK_KQ_CAL = 7.75, TEMPCODEC = 200 and TEMPCODEH = 400.

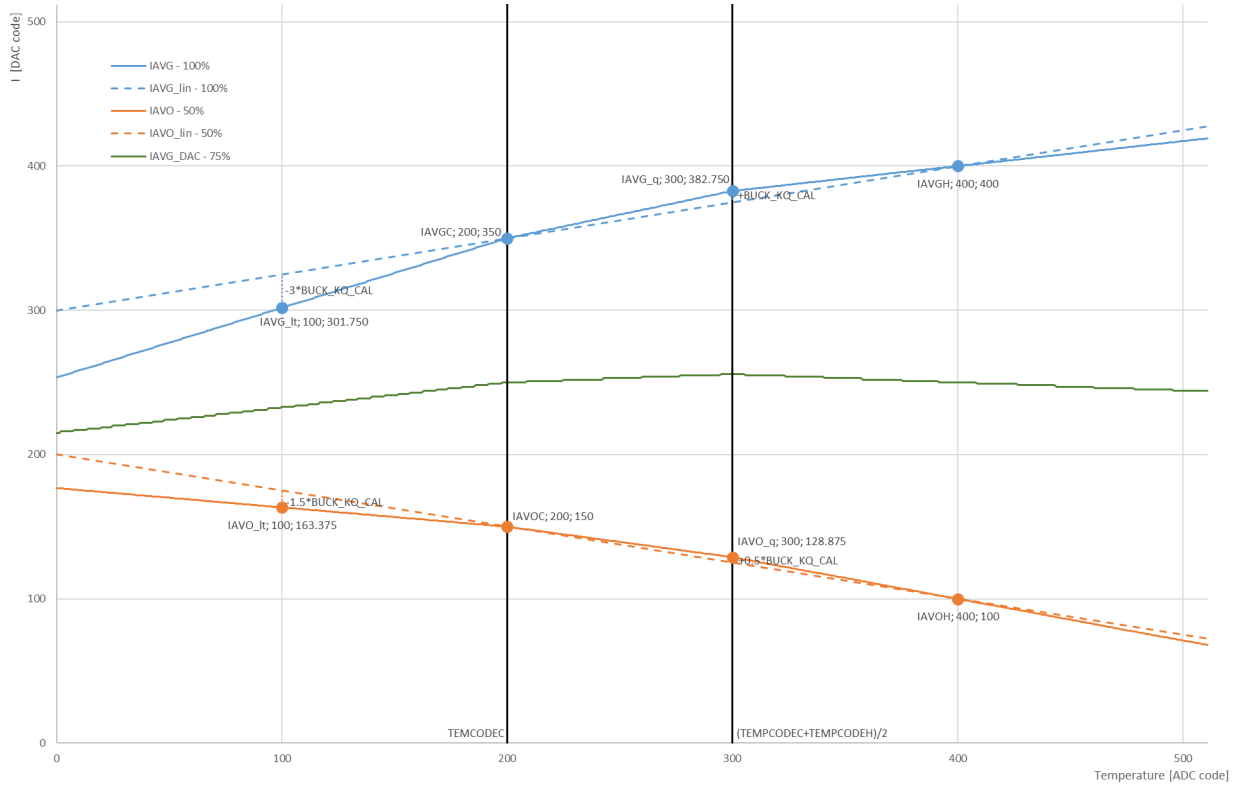


Figure 35. Bilinear Interpolation of BUCKx_IAVG

Paralleling the Bucks for Higher Current Capability

Different buck channels can be paralleled at the module output (after the buck inductors) for *higher current capability* on a unique channel, summing up together the individual DC currents.

Dimming

The NCV78964 supports both analog and digital dimming (or so called PWM dimming). Analog dimming is performed by controlling the LED amplitude current during operation. This can be done by means of changing the average current level (see Buck Regulator section).

In this section, we only describe PWM dimming as this is the preferred method to maintain the desired LED color temperature for a given current rating. In PWM dimming, the LED current waveform frequency is constant and the duty cycle is set according to the required light intensity. In order to avoid the beats effect, the dimming frequency should be set at “high enough” values, typically above 300 Hz.

The device handles two distinct PWM dimming mode: *external* or *internal*.

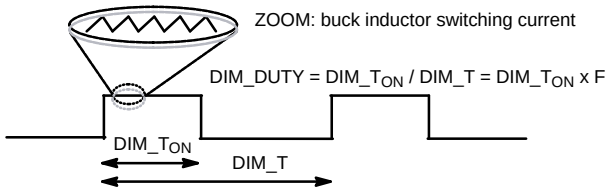


Figure 36. Buck Current Digital or PWM Dimming

External Dimming

The two independent control inputs LEDCTRLx handle the dimming signals for the related channel “x”. In external dimming, the buck activation is transparently linked to the logic status of the LEDCTRLx pins. The only difference is the controlled phase shift of typical 4 µs (Table 6 “5 V TOLERANT DIGITAL INPUTS (SCLK, CSB, SDI, LEDCTRL1, LEDCTRL2, BSTSYNC)”) that allows synchronized measurements of the VLEDx pins via the ADC (see dedicated section for more details). As the phase shift is applied both to rising edges and falling edges, with a very limited jitter, the PWM duty cycle is not affected. Apart from the phase shift and the system clock OSC16M, there is no limitation to the PWM duty cycle values or resolutions at the bucks, which is a copy of the reference provided at the inputs.

Internal Dimming

This mode is applied by means of BUCKx_DIM_DUTY[7:0] registers for corresponding channel. There is exponential dependency of the applied duty ratio on the BUCKx_DIM_DUTY[7:0] register value:

$$\text{Duty Ratio [−]} = 2^{\frac{\text{BUCKx\_DIM\_DUTY[7:0]} - 255}{16}} \quad \text{(eq. 13)}$$

Or in percentage:

$$\text{Duty Ratio [\%]} = 100 \times 2^{\frac{\text{BUCKx\_DIM\_DUTY[7:0]} - 255}{16}} \quad \text{(eq. 14)}$$

The dimming PWM frequency is common between the channels and is programmable via the SPI parameter BUCK_DIM_FREQ[1:0] (in register 0x0D), as displayed in the table below. All frequencies are chosen sufficiently high to avoid the beads effect in the application. Please also note that the higher the frequency, the lower the voltage drop on the booster output due to the lower load power step.

Table 18. INTERNAL PWM DIMMING PROGRAMMABLE FREQUENCIES

BUCK_DIM_FREQ[1:0]	PWM Frequency (Hz)
0	244
1	488
2	977
3	1953

The phase shift between the channels during internal dimming can be controlled by programming the bit BUCKx_DIM_SHIFT for corresponding channel.

Table 19. INTERNAL PWM DIMMING PROGRAMMABLE PHASE SHIFT

BUCKx_DIM_SHIFT	BUCKx Phase Shift
0	0°
1	180°

Fading

Fading feature performs smooth transitions between different duty ratios. Fading effect is enabled when BUCKx_DIM_FADEIN[2:0] or BUCKx_DIM_FADEOUT[2:0] is different from 0. BUCKx_DIM_FADE status flag being 1 indicates that fading effect is in progress.

Fade in effect (increasing of the brightness) is started and performed when newly written value in BUCKx_DIM_DUTY[7:0] register is higher than actual duty ratio. Applied duty ratio is then gradually increased by 1 with step duration defined by BUCKx_DIM_FADEIN[2:0] register.

Fade out effect (decreasing of the brightness) is started and performed when newly written value in BUCKx_DIM_DUTY[7:0] register is lower than actual duty ratio. Applied duty ratio is then gradually decreased by 1 with step duration defined by BUCKx_DIM_FADEOUT[2:0] register:

Table 20. FADE IN/OUT PROGRAMMABLE STEP DURATION

BUCKx_DIM_FADEIN[2:0] or BUCKx_DIM_FADEOUT[2:0]	FADE IN/OUT Step Duration (µs)
0	FADE IN/OUT OFF
1	256
2	512
3	1024
4	2048
5	4096
6	8192
7	16384

Fade in and fade out effects are functional also when output is activated/deactivated by LEDCTRLx pin. Fade in effect then starts with zero duty ratio and ends at duty ratio corresponding to BUCKx_DIM_DUTY[7:0] register value. Fade out effect starts at duty ratio corresponding to BUCKx_DIM_DUTY[7:0] register value and ends at zero duty ratio.

Required Enable/Disable Sequences and Enhanced Dimming Control

Case 1: Controlling the Buck Channels via LEDCTRLx Pins

The Buck channel with register BUCKx_DIM_SHIFT[1:0] programmed to value different from 0 must not be switched off by LEDCTRLx pin as the last from all channels. When BUCKx_DIM_FADEOUT[2:0] is different from 0, this constraint does not apply.

Case 2: Activating the Buck Channels via SPI Commands

The BUCKx_DIM_DUTY[7:0] can be set to 255 only after BUCKx_EN is set to 1 when BUCKx_DIM_FADEIN[2:0] is different from 0. Recommended sequence is then: BUCKx_EN=0 → BUCKx_DIM_DUTY[7:0]=0 → BUCKx_EN=1 → BUCKx_DIM_DUTY[7:0]=255. When BUCKx_DIM_FADEIN[2:0]=0, this constraint does not apply.

Case 3: Transition of Control Method from SPI to LEDCTRLx Pins via LEDCTRLx_MD[1:0] Register

When BUCKx_DIM_FADEIN[2:0] is different from 0 and LEDCTRLx_MD[1:0] is changed from 'Ignored' to 'Normal' (also via using EEPROM and FSO mode), the transition on LEDCTRLx pin is required to recover and synchronize the correct state of LEDCTRLx pin.

In LEDCTRLx_MD[1:0] transition from 'Ignored' to 'Inverted', the LEDCTRLx pin state is synchronized immediately.

When BUCKx_DIM_FADEIN[2:0]=0, the LEDCTRLx pin state is synchronized immediately after LEDCTRLx_MD[1:0] transition from 'Ignored' to 'Normal'.

Buck Diagnostic Description

- *Open LEDx String*: individual open LED diagnostic flags indicate whether the "x" string is detected open. The detection is based on a counter overflow of typical 50 μs when the related channel is activated. BUCKx_OPENLED flags (non-latched) are contained in status registers 0x21 and 0x28. Please note that the open detection does not disable the buck channel(s).

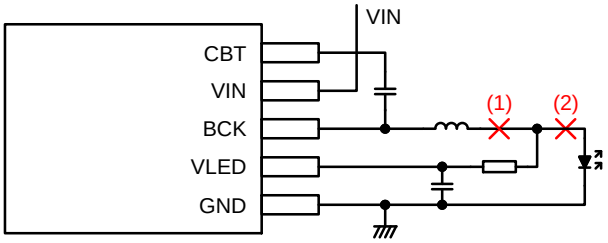


Figure 37. OPENLED Failure

- *Short LEDx String*: a short circuit detection is available independently for each LED channel per means of the flag BUCKx_SHORTLED (non-latched, status registers 0x21 and 0x28). The detection is based on the voltage measured at the VLEDx pins via a dedicated internal comparator: when the voltage drops below the VLEDLOW threshold (typical 1.0 V) the related flag is set. Note that the detection is inactive during first 5, 1, 10 (defined by BUCKx_SHORTLED_MASK[1:0]) switching periods after Buck regulation start. SHORTLED detection is disabled when BUCKx_SHORTLED_MASK[1:0] = 3.

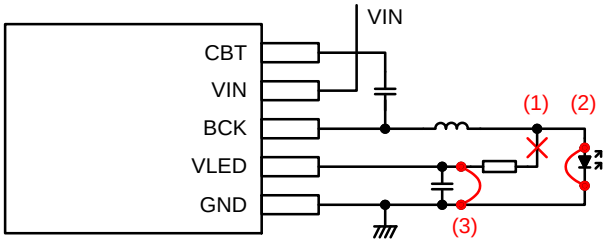


Figure 38. SHORTLED Failure

Table 21. INTERNAL PWM DIMMING PROGRAMMABLE FREQUENCIES

BUCKx_SHORTLED_MASK [1:0]	SHORTLED Detection Masked (After Buck Regulation Start)
0	During first 5 periods
1	During first period
2	During first 10 periods
3	SHORTLED detection disabled

- *LEDx Overcurrent*: being a current regulator, the NCV78964 buck is by nature preventing overcurrent in all normal situations. However, in order to protect LEDx and the buck channel x electronics from overcurrent even in case of failures, protection mechanism is available. It is based on monitoring of 8 consecutive buck periods with

min Ton time. As the overcurrent is detected, the Buck channel is switched off and corresponding SPI error flag BUCKx_OVLD (latched, status registers 0x21 and 0x28) is raised. Buck is kept continuously off until next re-enabling of the channel, what can be done by writing BUCKx_EN SPI signal to 0 followed by writing the BUCKx_EN to 1. After re-enabling, the Buck will try to regulate the current again. SPI error flag BUCKx_OVLD can be cleared by reading out corresponding register after channel was disabled by writing BUCKx_EN to 0.

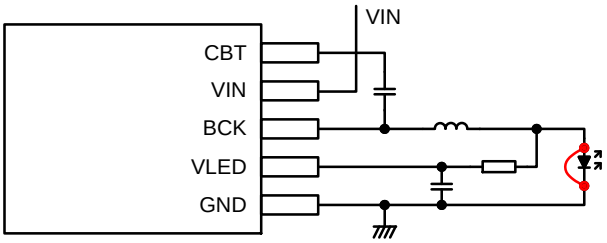


Figure 39. LED Overcurrent Failure

Automatic recovery feature is available for BUCKx_OVLD protection. This can be especially useful in FSO/Stand alone mode. The feature is controlled for both protections by common register BUCKx_RCVR[1:0] according to table below:

Table 22. AUTOMATIC RECOVERY FOR BUCKX_OVLD PROTECTION

BUCKx_RCVR [1:0]	Time between Attempts (ms)	# of Attempts
0	Auto-recovery OFF	0
1	8	3
2	65	3
3	65	Infinity

- *Short on the BCK node/Buck switch overload*: this protection is based on sensing of the voltage drop over the top switch just after the switch-on sequence and comparing it with maximum allowed threshold. Buck output goes off and corresponding SPI error flag BUCKx_OVLD (latched, status registers 0x21 and 0x28) is raised after the overload situation in detected for two consecutive buck periods. Buck is kept continuously off until next re-enabling of the channel, what can be done by writing BUCKx_EN SPI signal to 0 followed by writing the BUCKx_EN to 1. After re-enabling, the Buck will try to regulate the current again. SPI error flag BUCKx_OVLD can be cleared by reading out corresponding register after channel was disabled by writing BUCKx_EN to 0.

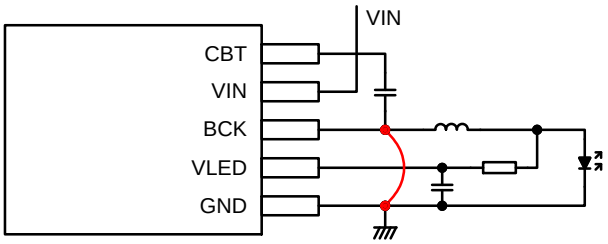


Figure 40. Buck Switch Overload Failure

Automatic recovery feature is available for BUCKx_OVLD protection as summarized by Table 22.

- *Undervoltage/Reset on floating domain*: this protection monitor whether the voltage on CBT capacitor is sufficient to guarantee proper operation of floating domain circuits. If drop of the voltage below VPOROFF (see Table 6 “BUCK REGULATOR − CBT RECHARGE CIRCUIT”) is detected, the Buck is disabled and corresponding SPI error flag BUCKx_CBT_UV (non-latched, status registers 0x21 and 0x28) is raised.

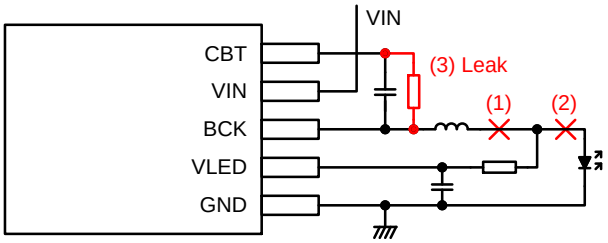


Figure 41. CBT_UV Protection

- *Overvoltage on CBT domain*: this protection mechanism monitors whether voltage on CBT capacitor is not too high to guarantee correct operation. In case the voltage exceeds CBTOV threshold (see Table 6 “BUCK REGULATOR − CBT RECHARGE CIRCUIT”), the Buck is disabled and corresponding SPI error flag BUCK_CBT_OV (latched, status registers 0x21 and 0x28) is raised.

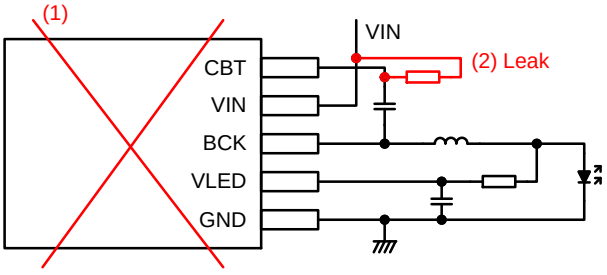


Figure 42. CBT_OV Failure

- *Buckx Running at Minimum TON Time*: registers BUCKx_MIN_TON (latched, status registers 0x21 and 0x28) indicate that minimal TON time is detected on the corresponding channel. TON time is so short that neither Average nor Peak current comparison could be reliably performed and as a result the output current is not in regulation and under the control by Buck regulator. BUCKx_MIN_TON is clear by read flag.
- *Buckx Zero Cross Event detection*: registers BUCKx_ZCDMODE (status registers 0x21 and 0x28) indicate that Zero Cross event was detected by Zero Cross detector.
- *Buckx Status*: registers BUCKx_RUNNING (non-latched, status registers 0x21 and 0x28) show the actual status of Buckx output. When BUCKx_RUNNING is 1, the corresponding output regulates current to the LED.
- *Buck switch local thermal shutdown*: registers BUCKx_TSD (latched, status registers 0x21 and 0x28) indicate that the local temperature of the Buck switch exceeded allowed threshold. The Buck switch thermal shutdown level is not user programmable and is factory trimmed (see BUCKTSD in Table 6 “ADC FOR MEASURING VIN1, VIN2, VBST, VCC, VDRV, VINT, VLED1, VLED2, TEMP”). This protection is implemented to protect the Buck power switch from too high temperature, which however impacts only its Ron resistance. Other analog blocks are at much lower temperature due to temperature gradient. Buck outputs are re-enabled automatically if BUCKx_TSD_RCVR = 1 when temperature drops below THERMAL_WARNING_THR[8:0] threshold, respectively can be re-enabled by rising edge on BUCKx_EN if BUCKx_TSD_RCVR = 0.
- *LEDCTRLx Pin Monitor*: registers LEDCTRLx_MON[1:0] (latched, status registers 0x21 and 0x28) indicate the actual logic level of the debounced LEDCTRLx pins. These signals follow the output of 250 ns digital debouncers implemented on LEDCTRLx pins. LEDCTRLx_MON[0] is set when “log. 0” on LEDCTRLx pin is detected. LEDCTRLx_MON[1] is set when “log. 1” on LEDCTRLx pin is detected. These flags are latched and stay set until they are cleared by reading of appropriate register. By this mean it is also possible to detect e.g. PWM dimming.
- *Buckx TOFF Monitor*: registers BUCKx_TOFF_MON[6:0] (status registers 0x22 and 0x29) monitor actual regulated or set $T_{OFF} \cdot V_{COIL}$ parameter (physically corresponding to inductor current ripple).
- *TOFF Monitor Updated*: registers BUCKx_TOFF_UPD (latched, status registers 0x22 and 0x29) inform, that corresponding BUCKx_TOFF_MON[6:0] register was updated with actual measurement result. BUCKx_TOFF_UPD is clear by read flag.
- *Regulated IRIP value*: registers BUCKx_IRIP[8:0] (status registers 0x22 and 0x29) provides information about “$I_{BUCK_{peak}} - I_{BUCK_{AVG}}$” value regulated by internal algorithm for average current regulation.
- *IRIP Updated*: registers BUCKx_IRIP_UPD (latched, status registers 0x22 and 0x29) inform, that corresponding BUCKx_IRIP[8:0] register was updated with actual measurement result. Update should happen at each Buck period end. BUCKx_IRIP_UPD is clear by read flag.
- *Buckx TOFF Time Duration*: registers BUCKx_TOFF_DUR[9:0] (status registers 0x25 and 0x2C) reflect the last measured Buckx TOFF time (1LSB = 62.5 ns) on the corresponding channel.
- *Buckx TON Time Duration*: registers BUCKx_TON_DUR[9:0] (status registers 0x25 and 0x2C) reflect the last measured Buckx TON time (1LSB = 62.5 ns) on the corresponding channel. Maximum value is 800 (corresponds to 50 μs). When Buckx runs with TON time < typ. 62.5 ns, the BUCKx_TON_DUR[9:0] SPI register returns value 0x0. When Buckx is stopped, the BUCKx_TON_DUR[9:0] register keeps the last measured TON time.
- *TOFF and TON Times Updated*: registers BUCKx_T_UPD (latched, status registers 0x25 and 0x2C) inform, that corresponding BUCKx_TOFF_DUR[9:0] and BUCKx_TON_DUR[9:0] registers were updated with actual measurement result. BUCKx_T_UPD is clear by read flag.
- *Icoil*: registers BUCKx_ICOIL[7:0] (status registers 0x26 and 0x2D) reflect actual value of Average current. It is calculated as BUCKx_IAVG_DAC[8:0] x *BUCKx_ICOIL_RAT* (ratio of the time when current is flowing through the coil and time of Buck period). In continuous current mode (where current does not drop to zero and is flowing through the coil whole Buck period), the *BUCKx_ICOIL_RAT* is 1. When Buck runs in BCM or DCM mode, the *BUCKx_ICOIL_RAT* will contain values from 0 to 1 according to detected ratio.
- *Icoil Updated*: registers BUCKx_ICOIL_UPD (latched, status registers 0x26 and 0x2D) inform, that corresponding BUCKx_ICOIL[7:0] register was updated with actual measurement result. BUCKx_ICOIL_UPD is clear by read flag.
- *IAVG DAC*: registers BUCKx_IAVG_DAC[8:0] (status registers 0x27 and 0x2E) reflect value of internal IAVG register after calibration with actual measured temperature VTEMP
- *IRIP DAC*: registers BUCKx_IRIP_DAC[8:0] (status registers 0x27 and 0x2E) reflect value of internal IRIP register after calibration with actual measured temperature VTEMP

A short summary table of the main diagnostic bits related to the LED outputs follows.

Table 23. LED OUTPUTS DIAGNOSTIC SUMMARY

Diagnose		Detection Level	LED Output	Latched
Flag	**Description**			
SPIERR	SPI error	See SPI section	Not Disabled	Yes
TW	Thermal Warning	SPI register programmable	Not Disabled (if no TSD or BUCKx_TSD, otherwise disabled)	Yes
TSD	Thermal Shutdown	Factory trimmed	Disabled (automatically re-enabled when temp falls below TW and BUCKx_TSD_ RCVR = 1)	Yes
BUCKx_TSD	Buck Switch Local Thermal Shutdown	Factory trimmed	Disabled (automatically re-enabled when temp falls below TW and BUCKx_TSD_ RCVR = 1)	Yes
BUCKx_OPENLED	Open LED string	Buck on time > 50 μs	Not Disabled	No
BUCKx_SHORTLED	Shorted LED string	VLEDx < VLEDLOW	Not Disabled	No
BUCKx_OVLD	LED string overcurrent	8 consecutive periods with min Ton time	Disabled Automatic recovery available by means of BUCKx_RCVR [1:0]	Yes
	Buck switch overload	2 consecutive periods above overload threshold	Disabled Automatic recovery available by means of BUCKx_RCVR [1:0]	Yes
BUCKx_CBT_UV	CBT domain reset	VCBTx < VPOROFF	Disabled	No
BUCKx_CBT_OV	CBT domain overvoltage	VCBTx > CBTOV	Disabled	Yes
BUCKx_MIN_TON	Buck minimum Ton time	Min Ton time detected	Not disabled	Yes

General Diagnostic Description

- *Thermal Warning*: this mechanism detects a user-programmable junction temperature which is in principle close, but lower, to the chip maximum allowed, thus providing the information that some action (power de-rating) is required to prevent overheating that would cause Thermal Shutdown. A typical power de-rating technique consists in reducing the output dimming duty cycle in function of the temperature: the higher the temperature above the thermal warning, the lower the duty cycle. The thermal warning flag (TW) is given in status register 0x20 and is latched. When VTEMP[8:0] raises to or above THERMAL_WARNING_THR[8:0] threshold, the TW flag is set. At power up the default thermal warning threshold is typically 150 °C (20 codes below TSD level).
- *Thermal Shutdown*: this safety mechanism intends to protect the device from damage caused by overheating, by disabling both buck channels and booster. The diagnostic is displayed per means of the TSD bit in status register 0x20 (latched). Once occurred, the thermal shutdown condition is exited when the temperature drops below the thermal warning level, thus providing hysteresis for thermal shutdown recovery process. Buck outputs are re-enabled automatically if BUCKx_TSD_RCVR = 1 when temperature drops below THERMAL_WARNING_THR[8:0] threshold, respectively can be re-enabled by rising edge on BUCKx_EN if BUCKx_TSD_RCVR = 0. Booster is re-enabled automatically once thermal shutdown condition is exited. The application thermal design should be made as such to avoid the thermal shutdown in the worst case conditions. The thermal shutdown level is not user programmable and is factory trimmed (see ADC_TSD in Table 6 “ADC FOR MEASURING VIN1, VIN2, VBST, VCC, VDRV, VINT, VLED1, VLED2, TEMP”).
- *SPI Error*: in case of SPI communication errors the SPIERR bit in status register 0x20 is set. The bit is latched. For more details, please refer to section “SPI Framing Error”.
- *EEPROM Error*: in case of read or write error during manipulation with EEPROM memory, the EEPROMERR bit in status register 0x20 is set. EEPROMERR is logical OR of EEPROM_WRITEFAIL and EEPROM_READFAIL errors.
- *Trimming Error*: TRIMERR bit in status register 0x20 is set when CRC_EEPROM_TRIM error is detected.
- *Command Reject*: CMD_REJECT bit in status register 0x20 is set when any EEPROM operation or write into EEPROM_DATA_WRITE[19:0] register is not accepted or when trial to write into SPI registers (except SWRESET, FSO_ENTER, FSO_EXIT, FSO_WDG_ENA[1:0] and FSO_WDG_CFG[1:0]) in FSO mode is made and rejected.
- *HW Reset*: the out of reset condition is reported through the HWR bit (latched, status register 0x20). This bit is set after each Power On Reset (POR) or SW reset (by SWRESET bit) and indicates the device is ready to operate.

- FSO Mode: presence in FSO mode is reported through the FSO bit in status register 0x20.
- *Frame Counter*: when valid SPI frame is received by the device, the register FRAME_CNT[3:0] (status register 0x20) is incremented. When actual value of the counter is 15, it will overflow to 0 after next valid SPI frame is received.
- *CSB Duration*: register CSB_DUR[19:0] (status registers 0x3D) reflects the last measured duration of CSB low pulse. CSB low pulse will be measured even in case of invalid SPI frame. Resolution of the register is 1LSB = 62.5 ns. If CSB low pulse is longer than maximum what can be held by CSB_DUR[19:0] register (~65.5 ms), the register will keep maximum value.

Functional Mode Description

Overview of all functional modes is in accordance to the state diagram on Figure 43. Individual states are described below.

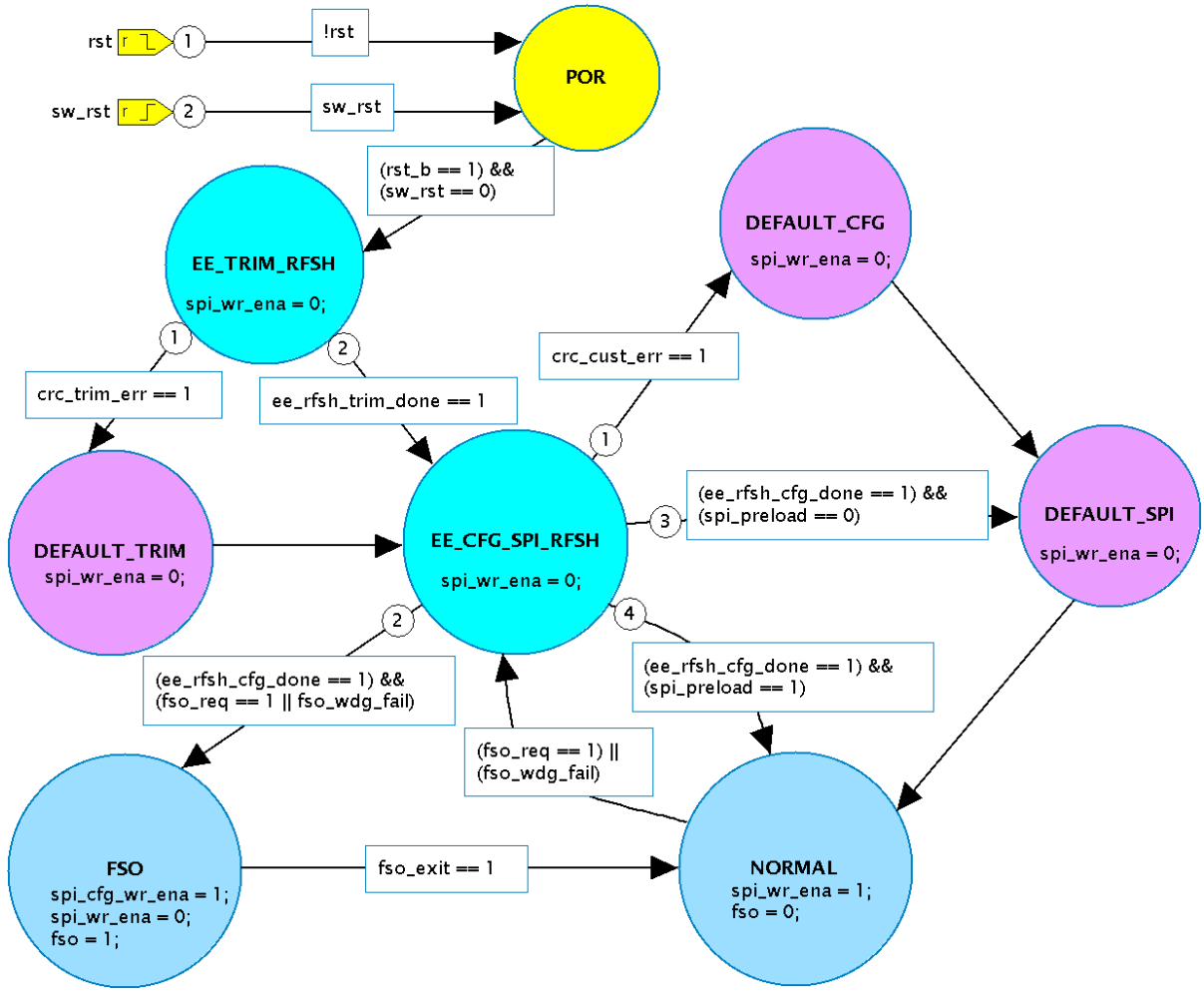


Figure 43. Functional Modes State Diagram

Reset

Asynchronous reset is caused either by POR (POR always causes asynchronous reset − transition to reset state) or by SWRESET SPI bit being written to 1.

Init and Normal Mode/FSO Mode

After the Reset, Trimming and Calibration constants are loaded from EEPROM into shadow registers and CRC check is performed. CRC check of trimming and calibration constants in shadow registers is performed also after each VTEMP measurement.

When EEPROM preload and CRC check of trimming constants in shadow registers fails also after the second trial, the CRC_EEPROM_TRIM (trimming data CRC check) error is raised and default trimming values are loaded into trimming shadow registers.

Calibration data are preloaded into shadow registers and CRC check is performed also after change of BUCKx_IRNG[1:0] SPI register.

When CRC_EEPROM_TRIM (trimming data CRC check) error is detected, SPI flag TRIMERR at address 0x20 is set to 1.

Configuration registers FSO_ENTER, FSO_WDG_ENA[1:0] and FSO_WDG_CFG[1:0] are loaded from EEPROM into SPI registers after the reset before entrance into FSO or Normal mode.

SPI bit FSO_ENTER controls entrance into FSO mode; if register value is 1, FSO mode will be entered, otherwise Normal mode will be entered.

Configuration register SPI_PRELOAD (EEPROM address 0x11), which is loaded from EEPROM after the reset, controls whether in Normal mode SPI registers will be loaded with values from EEPROM (addresses from 0x11 to 0x1B) or with default SPI values. When SPI_PRELOAD is 1, SPI registers will be preloaded from EEPROM and this mode can be referred as Stand-Alone mode.

Customer EEPROM data are protected by CRC_EEPROM_CUST CRC check. When CRC_EEPROM_CUST (customer data CRC check) error is detected, SPI register EEPROM_READFAIL is set to 1 and default values will be loaded into SPI control registers.

Fail-Safe Operation Mode

FSO (Fail-Safe Operation) mode can be used for the purpose of **Fail-Safe** functionality (chip functionality definition in fail-safe mode when the external microcontroller functionality is not guaranteed).

FSO mode is entered in the following situations:

- After POR when control registers are preloaded and FSO_ENTER contains 1,
- From Normal mode when rising edge on FSO_ENTER SPI bit is detected and at the same moment SPI bit FSO_EXIT is 0,
- From Normal mode when Watchdog time-out elapses (indicated by FSO_WDG_FAIL).

When transitioning into FSO mode, the EEPROM refresh is performed. Please note, that when CRC error has been detected, SPI register EEPROM_READFAIL is set to 1, FSO mode is not entered and default values are loaded into SPI registers.

FSO mode can be exited when rising edge on FSO_EXIT SPI bit is detected and at the same moment SPI bit FSO_ENTER is 0.

FSO bit in status register 0x20 (and its mirror in SPI frame) is set to 1 when device is inside the FSO mode. FSO status bit is 0 outside the FSO mode.

In FSO mode write operations are allowed to SWRESET, FSO_ENTER, FSO_EXIT, FSO_WDG_ENA[1:0] and FSO_WDG_CFG[1:0] control registers at address 0x1D.

Stand-Alone Mode

Stand-Alone modes can be used for the purpose of default power-up operation of the chip (**Stand-Alone** functionality without external microcontroller or preloading of the registers with default content for default operation before microcontroller starts sending SPI commands for chip settings).

Stand-Alone mode is in fact Normal mode where SPI registers were preloaded from EEPROM after the reset and is entered in the following situation:

- After POR when configuration register SPI_PRELOAD, which is loaded from EEPROM, contains 1.

During SPI preload, the EEPROM refresh is performed. Please note, that when CRC error has been detected, SPI register EEPROM_READFAIL is set to 1 and default values are loaded into SPI registers.

FSO Watchdog

Watchdog is restarted each time the valid SPI frame is received. When Watchdog is not properly restarted and time-out elapses, transition into FSO mode is started.

The watchdog can be configured and activated according to Table 24:

Table 24. WATCHDOG MODES

FSO_WDG_ENA [1:0]	Description
0	Watchdog disabled
1	Watchdog enabled after the first valid SPI frame
2	Watchdog enabled after NORMAL mode entrance
3	Watchdog enabled after NORMAL mode entrance with timeout 258.048 ±4.096 ms until the first valid SPI frame

FSO_WDG_CFG[1:0] control register defines the watchdog time-out:

Table 25. WATCHDOG TIME-OUT

FSO_WDG_CFG [1:0]	Min Timeout (ms)	Max Timeout (ms)
0	24.576	32.768
1	57.344	65.536
2	122.880	131.072
3	253.952	262.144

Failure Output

SDO pin can be used as failure indicator (active low) when at least one of the SPI bits BST_FAIL_OUT, BUCK1_FAIL_OUT or BUCK2_FAIL_OUT at address 0x1D is set to 1.

SDO output will be asserted low when the following condition persists for more than 49 ms:
not SDO = (CSB pin = 1) and (*BCK1ERR* and *buck1_active* and BUCK1_FAIL_OUT) or (*BCK2ERR* and *buck2_active* and BUCK2_FAIL_OUT) or (*BSTERR* and BST_FAIL_OUT)

Please note that *BCK1ERR*, *BCK2ERR* and *BSTERR* are used also in SPI read frame in FAILURE_FLAGS[5:0] section, please see SPI Read Frame description for more details.

Meaning of the *BCK1ERR*, *BCK2ERR* and *BSTERR* is the following:

BUCKxERR = BUCKx_OVLD or *BUCKx_CBT_UV_DEB* or BUCKx_TSD or TSD or (BUCKx_OPENLED and BUCKx_OPENLED_FMASK) or (BUCKx_SHORTLED and BUCKx_SHORTLED_FMASK) or (BUCKx_REGSTATUS = 1 and BUCKx_REGFAIL_FMASK),
where *BUCKx_CBT_UV_DEB* is set when BUCKx_CBT_UV lasts 500 ms and more

BSTERR = (not BST1_RUNNING and BST1_EN) or (not BST2_RUNNING and BST2_EN) or TSD or ((BSTx_REGSTATUS = 1 or BSTx_REGSTATUS = 2) and BST_ILIM_FMASK)

Meaning of the *buck1_active* and *buck2 active* is the following:

buckx_active = BUCKx_EN and ((LEDCTRLx pin xor LEDCTRLx_MD[0]) or LEDCTRLx_MD[1])

SPI INTERFACE

General

The serial peripheral interface (SPI) is used to allow an external microcontroller (MCU) to communicate with the device. NCV78964 acts always as a slave and it cannot initiate any transmission. The operation of the device is configured and controlled by means of SPI registers, which are observable for read and/or write from the master. The NCV78964 SPI transfer size is 32 bits. Maximum communication SPI speed supported by NCV78964 is 4 MHz.

During an SPI transfer, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines: DO and DI. The DO signal is the output from the Slave (NCV78964), and the DI signal is the output from the Master.

A slave or chip select line (CSB) allows individual selection of a slave SPI device in a time multiplexed multiple-slave system.

The CSB line is active low. If an NCV78964 is not selected, DO is in high impedance state and it does not interfere with SPI bus activities. When the CSB line is low, the DO output is configured as push-pull to support higher communication speeds.

Since the NCV78964 always clocks data out on the falling edge and samples data in on rising edge of clock, the MCU SPI port must be configured to match this operation.

The implemented SPI allows connection to multiple slaves by means of star connection (CSB per slave.

An SPI star connection requires a bus = (3 + N) total lines, where N is the number of Slaves used, the SPI frame length is 32 bits per communication.

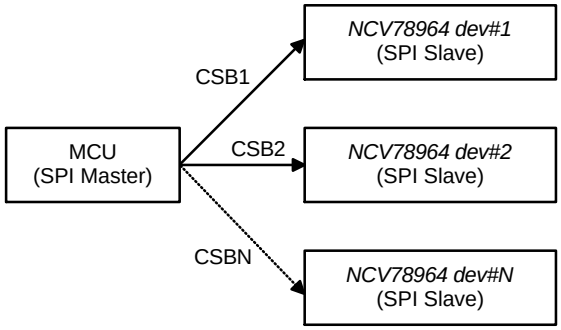


Figure 44. SPI Star Connection

SPI Transfer Format

Two types of SPI commands (to DI pin of NCV78964) from the micro controller can be distinguished: “Write to a control register” and “Read from register (control or status)”.

The frame protocol for the *write operation*:

Bits	[31]	[30:25]	[24:4]	[3:0]
SDI data	CMD	WRITE_ADDR[5:0]	WRITE_DATA[20:0]	CRC[3:0]
SDO data	SPIERR	LAST_ADDR[5:0]	LAST_DATA[20:0]	ECRC[3:0]

Figure 45. SPI Write Frame

Referring to the previous picture, the write frame coming from the master (into the DI) is composed from the following fields:

- Bit[31] (MSB): CMD bit = 1 for write operation,
- Bits[30:25]: 6 bits WRITE ADDRESS field,
- Bits[24:4]: 21 bit DATA to write,
- Bits[3:0]: CRC field computed over CMD, WRITE_ADDR and WRITE_DATA in shown order from MSB to LSB.

Device in the same time replies to the master (on the DO):

- Bit[31] (MSB): SPI ERROR bit set in case last received SPI frame was invalid,
- Bits[30:25]: 6 bit ADDRESS (WRITE_ADDR or READ_ADDR) transmitted in previous valid SPI frame,
- Bits[24:4]: 21 bit actual DATA stored on address LAST_ADDR,
- Bits[3:0]: ECRC (extended CRC) computed over SPIERR, LAST_DATA, LAST_ADDR, CMD (which has to be extended to 2 bits by one zero from left) and WRITE_ADDR in shown order from MSB to LSB.

In case the write operation is the first frame after power-on-reset, address of NOP register is used as LAST_ADDR.

If CRC in the frame is wrong, device will not perform command and <SPIERR> flag will be set.

The frame protocol for the *read operation*:

Bits	[31]	[30:25]						[24:4]	[3:0]
SDI data	CMD	READ_ADDR[5:0]						IGNORED[20:0]	CRC[3:0]
SDO data	SPIERR	FAILURE_FLAGS[5:0]						READ_DATA[20:0]	ECRC[3:0]
		HWR	TW	FSO	BCK1ERR	BCK2ERR	BSTERR		

Figure 46. SPI Read Frame

Referring to the previous picture, the read frame coming from the master (into the DI) is composed from the following fields:

- Bit[31] (MSB): CMD bit = 0 for read operation,
- Bits[30:25]: 6 bits READ ADDRESS field,
- Bits[24:4]: 21 bits zeroes field,
- Bits[3:0]: 4 bits CRC field computed over CMD, READ_ADDR and IGNORED in shown order from MSB to LSB.

Device in the same frame provides to the master (on the DO):

- Bit[31] (MSB): SPI ERROR bit set in case last received SPI frame was invalid,
- Bits[30:25]: FAILURE_FLAGS[5:0] field composed from:
  - HWR flag (mirror of HWR SPI flag),
  - TW flag (mirror of TW SPI flag),
  - FSO flag (mirror of FSO SPI flag),
  - BCK1ERR fail status,
  - BCK2ERR fail status,
  - BSTERR fail status; please see Failure Output chapter to see details from which bits these fail status indicators are composed,
- Bits[24:4]: actual data from address READ_ADDR,
- Bits[3:0]: ECRC (extended CRC) computed over SPIERR, FAILURE_FLAGS, READ_DATA, CMD (which has to be extended to 2 bits by one zero from left) and READ_ADDR in shown order from MSB to LSB.

Read frame provides data from the required address to the output within the same frame (in frame response), thus achieving the lowest communication latency.

CRC Calculation

Received and transmitted frames are protected by CRC with following parameters:

- CRC length is 4 bits,
- CRC polynomial 0x9 (Koopman's notation; x4+x+1),
- CRC initialization value 0xF.

SPI Framing Error

SPI communication framing error is detected by the NCV78964 in the following situations:

- Not zero or 32 CLK pulses are received during the active-low CSB signal;
- CRC calculated from all received bits is not equal to zero;
- Write operation to read only register was performed.

Once an SPI error occurs, the <SPIERR> flag can be reset only by reading the status register in which it is contained by valid SPI frame.

Each read-only register has parity bit on its MSB position. The value of this bit is calculated as odd parity over register data together with register address. Parity bit should be used by external MCU to validate whether data were read from the requested SPI address.

CRC Code Example

```
#include <stdint.h>

// Calculates 4 bit CRC from given data array "data" and data byte count "length". Returns 4 bit CRC value
uint8_t CalcCRCfromByteArray(uint8_t* data, uint8_t length) {
    static const uint8_t CRC_POLY = 0x03;   // Polynomial x^4 + x + 1 (0x03 Normal representation, 0x09 Koopman)
    static const uint8_t CRC_INIT = 0x0F;   // Initialization value

    uint8_t crc = 0;                        // CRC register
    uint8_t bit = 0;                        // Bit to be shifted into CRC register

    // Begin CRC calculation byte by byte
    for(uint8_t byteIdx = 0; byteIdx < length; byteIdx++) {
        if(byteIdx == 0) {
            // Initialize CRC register - Shift in the first 4 highest bits (starting from CMD),
            for(int8_t bitIdx = 7; bitIdx >= 4; bitIdx--) {
                bit = (data[byteIdx] >> bitIdx) & 0x01;
                crc = (crc << 1) | bit;
            }
            crc ^= CRC_INIT;                // XOR with CRC initial value
        }

        // Continue from bit 3...0 after Init in case of First byte is processed
        // Else process all 8 bits (7...0) of given byte
        for (int8_t bitIdx = (byteIdx == 0 ? 3 : 7); bitIdx >= 0; bitIdx--) {
            bit = (data[byteIdx] >> bitIdx) & 0x01;
            crc = (crc << 1) | bit;
            if (crc & 0x10) {               // Check CRC register popout bit
                crc ^= CRC_POLY;
            }
        }
    }

    return (crc & 0x0F);                    // Return CRC - only the lower 4 bits
}

// CRC Calculation from masterOUT message
uint8_t CalcCRC(uint32_t masterOUT) {
    // Create data byte array with expected structure for CRC calculation
    uint8_t data[4] = {0};                  // 4 data bytes
    data[0] = (masterOUT >> 24) & 0xFF;     // Bits 31...24 (31 = CMD)
    data[1] = (masterOUT >> 16) & 0xFF;     // Bits 23...16 (23 = write_data/ignored[19])
    data[2] = (masterOUT >> 8) & 0xFF;      // Bits 15...8 (15 = write_data/ignored[11])
    data[3] = masterOUT & 0xF0;             // Bits 7...4   (7 = write_data/ignored[3])
                                            // Bits 3...0   (CRC padding = 0)
    return CalcCRCfromByteArray(data, 4);
}

// ECRC Calculation from device response (masterIN) and part of masterOUT message
uint8_t CalcECRC(uint32_t masterOUT, uint32_t masterIN) {
    // Create data byte array with expected structure for CRC calculation
    uint8_t data[5] = {0};                  // 5 data bytes
    data[0] = (masterIN >> 24) & 0xFF;      // Bits 39...32 (39 = SPIERR)
    data[1] = (masterIN >> 16) & 0xFF;      // Bits 31...24 (31 = last_/read_data[19])
    data[2] = (masterIN >> 8) & 0xFF;       // Bits 23...16 (23 = last_/read_data[11])
    data[3] = (masterIN & 0xF0) |           // Bits 15...12 (last_/read_data[3]...last_/read_data[0])
              (masterOUT >> 29) & 0x07;     // Bits 11...8  (11 = 0 (extended CMD), 10 = CMD)
    data[4] = ((masterOUT >> 25) & 0x0F) << 4;  // Bits 7...4   (write_/read_addr[3]...[0])
                                            // Bits 3...0   (ECRC calculation padding = 0)
    return CalcCRCfromByteArray(data, 5);
}

//*****************************************************************************//
// Example CRC/ECRC calculation - Read Register 0x3F (REVID) after device power up
// ...
uint32_t masterOUT = 0x7e000000;  // Master out message (CMD = 0; read_addr = 0x3F, CRC = 0 [placeholder])
uint8_t crc = CalcCRC(masterOUT); // Expected CRC result = 0x4
masterOUT |= (crc & 0x0F);        // Set lowest 4 bits to calculated CRC value (masterOUT = 0x7e000004)

// Write data to SPI while reading device in frame response (into masterIN variable)
uint32_t masterIN = spiTransfer(masterOUT);

// Expected  response of NCV78964 (0x40001087) - HWR set; REVID = 0x108; ECRC = 0x7

uint8_t ecrc_response = (masterIN & 0x0F);         // Read lowest 4 bits of response - ECRC
uint8_t ecrc_calc = CalcECRC(masterOUT, masterIN); // Check ECRC validity (should match response ECRC)

if(ecrc_calc != ecrc_response) {
        // ...Handle ECRC error
}
// ...Process Device Response
// ...
```

SPI ADDRESS MAP

	ADDR	bit20	bit19	bit18	bit17	bit16	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0x00	NOP[20:0]																				
1	0x01	BUCK1_DCM_CORR[2:0]			BUCK1_ZCD_DIS	BUCK1_TOFF[6:0]							BUCK1_IRNG[1:0]		BUCK1_IAVG[7:0]							
2	0x02		BUCK1_TSD_RCVR	BUCK1_RCVR[1:0]		BUCK1_SHORTLED_MASK[1:0]		VLED1_RNG	BUCK1_IREG_PAUSE	BUCK1_FREQ_PAUSE	BUCK1_FREQ_RATE[1:0]		BUCK1_FREQ_RSP[1:0]	BUCK1_FREQ_FAST_RCVR	BUCK1_FREQ_ABOVE				BUCK1_FREQ[5:0]		
3	0x03					BUCK1_DIM_SHIFT		BUCK1_DIM_FADEOUT[2:0]		BUCK1_DIM_FADEIN[2:0]				BUCK1_DIM_DUTY[7:0]							LEDCTRL1_MD[1:0]	
4	0x04																			BUCK1_REGFAIL_FMASK	BUCK1_OPENLED_FMASK	BUCK1_SHORTLED_FMASK
5	0x05	BUCK2_DCM_CORR[2:0]			BUCK2_ZCD_DIS	BUCK2_TOFF[6:0]							BUCK2_IRNG[1:0]		BUCK2_IAVG[7:0]							
6	0x06		BUCK2_TSD_RCVR	BUCK2_RCVR[1:0]		BUCK2_SHORTLED_MASK[1:0]		VLED2_RNG	BUCK2_IREG_PAUSE	BUCK2_FREQ_PAUSE	BUCK2_FREQ_RATE[1:0]		BUCK2_FREQ_RSP[1:0]	BUCK2_FREQ_FAST_RCVR	BUCK2_FREQ_ABOVE				BUCK2_FREQ[5:0]		
7	0x07					BUCK2_DIM_SHIFT		BUCK2_DIM_FADEOUT[2:0]		BUCK2_DIM_FADEIN[2:0]				BUCK2_DIM_DUTY[7:0]							LEDCTRL2_MD[1:0]	
8	0x08																			BUCK2_REGFAIL_FMASK	BUCK2_OPENLED_FMASK	BUCK2_SHORTLED_FMASK
9	0x09																					
10	0x0A																					
11	0x0B																					
12	0x0C																					
13	0x0D																	BUCK_DIM_FREQ[1:0]			BUCK2_EN	BUCK1_EN
14	0x0E								BST1_SLP_CTRL[2:0]			BST1_COMP_DIV[2:0]		BST1_VLIM_THR[7:0]								
15	0x0F								BST2_SLP_CTRL[2:0]			BST2_COMP_DIV[2:0]		BST2_VLIM_THR[7:0]								
16	0x10																					
17	0x11	BST_IUM_FMASK	VDRV_UV_RCVR	VDRV_UV_THR[2:0]			BST_OTA_GAIN[1:0]		BST_MIN_TON[1:0]		BST_MIN_TOFF[2:0]			BST_SRC_FREQ[4:0]					BST_SRC_DIV	BST_SRC_INV	BST_SRC[1:0]	
18	0x12	BST_SKCL_THR[1:0]		BST_SOFTSTART_UV		BST_SOFTSTART[2:0]		BST_OV_REACT[1:0]		BST_OV_SD[2:0]				BST_VSETPOINT[6:0]							BST2_EN	BST1_EN
19	0x13																					
20	0x14																					
21	0x15																					
22	0x16																					
23	0x17																					
24	0x18																					
25	0x19																					
26	0x1A								OSC_CAL[4:0]					THERMAL_WARNING_THR[8:0]								
27	0x1B	EEPROM_DATA_WRITE[19:0]																				
28	0x1C												EEPROM_ADDRESS[4:0]						EEPROM_CTRL[3:0]			
29	0x1D												BST_FAIL_OUT	BUCK2_FAIL_OUT	BUCK1_FAIL_OUT	FSO_WDG_CFG[1:0]		FSO_WDG_ENA[1:0]	FSO_EXIT	FSO_ENTER	SWRESET	
30	0x1E																					
31	0x1F																					
32	0x20										TRIMERR	EEPROMERR	SPIERR	CMD_REJECT	FRAME_CNT[3:0]				TSD	TW	FSO	HWR
33	0x21								BUCK1_TSD	BUCK1_CBT_OV	BUCK1_CBT_UV	BUCK1_OPENLED	BUCK1_SHORTLED	BUCK1_OVLD	BUCK1_MIN_TON	BUCK1_ZCDMODE	LEDCTRL1_MON[1:0]		BUCK1_DIM_FADE	BUCK1_REGSTATUS[1:0]		BUCK1_RUNNING
34	0x22			BUCK1_TOFF_UPD	BUCK1_TOFF_MON[6:0]								BUCK1_IRIP_UPD	BUCK1_IRIP[8:0]								
35	0x23			VIN1[8:0]										VLED1[8:0]								
36	0x24			VLED1ON[8:0]										VLED1OFF[8:0]								
37	0x25	BUCK1_T_UPD	BUCK1_TOFF_DUR[9:0]											BUCK1_TON_DUR[9:0]								
38	0x26													BUCK1_ICOIL_UPD	BUCK1_ICOIL[7:0]							
39	0x27			BUCK1_IAVG_DAC[8:0]										BUCK1_IRIP_DAC[8:0]								
40	0x28								BUCK2_TSD	BUCK2_CBT_OV	BUCK2_CBT_UV	BUCK2_OPENLED	BUCK2_SHORTLED	BUCK2_OVLD	BUCK2_MIN_TON	BUCK2_ZCDMODE	LEDCTRL2_MON[1:0]		BUCK2_DIM_FADE	BUCK2_REGSTATUS[1:0]		BUCK2_RUNNING
41	0x29			BUCK2_TOFF_UPD	BUCK2_TOFF_MON[6:0]								BUCK2_IRIP_UPD	BUCK2_IRIP[8:0]								
42	0x2A			VIN2[8:0]										VLED2[8:0]								
43	0x2B			VLED2ON[8:0]										VLED2OFF[8:0]								
44	0x2C	BUCK2_T_UPD	BUCK2_TOFF_DUR[9:0]											BUCK2_TON_DUR[9:0]								
45	0x2D													BUCK2_ICOIL_UPD	BUCK2_ICOIL[7:0]							
46	0x2E			BUCK2_IAVG_DAC[8:0]										BUCK2_IRIP_DAC[8:0]								
47	0x2F																					
48	0x30																					
49	0x31																					
50	0x32																					
51	0x33																					
52	0x34																					
53	0x35																					
54	0x36							BST_SKCL	BST_OV	BST_SYNCFAIL	BST_FBFAIL	BST_OSCFAIL	VDRV_UV				BST2_REGSTATUS[1:0]		BST2_RUNNING	BST1_REGSTATUS[1:0]		BST1_RUNNING
55	0x37													VIST[8:0]								
56	0x38																					
57	0x39																					
58	0x3A																					
59	0x3B			VCC[8:0]										VINT[8:0]								
60	0x3C			VDRV[8:0]										VTEMP[8:0]								
61	0x3D	CSB_DUR[19:0]																				
62	0x3E	EEPROM_DATA_READ[19:0]																				
63	0x3F					EEPROM_LOCK_CUST	EEPROM_WRITEFAIL	EEPROM_READFAIL	EEPROM_BUSY	REVID[12:0]												

	Write
	Write FSO
	Read Only
	Read Only Clear by Read
	NOP

Figure 47. NCV78964 SPI Address Map

Default value of all SPI registers after POR is 0x00 if not specified explicitly.

SPI register SPI_REVID[12:0] is used to track the silicon version, following encoding mechanism is used:

- REVID[12:8]: Device ID for NCV78964 = 00001 [binary]
- REVID[7:6]: Option ID
- REVID[5:3]: Full Mask Version
- REVID[2:0]: Metal Tune

Table 26. SPI MAP BIT DEFINITION

Symbol	MAP Position	Description
REGISTER 0x00 (CR): NOP REGISTER		
NOP[20:0]	Bits [20:0] − ADDR_0x00	NOP Register (Read/Write Operation Ignored)
REGISTER 0x01 (BUCK1) or 0x05 (BUCK2) (CR): BUCKx CONFIGURATION		
BUCK1_DCM_CORR[2:0]	Bits [20:18] − ADDR_0x01	Correction of the average current in DCM mode
BUCK1_ZCD_DIS	Bit 17 − ADDR_0x01	Disabling the Buck Zero Cross Detector
BUCK1_TOFF[6:0]	Bits [16:10] − ADDR_0x01	Buck Current Ripple (TOFF·VCOIL constant)
BUCK1_IRNG[1:0]	Bit 8 − ADDR_0x01	Buck Current Range 0 or 1
BUCK1_IAVG[7:0]	Bits [7:0] − ADDR_0x01	Buck Average Current
REGISTER 0x02 (BUCK1) or 0x06 (BUCK2) (CR): BUCKx CONFIGURATION		
BUCK1_TSD_RCVR	Bit 19 − ADDR_0x02	Automatic recovery of Buck after Thermal Shutdown (TSD) or Buck switch local thermal shutdown (BUCKx_TSD)
BUCK1_RCVR[1:0]	Bits [18:17] − ADDR_0x02	Automatic recovery of Buck after BUCKx_OVLD event
BUCK1_SHORTLED_MASK[1:0]	Bits [16:15] − ADDR_0x02	Disabling of Buck SHORTLED protection for first x periods
VLED1_RNG	Bit 14 − ADDR_0x02	LED string voltage measurement range: 70 V or 35 V
BUCK1_IREG_PAUSE	Bit 13 − ADDR_0x02	Pause of Buck Average current regulation (IRIP not updated)
BUCK1_FREQ_PAUSE	Bit 12 − ADDR_0x02	Pause of Buck Frequency regulation (TOFF not updated)
BUCK1_FREQ_RATE[1:0]	Bits [11:10] − ADDR_0x02	Buck Frequency regulation maximum regulation step in case FAST_RCVR is set to fast
BUCK1_FREQ_RSP[1:0]	Bits [9:8] − ADDR_0x02	Buck Frequency regulation minimal regulation response time
BUCK1_FREQ_FAST_RCVR	Bit 7 − ADDR_0x02	Buck Frequency regulation slow (0) or fast (1)
BUCK1_FREQ_ABOVE	Bit 6 − ADDR_0x02	Buck Frequency kept below or above programmed frequency
BUCK1_FREQ[5:0]	Bits [5:0] − ADDR_0x02	Buck Frequency
REGISTER 0x03 (BUCK1) or 0x07 (BUCK2) (CR): BUCKx CONFIGURATION		
BUCK1_DIM_SHIFT	Bit 16 − ADDR_0x03	Buck Internal dimming phase shift
BUCK1_DIM_FADEOUT[2:0]	Bits [15:13] − ADDR_0x03	Buck Fade Out settings
BUCK1_DIM_FADEIN[2:0]	Bits [12:10] − ADDR_0x03	Buck Fade In settings
BUCK1_DIM_DUTY[7:0]	Bits [9:2] − ADDR_0x03	Buck Internal dimming duty ratio
LEDCTRL1_MD[1:0]	Bits [1:0] − ADDR_0x03	Mode of LEDCTRL pin
REGISTER 0x04 (BUCK1) or 0x08 (BUCK2) (CR): BUCKx CONFIGURATION		
BUCK1_REGFAIL_FMASK	Bit 2 − ADDR_0x04	Adding the REGSTATUS failure into BUCKxERR for Failure Output and for SPI read frame FAILURE_FLAGS[5:0] section
BUCK1_OPENLED_FMASK	Bit 1 − ADDR_0x04	Adding the OPENLED failure into BUCKxERR for Failure Output and for SPI read frame FAILURE_FLAGS[5:0] section
BUCK1_SHORTLED_FMASK	Bit 0 − ADDR_0x04	Adding the SHORTLED failure into BUCKxERR for Failure Output and for SPI read frame FAILURE_FLAGS[5:0] section
REGISTER 0x0D (CR): BUCK CONFIGURATION		
BUCK_DIM_FREQ[1:0]	Bits [4:3] − ADDR_0x0D	Buck Internal dimming frequency
BUCK2_EN	Bit 1 − ADDR_0x0D	Buck 2 Enable

Table 26. SPI MAP BIT DEFINITION (continued)

Symbol	MAP Position	Description
REGISTER 0x0D (CR): BUCK CONFIGURATION		
BUCK1_EN	Bit 0 − ADDR_0x0D	Buck 1 Enable
REGISTER 0x0E (BOOST1) or 0x0F (BOOST2) (CR): BOOSTx CONFIGURATION		
BST1_SLP_CTRL[2:0]	Bits [13:11] − ADDR_0x0E	Booster Phase Slope Control
BST1_COMP_DIV[2:0]	Bits [10:8] − ADDR_0x0E	Booster Phase Division factor from the COMP pin
BST1_VLIM_THR[7:0]	Bits [7:0] − ADDR_0x0E	Booster Phase Current limitation threshold
REGISTER 0x11 (CR): BOOST CONFIGURATION		
BST_ILIM_FMASK	Bit 20 − ADDR_0x11	Adding the ILIM (current limitation) status into BSTERR for Failure Output and for SPI read frame FAILURE_FLAGS[5:0] section
VDRV_UV_RCVR	Bit 19 − ADDR_0x11	Automatic Recovery after VDRIVE Undervoltage
VDRV_UV_THR[2:0]	Bits [18:16] − ADDR_0x11	VDRIVE Undervoltage threshold
BST_OTA_GAIN[1:0]	Bits [15:14] − ADDR_0x11	Booster Error Amplifier Gain
BST_MIN_TON[1:0]	Bits [13:12] − ADDR_0x11	Booster Minimal TON time
BST_MIN_TOFF[2:0]	Bits [11:9] − ADDR_0x11	Booster Minimal TOFF time
BST_SRC_FREQ[4:0]	Bits [8:4] − ADDR_0x11	Booster Internal clock frequency
BST_SRC_DIV	Bit 3 − ADDR_0x11	Booster clock frequency divided by 1 or 2
BST_SRC_INV	Bit 2 − ADDR_0x11	Booster clock inversion
BST_SRC[1:0]	Bits [1:0] − ADDR_0x11	Booster clock source
REGISTER 0x12 (CR): BOOST CONFIGURATION		
BST_SKCL_THR[1:0]	Bits [20:19] − ADDR_0x12	Booster Skip cycle
BST_SOFTSTART_UV	Bits 18 − ADDR_0x12	Booster Soft-start activation after VDRIVE Undervoltage
BST_SOFTSTART[2:0]	Bits [17:15] − ADDR_0x12	Booster Soft-start
BST_OV_REACT[1:0]	Bits [14:13] − ADDR_0x12	Booster overvoltage reactivation level
BST_OV_SD[2:0]	Bits [12:10] − ADDR_0x12	Booster overvoltage level
BST_VSETPOINT[6:0]	Bits [9:3] − ADDR_0x12	Booster voltage setpoint
BST2_EN	Bit 1 − ADDR_0x12	Booster Phase 2 Enable
BST1_EN	Bit 0 − ADDR_0x12	Booster Phase 1 Enable
REGISTER 0x1A (CR): OSCILLATOR CALIBRATION & THERMAL WARNING SETTINGS		
OSC_CAL[4:0]	Bits [13:9] − ADDR_0x1A	Calibration of the internal Oscillator. Signed, coded as two's complement
THERMAL_WARNING_THR[8:0]	Bits [8:0] − ADDR_0x1A	Thermal Warning Threshold Settings
REGISTER 0x1B (CR): EEPROM OPERATION		
EEPROM_DATA_WRITE[19:0]	Bits [19:0] − ADDR_0x1B	EEPROM Data to be Written
REGISTER 0x1C (CR): EEPROM OPERATION		
EEPROM_ADDRESS[4:0]	Bits [8:4] − ADDR_0x1C	EEPROM Address
EEPROM_CTRL[3:0]	Bits [3:0] − ADDR_0x1C	EEPROM Command
REGISTER 0x1D (CR): FSO MODE CONFIGURATION		
BST_FAIL_OUT	Bit 9 − ADDR_0x1D	Providing the Booster failure BSTERR to Failure Output
BUCK2_FAIL_OUT	Bit 8 − ADDR_0x1D	Providing the Buck 2 failure BUCK2ERR to Failure Output
BUCK1_FAIL_OUT	Bit 7 − ADDR_0x1D	Providing the Buck 1 failure BUCK1ERR to Failure Output
FSO_WDG_CFG[1:0]	Bits [6:5] − ADDR_0x1D	Watchdog time-out configuration
FSO_WDG_ENA[1:0]	Bits [4:3] − ADDR_0x1D	Watchdog mode
FSO_EXIT	Bit 2 − ADDR_0x1D	FSO mode exit command

Table 26. SPI MAP BIT DEFINITION (continued)

Symbol	MAP Position	Description
REGISTER 0x1D (CR): FSO MODE CONFIGURATION		
FSO_ENTER	Bit 1 − ADDR_0x1D	FSO mode enter command
SWRESET	Bit 0 − ADDR_0x1D	Software Reset
REGISTER 0x20 (SR): DIAGNOSTIC		
TRIMERR	Bit 11 − ADDR_0x20	Trimming or Calibration EEPROM data CRC check failed
EEPROMERR	Bit 10 − ADDR_0x20	Logical OR of EEPROM_WRITEFAIL and EEPROM_READFAIL errors
SPIERR	Bit 9 − ADDR_0x20	SPI Error Flag, Latched
CMD_REJECT	Bit 8 − ADDR_0x20	EEPROM operation or write into EEPROM_DATA_WRITE[19:0] register not accepted or trial to write not allowed SPI registers in FSO mode rejected, Latched
FRAME_CNT[3:0]	Bits [7:4] − ADDR_0x20	SPI Frame Counter
TSD	Bit 3 − ADDR_0x20	Thermal Shutdown Flag, Latched
TW	Bit 2 − ADDR_0x20	Thermal Warning Flag
FSO	Bit 1 − ADDR_0x20	FSO mode indicator
HWR	Bit 0 − ADDR_0x20	Hardware Reset Flag, Latched
REGISTER 0x21 (BUCK1) or 0x28 (BUCK2) (SR): BUCKx DIAGNOSTIC		
BUCK1_TSD	Bit 13 − ADDR_0x21	BUCK Switch Local Thermal Shutdown Flag, Latched
BUCK1_CBT_OV	Bit 12 − ADDR_0x21	CBT domain Overvoltage Failure, Latched
BUCK1_CBT_UV	Bit 11 − ADDR_0x21	CBT domain reset
BUCK1_OPENLED	Bit 10 − ADDR_0x21	Open LED string Failure
BUCK1_SHORTLED	Bit 9 − ADDR_0x21	Shorted LED string Failure
BUCK1_OVLD	Bit 8 − ADDR_0x21	LED string or Buck Switch Overcurrent Failure, Latched
BUCK1_MIN_TON	Bit 7 − ADDR_0x21	Buck minimum Ton time detected, output current not in regulation, Latched
BUCK1_ZCDMODE	Bit 6 − ADDR_0x21	Zero Cross event detected by Zero Cross detector
LEDCTRL1_MON[1:0]	Bits [5:4] − ADDR_0x21	LEDCTRL pin monitor, bit [0] set when “log. 0” detected, bit[1] set when “log. 1” detected, Latched
BUCK1_DIM_FADE	Bit 3 − ADDR_0x21	Fading effect in process
BUCK1_REGSTATUS[1:0]	Bits [2:1] − ADDR_0x21	Buck current regulation status
BUCK1_RUNNING	Bit 0 − ADDR_0x21	Buck status indicating that output regulates current to the LED
REGISTER 0x22 (BUCK1) or 0x29 (BUCK2) (SR): BUCKx DIAGNOSTIC		
BUCK1_TOFF_UPD	Bit 17 − ADDR_0x22	BUCKx_TOFF_MON[6:0] register updated with actual measurement result, Latched
BUCK1_TOFF_MON[6:0]	Bits [16:10] − ADDR_0x22	Monitor of actual TOFF·VCOIL parameter
BUCK1_IRIP_UPD	Bit 9 − ADDR_0x22	IRIP register updated with actual measurement result, Latched
BUCK1_IRIP[8:0]	Bits [8:0] − ADDR_0x22	IRIP (“$I_{BUCK_{peak}} - I_{PEAK_{AVG}}$”) value regulated by internal algorithm for average current regulation
REGISTER 0x23 (BUCK1) or 0x2A (BUCK2) (SR): BUCKx DIAGNOSTIC		
VIN1[8:0]	Bits [18:10] − ADDR_0x23	Output of VIN ADC measurement
VLED1[8:0]	Bits [8:0] − ADDR_0x23	Output of VLED ADC measurement
REGISTER 0x24 (BUCK1) or 0x2B (BUCK2) (SR): BUCKx DIAGNOSTIC		
VLED1ON[8:0]	Bits [18:10] − ADDR_0x24	Output of VLED ON ADC measurement
VLED1OFF[8:0]	Bits [8:0] − ADDR_0x24	Output of VLED OFF ADC measurement

Table 26. SPI MAP BIT DEFINITION (continued)

Symbol	MAP Position	Description
REGISTER 0x25 (BUCK1) or 0x2C (BUCK2) (SR): BUCKx DIAGNOSTIC		
BUCK1_T_UPD	Bit 20 − ADDR_0x25	BUCKx_TOFF_DUR[9:0] and BUCKx_TON_DUR[9:0] registers updated with actual measurement result, Latched
BUCK1_TOFF_DUR[9:0]	Bits [19:10] − ADDR_0x25	Buck Toff Time Duration
BUCK1_TON_DUR[9:0]	Bits [9:0] − ADDR_0x25	Buck Ton Time Duration
REGISTER 0x26 (BUCK1) or 0x2D (SR): BUCKx DIAGNOSTIC		
BUCK1_ICOIL_UPD	Bit 8 − ADDR_0x26	BUCKx_ICOIL[7:0] register updated with actual measurement result, Latched
BUCK1_ICOIL[7:0]	Bits [7:0] − ADDR_0x25	Actual value of Average current
REGISTER 0x27 (BUCK1) or 0x2E (SR): BUCKx DIAGNOSTIC		
BUCK1_IAVG_DAC[8:0]	Bits [18:10] − ADDR_0x27	Value of internal IAVG register after calibration with actual measured temperature VTEMP
BUCK1_IRIP_DAC[8:0]	Bits [8:0] − ADDR_0x27	Value of internal IRIP register after calibration with actual measured temperature VTEMP
REGISTER 0x36 (SR): BOOST DIAGNOSTIC		
BST_SKCL	Bit 14 − ADDR_0x36	Booster Skip Cycle mode indicator, Latched
BST_OV	Bit 13 − ADDR_0x36	Booster Overvoltage detected, Latched
BST_SYNCFAIL	Bit 12 − ADDR_0x36	Booster External PWM Clock Failure
BST_FBFAIL	Bit 11 − ADDR_0x36	Booster Feedback Failure
BST_OSCFAIL	Bit 10 − ADDR_0x36	Booster Hardware error
VDRV_UV	Bit 9 − ADDR_0x36	VDRV Undervoltage detected
BST2_REGSTATUS[1:0]	Bits [5:4] − ADDR_0x36	Booster Phase 2 Regulation status
BST2_RUNNING	Bit 3 − ADDR_0x36	Booster Phase 2 Running indicator
BST1_REGSTATUS[1:0]	Bits [2:1] − ADDR_0x36	Booster Phase 1 Regulation status
BST1_RUNNING	Bit 0 − ADDR_0x36	Booster Phase 1 Running indicator
REGISTER 0x37 (SR): BOOST DIAGNOSTIC		
VBST[8:0]	Bits [8:0] − ADDR_0x37	Output of VBST ADC measurement
REGISTER 0x3B (SR): ADC		
VCC[8:0]	Bits [18:10] − ADDR_0x3B	Output of VCC ADC measurement
VINT[8:0]	Bits [8:0] − ADDR_0x3B	Output of VINT ADC measurement
REGISTER 0x3C (SR): ADC		
VDRV[8:0]	Bits [18:10] − ADDR_0x3C	Output of VDRV ADC measurement
VTEMP[8:0]	Bits [8:0] − ADDR_0x3C	Output of VTEMP ADC measurement
REGISTER 0x3D (SR): DIAGNOSTIC		
CSB_DUR[19:0]	Bits [19:0] − ADDR_0x3D	Measured Duration of CSB low pulse
REGISTER 0x3E (SR): EEPROM		
EEPROM_DATA_READ[19:0]	Bits [19:0] − ADDR_0x3E	EEPROM Read Data
REGISTER 0x3F (SR): EEPROM & REVID		
EEPROM_LOCK_CUST	Bit 16 − ADDR_0x3F	EEPROM Customer Data Locked
EEPROM_WRITEFAIL	Bit 15 − ADDR_0x3F	EEPROM Data Write Failure
EEPROM_READFAIL	Bit 14 − ADDR_0x3F	EEPROM Data CRC check Failure, Latched
EEPROM_BUSY	Bit 13 − ADDR_0x3F	EEPROM Busy
REVID[12:0]	Bits [12:0] − ADDR_0x3F	Revision ID of the Device

EEPROM MEMORY

	ADDR	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
17	0x11	BUCK_DIM_FREQ[1:0]		BST_FAIL_OUT	BUCK2_FAIL_OUT	BUCK1_FAIL_OUT	FSO_WDG_CFG[1:0]		FSO_WDG_ENA[1:0]		FSO_ENTER	SPI_PRELOAD	THERMAL_WARNING_THR[8:0]								
18	0x12		BUCK1_ZCD_DIS	BUCK1_TOFF[6:0]							BUCK1_IRNG[1:0]		BUCK1_IAVG[7:0]								BUCK1_EN
19	0x13	BUCK1_TSD_RCVR	BUCK1_RCVR[1:0]		BUCK1_SHORTLED_MASK[1:0]		VLED1_RNG		LEDCTRL1_MD[1:0]	BUCK1_IREG_PAUSE	BUCK1_FREQ_PAUSE	BUCK1_FREQ_RSP[1:0]		BUCK1_FREQ_FAST_RCVR	BUCK1_FREQ_ABOVE			BUCK1_FREQ[5:0]			
20	0x14	BUCK1_DCM_CORR[2:0]			BUCK1_FREQ_RATE[1:0]		BUCK1_DIM_SHIFT		BUCK1_DIM_FADEOUT[2:0]		BUCK1_DIM_FADEIN[2:0]			BUCK1_DIM_DUTY[7:0]							
21	0x15		BUCK2_ZCD_DIS	BUCK2_TOFF[6:0]							BUCK2_IRNG[1:0]		BUCK2_IAVG[7:0]								BUCK2_EN
22	0x16	BUCK2_TSD_RCVR	BUCK2_RCVR[1:0]		BUCK2_SHORTLED_MASK[1:0]		VLED2_RNG		LEDCTRL2_MD[1:0]	BUCK2_IREG_PAUSE	BUCK2_FREQ_PAUSE	BUCK2_FREQ_RSP[1:0]		BUCK2_FREQ_FAST_RCVR	BUCK2_FREQ_ABOVE			BUCK2_FREQ[5:0]			
23	0x17	BUCK2_DCM_CORR[2:0]			BUCK2_FREQ_RATE[1:0]		BUCK2_DIM_SHIFT		BUCK2_DIM_FADEOUT[2:0]		BUCK2_DIM_FADEIN[2:0]			BUCK2_DIM_DUTY[7:0]							
24	0x18		BST_ILIM_FMASK	BST_OTA_GAIN[1:0]		BST_SOFTSTART_UV	BST_SOFTSTART[2:0]			BST_OV_REACT[1:0]		BST_OV_SD[2:0]		BST_VSETPOINT[6:0]							
25	0x19	VDRV_UV_RCVR	VDRV_UV_THR[2:0]			BST_SKCL_THR[1:0]		BST_MIN_TON[1:0]		BST_MIN_TOFF[2:0]			BST_SRC_FREQ[4:0]				BST_SRC_DIV	BST_SRC_INV	BST_SRC[1:0]		
26	0x1A	BUCK1_REGFAIL_FMASK	BUCK1_OPENLED_FMASK	BUCK1_SHORTLED_FMASK			BST1_SLP_CTRL[2:0]			BST1_COMP_DIV[2:0]			BST1_VLIM_THR[7:0]							BST1_EN
27	0x1B	BUCK2_REGFAIL_FMASK	BUCK2_OPENLED_FMASK	BUCK2_SHORTLED_FMASK			BST2_SLP_CTRL[2:0]			BST2_COMP_DIV[2:0]			BST2_VLIM_THR[7:0]							BST2_EN
28	0x1C	EEPROM_LOCK_CUST				CRC_EEPROM_CUST[15:0]															

	Customer
	unused

Figure 48. NCV78964 EEPROM MEMORY MAP

EEPROM memory serves as persistent storage for Customer configuration and for **onsemi** calibration, trimming and test data. EEPROM memory is organized as 51 words, each 20 bits wide. The access to the memory is word-based.

EEPROM Operations

The NCV78964 supports following operations with EEPROM memory:

- EEPROM_CTRL[3:0] = 0xxx [binary]: EEPROM in Power-down state (no operation)
- EEPROM_CTRL[3:0] = 1xxx [binary]: **Enable**
- EEPROM_CTRL[3:0] = 1001 [binary]: **Read** − data addressed by SPI register EEPROM_ADDRESS[4:0] become available in SPI register EEPROM_DATA_READ[19:0] after end of Read operation
- EEPROM_CTRL[3:0] = 1110 [binary]: **Unlock Write**
- EEPROM_CTRL[3:0] = 1010 [binary]: **Write** − data in EEPROM_DATA_WRITE[19:0] SPI register will be written into address EEPROM_ADDRESS[4:0]

EEPROM Read Operation

The correct sequence to Read data from EEPROM memory should be the following:

- Write '**Enable**' (0x8) into EEPROM_CTRL[3:0] SPI register to bring EEPROM memory into powered state
- Read EEPROM_CTRL[3:0] SPI register and check that it is '**Enable**' (0x8)
- Wait until EEPROM_BUSY is 0 (EEPROM power-up time is app. 30 μs)
- Write required address into EEPROM_ADDRESS[4:0] SPI register and write '**Read**' (0x9) into EEPROM_CTRL[3:0] SPI register to perform Read command
- Read EEPROM_CTRL[3:0] SPI register and check that it is '**Read**' (0x9) and read EEPROM_ADDRESS[4:0] SPI register and check that it is correct
- Read data at EEPROM_DATA_READ[19:0] SPI register
- Repeat reading from all required addresses
- Write 'Power down' (0x0) into EEPROM_CTRL[3:0] SPI register to put EEPROM memory into power-down mode
- To check that all content was written correctly,

EEPROM write Operation

The correct sequence to Write data to EEPROM memory should be the following:

- Write '**Enable**' (0x8) into EEPROM_CTRL[3:0] SPI register to bring EEPROM memory into powered state
- Read EEPROM_CTRL[3:0] SPI register and check that it is '**Enable**' (0x8)
- Wait until EEPROM_BUSY is 0 (EEPROM power-up time is app. 30 μs)
- Write required data into EEPROM_DATA_WRITE[19:0] SPI register
- Read data at EEPROM_DATA_WRITE[19:0] SPI register and check if the content is correct
- Write '**Unlock Write**' (0xE) into EEPROM_CTRL[3:0] SPI register to enable write
- Read EEPROM_CTRL[3:0] SPI register and check that it is '**Unlock Write**' (0xE)
- Write required address into EEPROM_ADDRESS[4:0] SPI register and write '**Write**' (0xA) into EEPROM_CTRL[3:0] SPI register to perform Write command
- Read EEPROM_CTRL[3:0] SPI register and check that it is '**Write**' (0xA) and read EEPROM_ADDRESS[4:0] SPI register and check that it is correct
- Wait until EEPROM_BUSY is 0 (EEPROM word programming time is app. 9.2 ms)
- Check that EEPROM_WRITEFAIL is 0. Discard the device if EEPROM_WRITEFAIL is 1.
- Repeat writing into all required addresses
- Read and check EEPROM data from all written addresses
- Write 'Power down' (0x0) into EEPROM_CTRL[3:0] SPI register to put EEPROM memory into power-down mode

To provide extra safety, CRC protection is implemented to secure EEPROM memory content. The following CRC checks are implemented:

CRC_EEPROM_TRIM is internally calculated over **onsemi** trimming and calibration data.

CRC_EEPROM_CUST[15:0] (ADDR_0x1C) is calculated over all EEPROM Customer data, starting from bit 0 on EEPROM address 0x11 and ending at bit 19 of EEPROM address 0x1B.

CRC algorithm with following parameters is used:

- CRC length is 16 bits,
- CRC polynomial 0xBAAD (Koopman's notation; x16+x14+x13+x12+x10+x8+x6+x4+x3+x+1),
- CRC initialization value 0xFFFF.

External microcontroller should calculate its own CRC from the appropriate EEPROM data and verify that calculated CRC matches with CRC stored in EEPROM.

PCB LAYOUT RECOMMENDATIONS

This section contains instructions for the NCV78964 PCB layout application design. Although this guide does not claim to be exhaustive, these directions can help the developer to reduce application noise impact and ensuring the best system operation. All important areas are highlighted on the following picture:

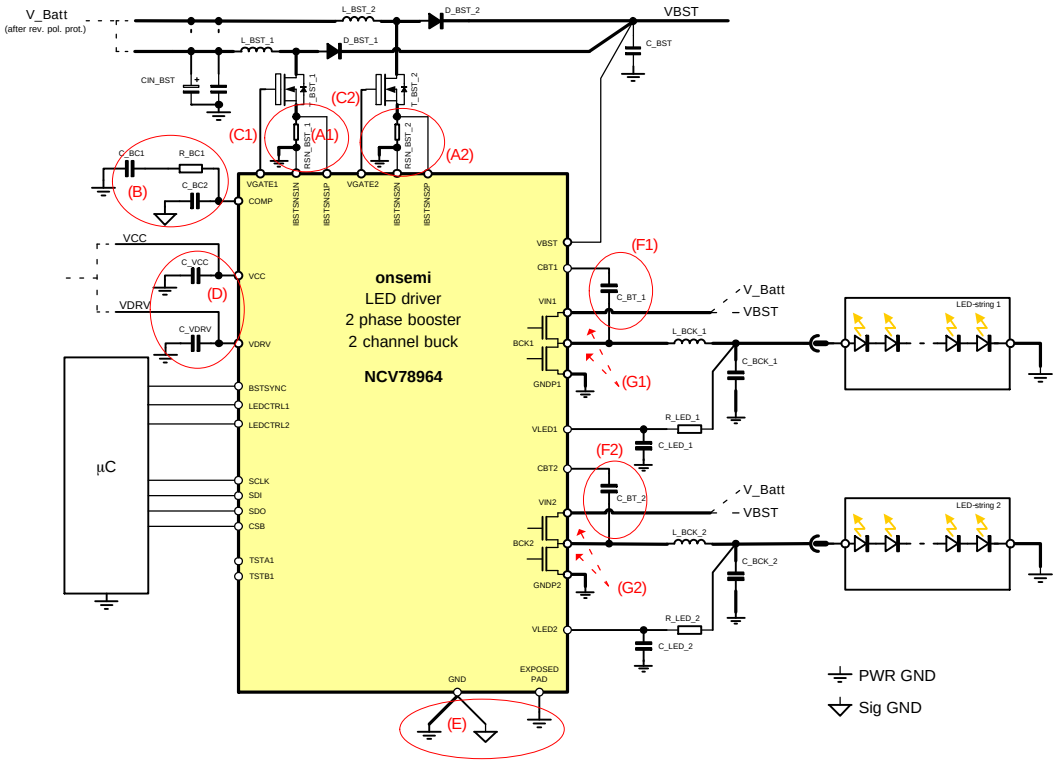


Figure 49. NCV78964 Application Critical PCB Areas

PCB Layout: Booster Current Sensing − Area (A1, A2)

The booster current sensing circuit is used both by the loop regulation and the current limitation mechanism. In case of current sensing over sensing resistor, it relies on a low voltage comparator, which triggers with respect to the sense voltage across the external resistors RSN_BST_1/2. In order to maximize power efficiency (= minimum losses on the sense resistor), the threshold voltage is rather low, with a maximum setting of typically 100 mV. This area may be affected by the MOSFET switching noise if no specific care is taken. The following recommendations are given:

1. Use a four terminals current sense method as depicted in the figure below. The measurement PCB tracks should run in parallel and as close as possible to each other, trying to have the same length. The number of vias along the measurement path should be minimized;
2. Place RSN_BST_1/2 sufficiently close to the MOSFET source terminal;
3. The MOSFET's dissipation area should be stretched in a direction away from the sense resistor to minimize resistivity changes due to heating;
4. If the current sense measurement tracks are interrupted by series resistors or jumpers (once as a maximum) their value should be matched and low ohmic (pair of 0 Ω to 47 Ω max) to avoid errors due to the comparator input bias currents. However, in case of high application noise, a PCB re-layout without RC filters is always recommended.
5. Avoid using the board GND as one of the measurement terminals as this would also introduce errors.

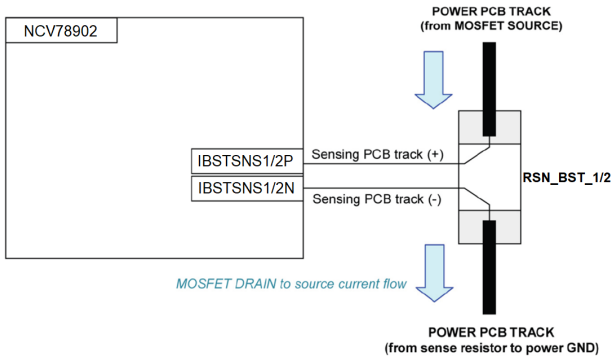


Figure 50. Four wires Method for Booster Current Sensing Circuit

NCV78964 allows also to use current sensing over MOSFET's RDSon. For this purpose the range of threshold for Imax current comparator is extended up to 600 mV. In this configuration it is recommended to place temperature sensor close to the MOSFET to have possibility to compensate RDSon temperature dependency.

PCB Layout: Booster Compensation Network − Area (B)

The compensation network must be placed very close to the chip to avoid noise capturing. Ground connection of booster compensation network should lead separately to signal ground of NCV78964 (pin GND) and only after this pin it should be connected to common power ground to avoid noise coming from other portions of the PCB ground. In addition a ground ring shall provide extra shielding ground around.

PCB Layout: Booster VGATE Signals − Area (C1, C2)

It has to be ensured that VGATE signals do not interfere with other signals like COMP or input of the IMAX or IREG comparators.

PCB Layout: VDD and VDRV Capacitors − Area (D)

The VDD decoupling capacitor has to be connected directly to the VDD and ground pins with separate PCB tracks to avoid coupling of the ground shift on the PCB into the chip.

PCB Layout: GND Connections − (E)

Ground connection between VINx decoupling capacitor and power GNDPx pins of NCV78964 device should be kept as short as possible to minimize power switching loop.

Ground connection of booster compensation network should lead separately to signal ground of NCV78964 (pin GND) and only after this pin it should be connected to common power ground signal to avoid noise coming from other portions of the PCB ground.

PCB Layout: Buck Bootstrap Capacitors − (F1, F2)

CBT capacitors should be placed as close as possible to the CBTx and BCKx pins.

PCB Layout: Buck Power Lines − (G1, G2)

VINx decoupling capacitors should be placed as close as possible to VINx pins and the tracks from BCKx pins to Buck inductors should be kept as short as possible. They should also be symmetrical and the straightest.

PCB Layout: Additional EMC Recommendations on Loops

It is suggested in general to have a good metal connection to the ground and to keep it as continuous as possible, not interrupted by resistors or jumpers. In additions, PCB loops for power lines should be minimized. A simplified application schematic is shown in the next figure to better focus on the theoretical explanation. When a DC voltage is applied to the VBB, at the left side of the boost inductor L_BOOST, a DC voltage also appears on the right side of L_BUCK and on the C_BUCK. However, due to the switching operation (boost and buck), the applied voltage generates AC currents flowing through the red area (1). These currents also create time variable voltages in the area marked in green (2). In order to minimize the radiation due to the AC currents in area 1, the tracks' length between L_BOOST and the pair L_BUCK plus C_BUCK must be kept low. At the contrary, if long tracks would be used, a bigger parasitic capacitance in area 2 would be created, thus increasing the coupled EMC noise level.

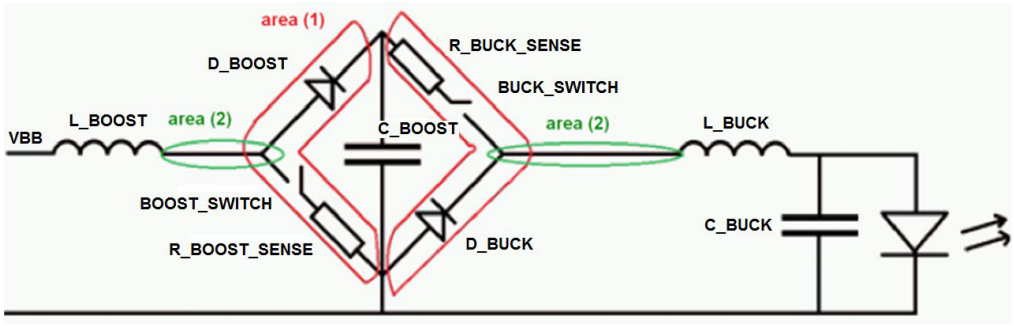


Figure 51. PCB AC Current Lines (1) and AC Voltage Nodes (2)

REFERENCE PCB LAYOUT

Recommended PCB layout for the NCV78964 is shown on the following figure. This layout comes from NCV78964 evaluation kit daughterboard which serves as a reference layout and where more details can be found if needed. This layout contains some extra components which would be avoided in final design (e.g. zero-ohm link selecting between booster current sensing over shunt resistor or MOSFET, resistors selecting voltage for VDD logic supply, etc.).

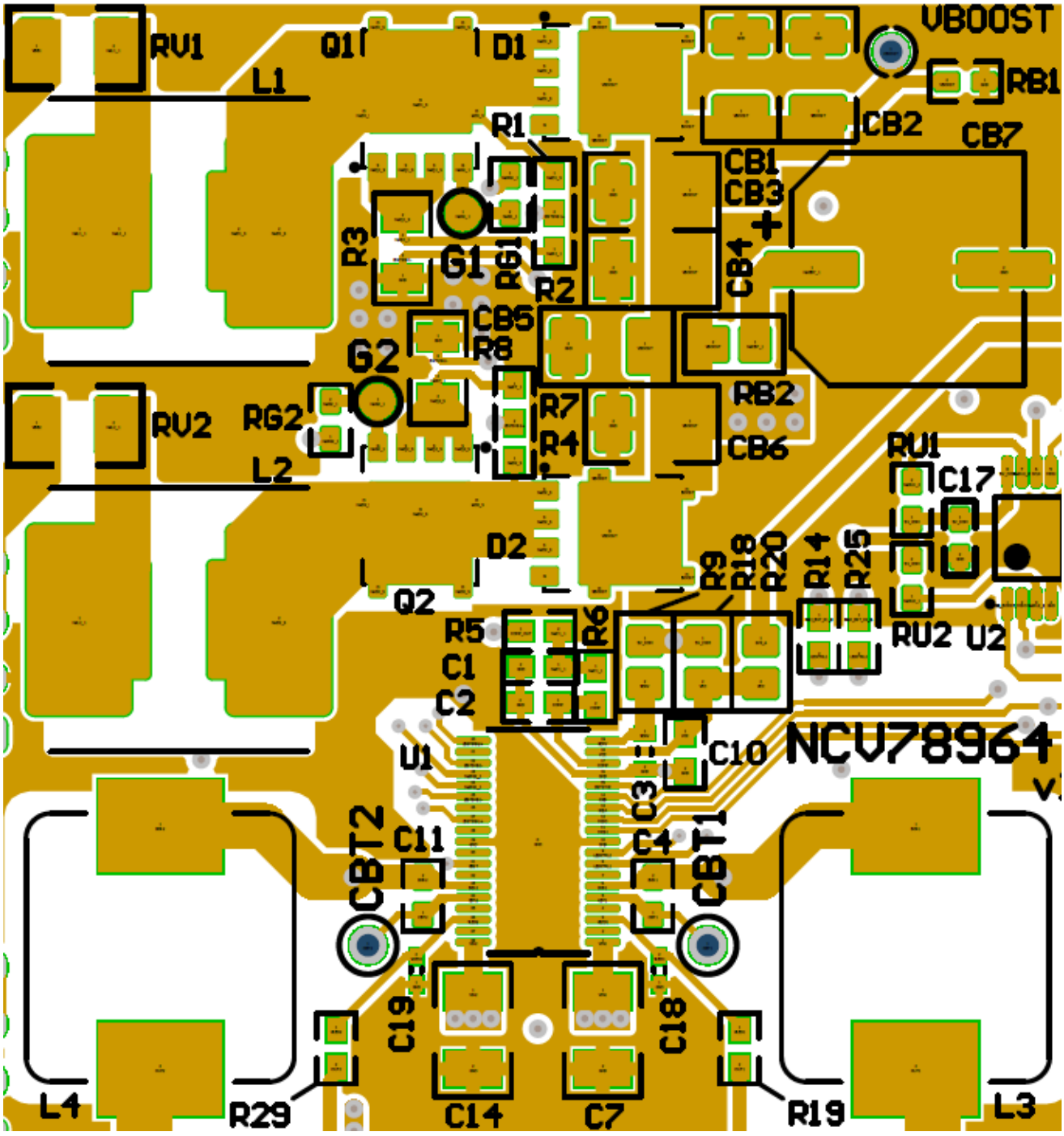


Figure 52. NCV78964 Reference PCB Layout

ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Shipping†
NCV78964PA0R2G	N7964 1	TSSOP38 EP (Pb-Free)	2500 / Tape & Reel
NCV78964PA1R2G	N96402	TSSOP38 TEP (Pb-Free)	2500 / Tape & Reel

* For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

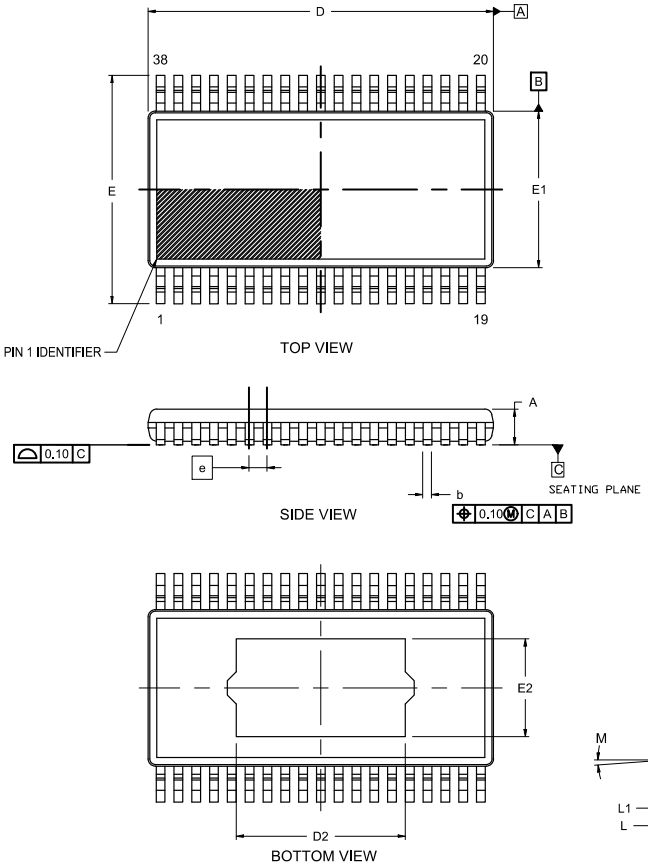
† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document version release.	9/18/2025

TSSOP38 EP 9.7x4.4
CASE 137AB
ISSUE O

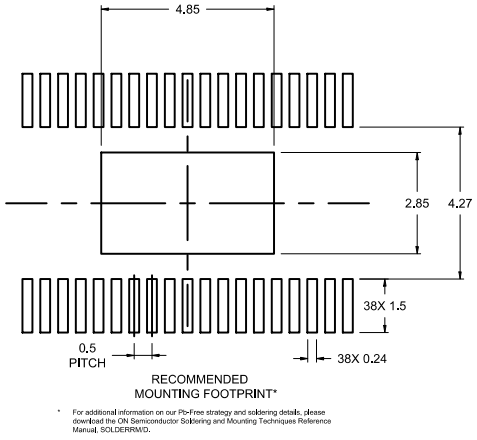
DATE 05 JUN 2019



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT BE IN 0.13 TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.10	0.15
A2	0.85	0.90	0.95
A3	0.34	---	0.43
b	0.17	---	0.27
b1	0.20 REF		
c	0.09	---	0.20
c1	0.127 REF		
D	9.60	9.70	9.80
D2	4.496	4.750	4.852
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
E2	2.489	2.743	2.845
e	0.50 BSC		
L	1.00 REF		
L1	0.50	---	0.70
M	0°	---	8°



For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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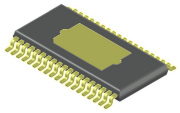
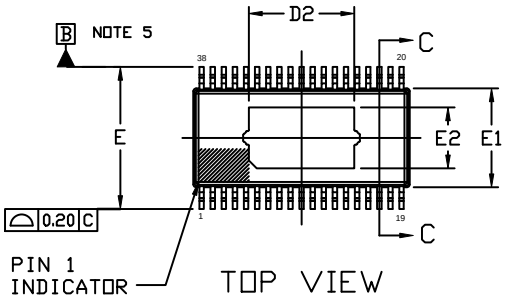
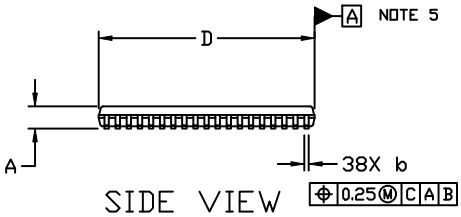
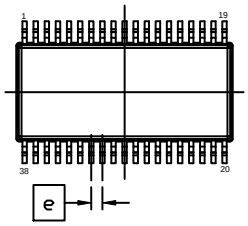


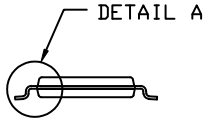
TSSOP38 TEP 9.7x4.4
CASE 948BX
ISSUE O

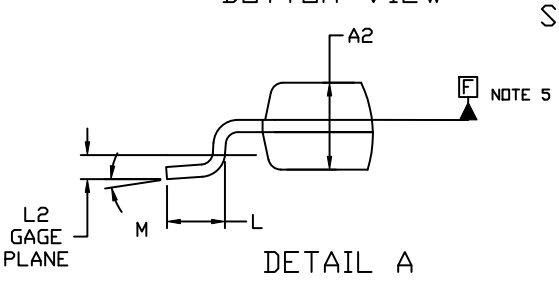
DATE 01 FEB 2021

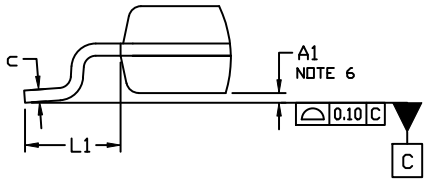












NOTES:
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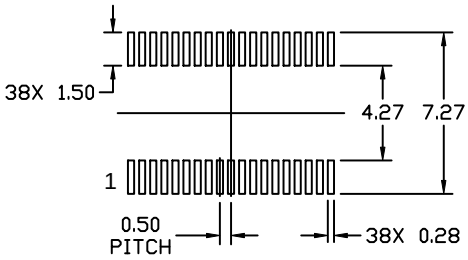
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.127 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. LEAD THICKNESS (c) AND LEAD WIDTH (b) INCLUDE PLATING THICKNESS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	---	0.15
A2	0.85	---	0.95
b	0.17	---	0.27
c	0.09	---	0.20
D	9.60	9.70	9.80
D2	4.496	---	4.852
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
E2	2.489	---	2.845
e	0.50 BSC		
L	0.50	---	---
L1	1.00 REF		
L2	0.25 REF		
M	0°	---	8°



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