Self-Test Ground Fault Circuit Interrupter (GFCI)

NCS37021

The NCS37021 is a UL943 compliant signal processor for GFCI applications with self-test. The device integrates a flexible power supply (including a 12 V shunt, two 3.3 V internal series regulators and a 1.8 V internal regulator), differential fault, and grounded-neutral detection circuits. Self-test is monitored at start up and then every minute.

Features

- Meets UL943 Self-test GFCI Requirements
- 4.0 – 12 V Operation
  (120−480 V AC Mains with the Appropriate Series Impedance)
- Wide Operating Temperature Range from −40 °C to 95 °C
- Low Quiescent Current
- Optimized Solenoid Deployment
  (Coil is not Energized Near the AC Mains Zero Crossings)
- Power Supply Monitor that Verifies Full Diode Bridge Operation
- Tiered GF Trip Times that Increase Immunity to Noise
- Under-voltage Detection that Allows for Increased Operation at Lower AC Input Voltages
- Intelligent Sensing Differentiating Ground Fault versus Ground Neutral Fault (Prevent Nuisance Tripping)
- 16 Pin QFN Package
- This is a Pb-Free Device

Typical Applications

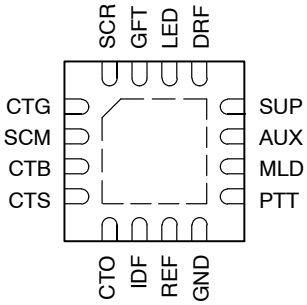
- GFCI Receptacles
- Load Panel GFCI Breakers
- In-line GFCI Circuits (Power Cords)

QFN16
CASE 485FQ

MARKING DIAGRAM

37021	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

BLOCK DIAGRAM

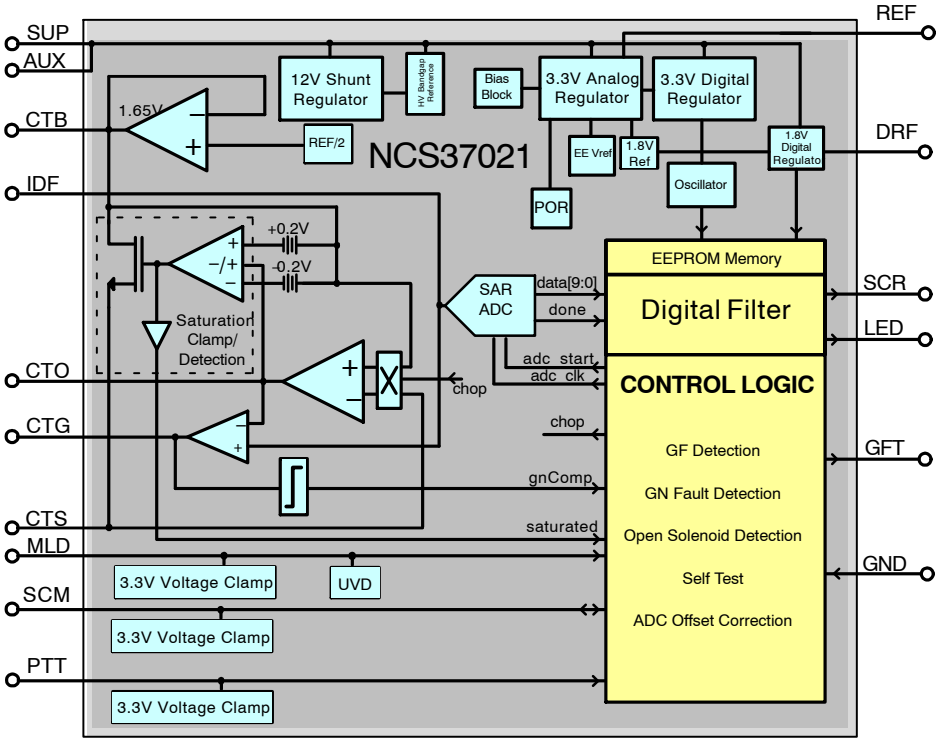


Figure 1. Simplified Block Diagram

Table 1. QFN PIN DESCRIPTION

Pin #	Name	Pin Description
1	CTG	Ground Neutral current transformer stimulus
2	SCM	Test input for SCR functionality
3	CTB	Differential current transformer bias voltage
4	CTS	Differential current input
5	CTO	Differential current to voltage output
6	IDF	Differential low pass filter/ADC input
7	REF	3.3 V Internal reference voltage
8	GND	Electronics ground
9	PTT	Reference current bias input Push to Test
10	MLD	Mains level/under voltage detector
11	AUX	Auxiliary power supply input
12	SUP	Power supply input
13	DRF	1.8 V Internal reference voltage
14	LED	End of life LED drive
15	GFT	Differential self-test output signal
16	SCR	SCR gate drive signal

Table 2. ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Rating	Symbol	Value	Unit
Supply Voltage Range	Vs	13.5	V
Supply Current	Is	10	mA
Input Voltage Range (Note 3)	V_{in}	−0.3 to 3.6	V
Output Voltage Range	V_{out}	−0.3 to 3.6 V or (V_{in} + 0.3), whichever is lower	V
Maximum Junction Temperature	$T_{J(max)}$	140	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 4)	ESD_{HBM}	2	kV
ESD Capability, Charge Device Model (Note 4)	ESD_{CDM}	500	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 5)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Functional operation above the Recommended Operating Conditions is not implied.
2. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC-Q100-002 (JEDEC JS-001-2010)
   ESD Charge Device Model tested per AEC-Q100-003 (JESD22-C101-A)
   Latchup Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78
5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, QFN16, 3 × 3.3 mm (Note 6) Thermal Resistance, Junction-to-Air (Note 7)	$R_{\theta JA}$	64	°C/W

6. Refer to ELECTRICAL CHARACTERISTICS for Safe Operating Area.
7. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

Table 4. OPERATING RANGES (Unless otherwise noted, ISUP = 3 mA, MLD input = 60 Hz, Refer to Figure 2)

Parameter	Conditions	Min	Typ	Max	Unit
Operating Temperature	Ambient	−40		95	°C
Shunt Regulator Voltage	SUP to GND, I_{SUP} = 1 mA	11		13	V
Shunt Regulator Current	I_{SUP}			10	mA
Quiescent Current	$I_{SUP\_Quiescent}$		1.3		mA
RMS Trip Threshold Voltage (5 mA)	IDF to CTB, R4A = 36 kΩ R4B = 50 Ω		160		mV
SCR Trigger Current	I_{SCR}			4	mA
SCR Trigger Output Voltage	SCR to GND, SUP > 4 V		3.3		V
LED Output Voltage	LED to GND, SUP > 4 V		3.3		V
CTB Bias Voltage	CTB to GND, VDA = 3.3 V		1.65		V
CTS−CTB Absolute Offset Voltage	CTS−CTB		±125		μV
Fault Response Time	5 mA ≤ I_{DIFF} < 15 mA			135	ms
Fault Response Time	15 mA ≤ I_{DIFF} < 30 mA			70	ms
Fault Response Time	30 mA ≤ I_{DIFF}			20	ms
CTG Comparator Threshold	CTG to GND, VDA = 3.3 V		1.95		V
CTG GN Trip Frequency	CTG to GND	2	4	7	kHz
GN Response Time	Continuous GN Fault		50		ms
Internal Oscillator Frequency	F_{AC} = 60 Hz ±0.1		25		MHz
Under Voltage Detect	V_{AC} to GND, R7 = 1 MΩ, ±1%	80	87	95	Vrms
MLD/SCM Max Clamp Current	I_{MLD} Max Sink Current			400	μA
MLD/SCM Pull Down Current	MLD = 1 V		1		μA
PTT Internal Pull Up Resistance	PTT = 0 V		50		kΩ
PTT Debounce Time	PTT Assert Low	16			ms
First ST Timer	VDA > 3 V		1		s
Periodic ST Timer, Pass	Steady State, ST Pass		1		min
Periodic ST Timer, Fail	ST Fail		12		AC cycle
Consecutive ST Failure Timer	ST Fail Counter, Enable SCR		7		times
LED Blink Frequency	First ST Failure		4		Hz
ST Cycle GF Pass Window	I_{DIFF} Ground Fault		7		mA
MLD Pin Check Wait Time to Enable LED	No MLD signal		64		ms
MLD Pin Continuity Pass	Input Frequency		60		Hz
LED Blink Frequency	No MLD signal		4		Hz
MLD/SCM Pin Check Wait Time to Enable SCR	No MLD signal		4		s

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

APPLICATIONS INFORMATION

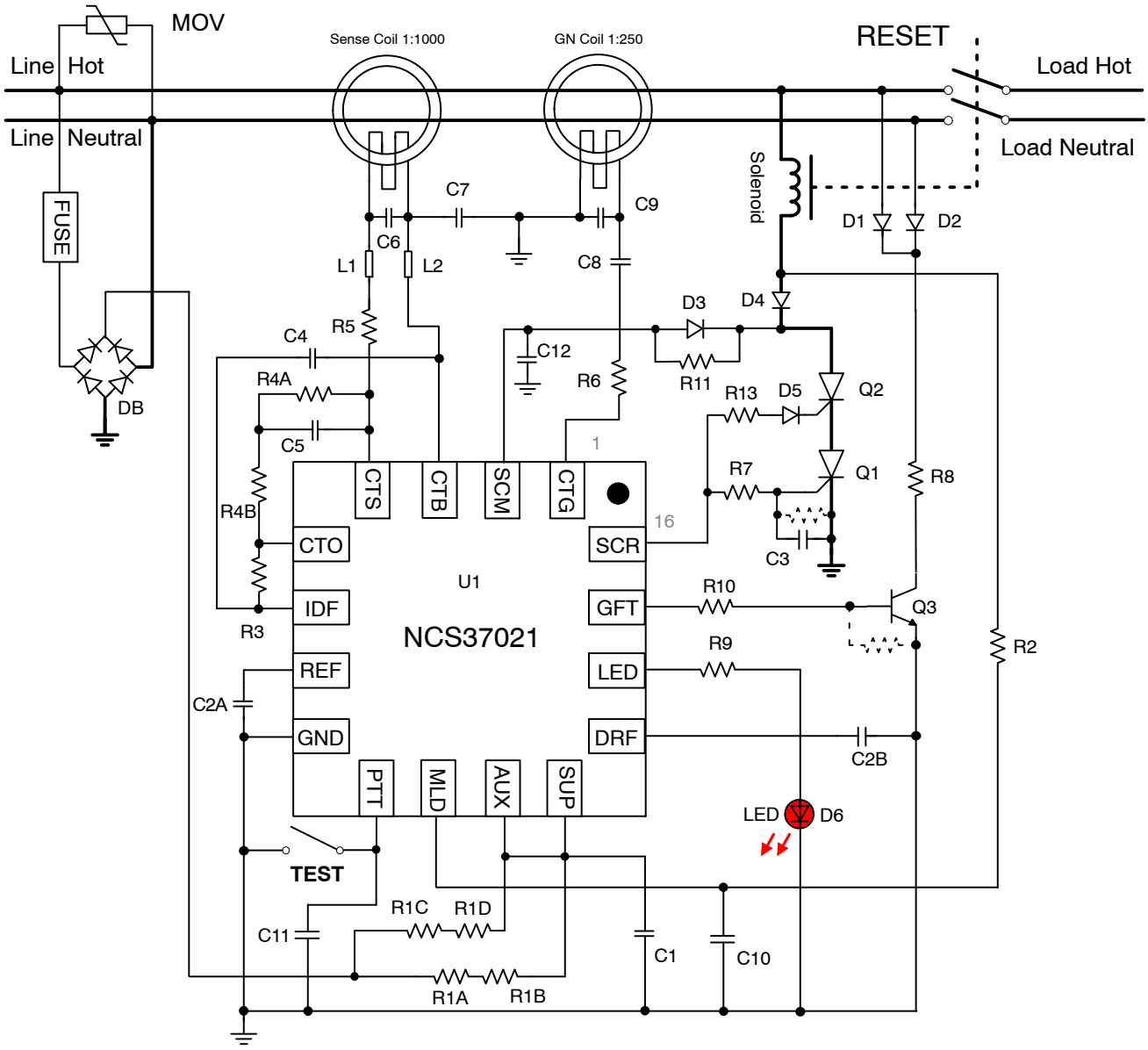


Figure 2. GFCI Receptacle Application Diagram

Table 5. RECOMMENDED EXTERNAL COMPONENTS

Component Type	Instance	Value	Note
SCR	Q1, Q2	–	
NPN	Q3	–	MMBT6517LT1−D
Diode Bridge	DB	–	
Diode	D1, D2, D3, D4, D5	–	1N4007
LED	D6	–	LED for self-test failure
Capacitor	C1	1 μF	SUP pin holding capacitor
Capacitor	C2A, C2B	1 μF	Internal 3.3 V and 1.8 V reference filter cap
Capacitor	C3	100 nF	SCR gate filter capacitor
Capacitor	C4	56 nF	Anti-aliasing filter (140 Hz corner frequency)
Capacitor	C5	2.2 nF	High frequency filter
Capacitor	C6	33 nF	Differential current filter capacitor
Capacitor	C7	1 nF	CTB bias filter
Capacitor	C8	10 nF	Ground Neutral CT resonance capacitor (Set the CTG GN Trip Frequency approximately 4 kHz)
Capacitor	C9	120 pF	Ground Neutral CT AC coupler
Capacitor	C10, C11, C12	100 pF	Ground noise filter
Resistor	R1A, R1B, R1C, R1D	25 kΩ	Current limit resistors
Resistor	R2	1 MΩ	MLD current limit/under voltage attenuator
Resistor	R3	20 kΩ	Differential filter resistor
Resistor	R4A	36 kΩ	Precision resistor (1%), Differential burden/CT low pass filter
Resistor	R4B	50 Ω	CT low pass filter
Resistor	R5	370 Ω	Differential burden resistor, 1% tolerance
Resistor	R6	0−10 Ω	Sets the GN sensitivity
Resistor	R7, R13	4.7 kΩ	Sets the SCR gate current
Resistor	R8	15 kΩ	Controls the self-test current in the Q3
Resistor	R9	3.3 kΩ	LED current limiter resistor
Resistor	R10	10 kΩ	Sets the current in the base of Q3
Resistor	R11	1 MΩ	Current limit resistor for SCM
Inductor	L1, L2	1 k @ 100 MHz	CIM05U102, CT RF filter
Current Transformer	CT1	1000	Differential current transformer
Current Transformer	CT2	250	GN current transformer

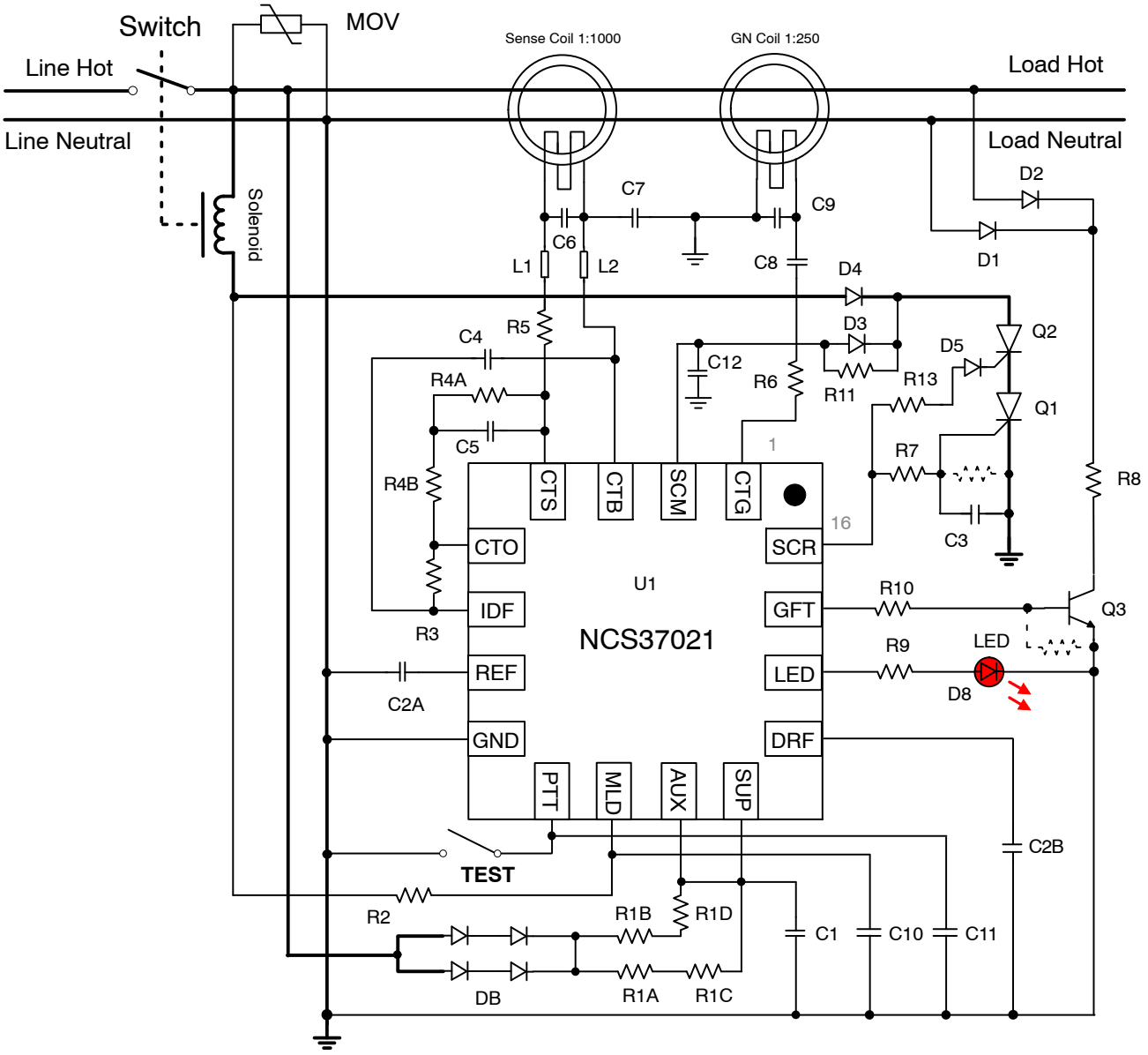


Figure 3. Circuit Breaker Application Diagram (Half Bridge Supply)

FUNCTIONAL DESCRIPTION (Refer to Application Circuit)

The NCS37021 provides ground fault, grounded neutral and self-test protection solution for a single IC controller per the UL943 standard.

The key internal blocks include:

- 12 V shunt regulator,
- Precision bandgap reference,
- Two 3.3 V linear regulators (one for the digital IO and one for the analog core circuit),
- 1.8 V linear regulator for digital core circuit,
- Sense amplifiers with V_{OS} cancellation,
- 1.65 V reference for the CT,
- 25 MHz oscillator dynamically trimmed to the AC line frequency,
- 10-bit SAR ADC,
- Comparators, digital filters, and digital control logic.

The SUP pin provides the bias voltage for the analog and digital IO via two 3.3 V linear regulators, as well as for the 1.8 V linear regulator for the internal digital circuitry. For safety operation this pin is clamped at ~12 volts by the shunt regulator.

At POR detection (REF > 2.475) the logic is reset and the bias circuitry is enabled. The MLD pin is continually checked for an input signal of 60 Hz. If the MLD has not toggled in approximately 64 ms, the fault condition is sent to the SCR block. If, after 4 seconds, the fault condition is still present, the SCR will fire for approximately 20 ms. This timing will continue if the fault condition remains.

The first self-test (ST) cycle will occur at 1 second after power-up and thereafter every 1 minute. During the ST cycle the GFT pin will be enabled at the positive MLD phase for ~16 ms and the CT current (set at 8 mA RMS, R8) will be verified for positive or negative MLD phase. During the next negative half cycle, at the beginning of the cycle the SCR's anode voltage will be pre-biased by the SCM pin to ~3.3 volts which will be verified by internal logic. The SCR will then be enabled and the SCR's anode voltage will be monitored by the SCM pin. If the anode voltage goes below ~2.1 volts, the SCR will be disabled after at least 250 us verification check and the ST logic will register a passing ST cycle. If a ST cycle fails due to a low GF detection, the LED blinking logic will be enabled. After a self-test failure, the testing frequency is accelerated to a faster interval 12 MLD. If seven consecutive ST cycles fail the SCR will be enabled. If a ST cycle passes before any of the 7 consecutive ST cycle counter, the ST logic will be reset and a ST cycle will occur in 1 minute.

The CT is biased approximately at 1.65 volts. The sense amplifier monitors the ground fault current. This current is converted to a voltage level at the CTO pin which is the input to the ADC (IDF pin). The resistor R4 sets the GF threshold per the following equation, and it needs to be above this threshold for > 8.35 ms within an AC Mains period:

$$I_{diff} = \frac{0.160 \times CT_1 \times \left(R_{CT1} + R_5 + 2\pi f_{AC} L_{CT1}\right)}{R_{4A} \times \left(R_{CT1} + 2\pi f_{AC} L_{CT1}\right)} \quad \text{(eq. 1)}$$

R_{CT1} is DC winding resistance of differential CT

f_{AC} is AC mains frequency

L_{CT1} is Inductance of differential CT

The ground fault detection circuit has different levels of time delay before the SCR is enabled:

6 mA to 15 mA	≤ 135 ms
15 mA to 30 mA	≤ 70 ms
> 30 mA	≤ 20 ms

If a very high GF occurs and a greater than 230 mV signal occurs across the CT for greater than 1.4 ms, the SCR will be immediately enabled.Note that the above equation is for an ideal CT. In practice, the GF threshold can be +/−20% different and should be empirically set.

When the PTT pin is enabled for greater than 16 ms a ST cycle will be enabled. If the ST cycle passes, the SCR will be enabled ~20 ms and the LED will blink once (for breakers, the LED can blink until power down). If the ST cycle fails, the LED will keep blinking and SCR will not be fired. The PTT pin has an internal 50 kΩ pull up resistor. This pin is a CMOS input with hysteresis. To enable the PTT function, the input voltage should go below 1.2 volts.

The MLD pin monitors the phase and zero cross for the AC supply. The MLD circuit clamps the pin voltage to GND and REF. When the pin is clamped at REF, the current on the MLD Pin is compared to an internal current threshold refence such that if the VAC mains voltage is below 87 VRMS, the ST GF threshold will be reduced by 50%. This function provides for an AC under voltage detection which allows for the ST cycle to pass with a lower GF threshold. The AC UVD threshold can be user programmable by changing R2.

Grounded Neutral detection is accomplished by the addition of a GN coil to generate a "Dormant Oscillator" circuit. When a GN condition occurs, both the sense coil and GN coils are mutually coupled and the GN amplifier will oscillate. This oscillation can be observed at the CTG pin. The sensitivity of the GN detection can be changed by capacitor C8 and resistor R6. The frequency of this CTG oscillation needs to be between 2 kHz and 7 kHz. When the voltage of CTG pin is above 1.95 volts within this oscillation frequency, the internal NCS37021 logic will disable the GN amplifier to stop the CTG oscillation. During this time, if the oscillation at the CTG pin is less than 1 kHz, that indicates it is potential GN Fault. After three times of completing this cycle, the SCR driver logic will be enabled. During the Power-Up, the GN amplifier will be powered down for the first approximately 70 ms.

The internal oscillator is trimmed to 25 MHz. If the AC mains frequency changes it can impact the accuracy of the GF and GN sensitivity, for lower ADC mains frequency, the GF trip threshold response time will be slower and the GN sensitivity will be lower.

When the IC logic enables the SCR gate driver circuit, the SCR pin will go high 2 ms after zero cross (for AC Mains at 60 Hz) for ~6ms covering the duration of the MLD half cycle.

Contact **onsemi** for self-test requirement details and noise filtering recommendations.

WAVEFORMS

Ch1: SCM, Ch2: SCR, Ch3: MLD, Ch4: GFT

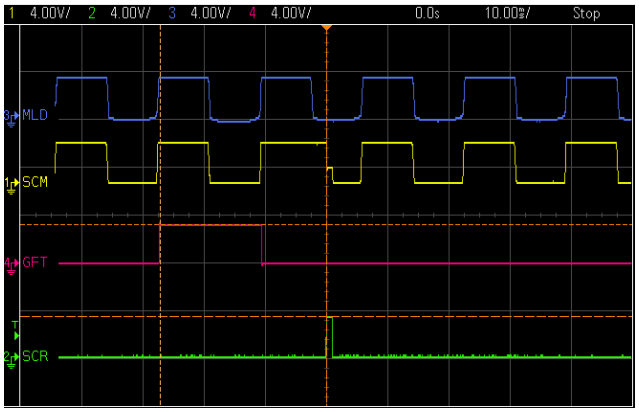


Figure 4. Self Test

Ch1: CTG Ch2: SCR, Ch3: MLD, Ch4: REF

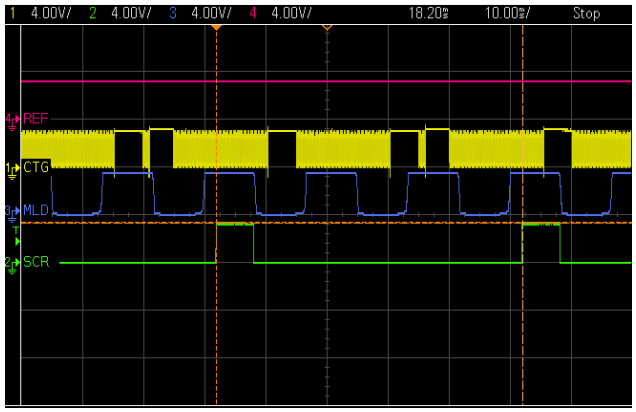


Figure 5. Grounded Neutral Fault Detection

Ch1: IDF Ch2: SCR, Ch3: MLD, Ch4: REF

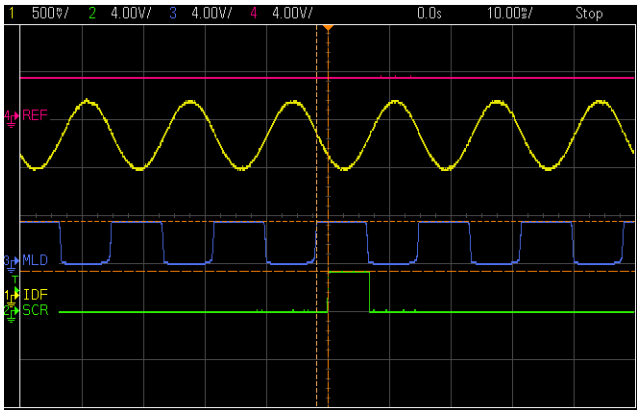


Figure 6. Ground Fault Detection

Ch1: SCM Ch2: SCR, Ch3: MLD, Ch4: PTT

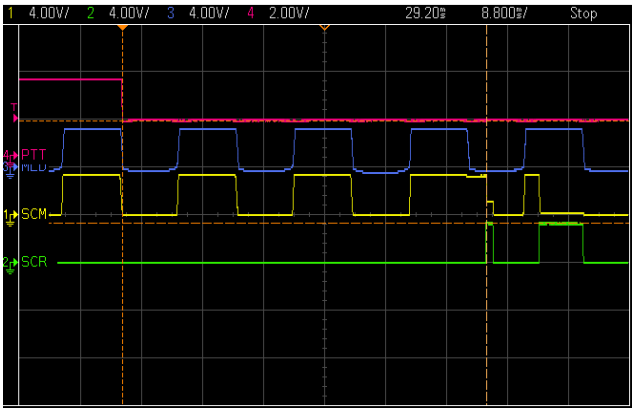


Figure 7. PTT Self Test

ORDERING INFORMATION

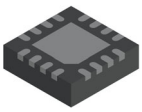
Device	Package	Shipping†
NCS37021MNTWG	QFN16 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

REVISION HISTORY

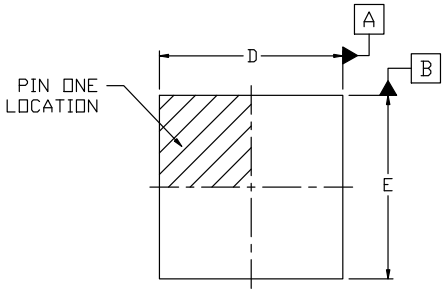
Revision	Description of Changes	Date
1	One bullet edit, one table 4 edit, replace figures 2 and 3, multiple edits table 5, text changes page 8	8/27/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

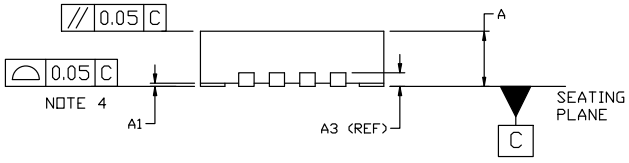


QFN16 3x3, 0.5P
CASE 485FQ
ISSUE B

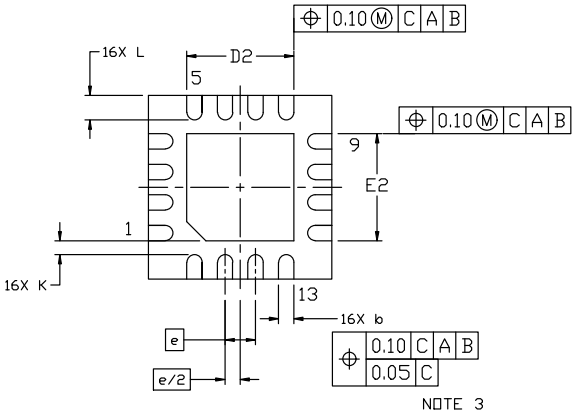
DATE 12 JUL 2022



TOP VIEW



SIDE VIEW

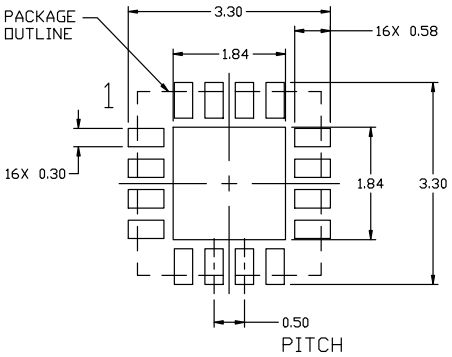


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASUREDBETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	---	---	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	2.90	3.00	3.10
D2	1.65	1.75	1.85
E	2.90	3.00	3.10
E2	1.65	1.75	1.85
e	0.50 BSC		
K	0.18 TYP		
L	0.30	0.40	0.50



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON84763G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN16 3x3, 0.5P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales