High Voltage Linear Regulator

65 V, 100 mA

NCP737

The NCP737 is a high-voltage tolerant linear regulator that offers the benefits of thermally enhanced MSOP8 EP and DFNW8 3x3 (on request) packages and is able to withstand continuous DC or transient input voltages up to 65 V with Ultra-low Quiescent Current below 5 μA. The device is stable with small 1 μF Ceramic Output Capacitors which allows smaller PCB design. The devices features enable pin compatible with standard CMOS logic, internal power good circuit with a user programmable delay via external capacitor. The active high output of power good has open drain with internal current limitation.

Features

- Wide Input Voltage Range: 3 V to 65 V
- Output Voltage Versions:
  - Fixed: 3.3 V (other versions on request)
  - Adjustable: from 1.2 V up to 20.0 V
- ±0.5% Accuracy at T_J = 25 °C
- Very Low Quiescent Current: 5 μA typ.
- Standby Current: 0.5 μA typ.
- Stable with 1 μF Ceramic Output Capacitor
- Power Good with Programmable Delay
- Thermal Shutdown and Current Limit Protection
- Built-in Soft Start Circuit to Suppress Inrush Current
- Available in Thermally Enhanced MSOP8 EP and DFNW8 3x3 (on request) Packages
- Output Active Discharge Functions
- These are Pb-free Devices

Typical Applications

- Telecom, Industrial
- Battery and High-voltage Rail Sensors, Alarms and Security Systems
- Battery Powered Hand Tools
- Home Automation
- Smart Metering
- White Goods

MARKING DIAGRAMS

MSOP8 EP 3x3
(DN SUFFIX)
CASE 846AT

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

On Request

DFNW8 3x3
(ML SUFFIX)
CASE 507AD

XXXXX = Specific Device Marking
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

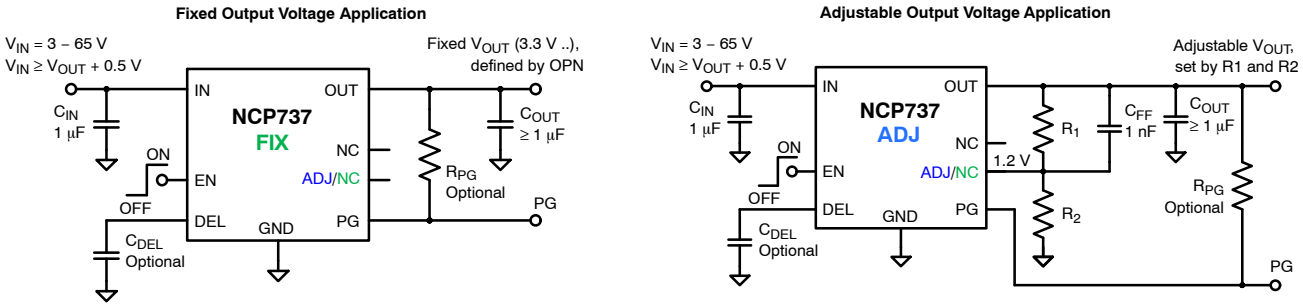


Figure 1. Typical Application Schematics

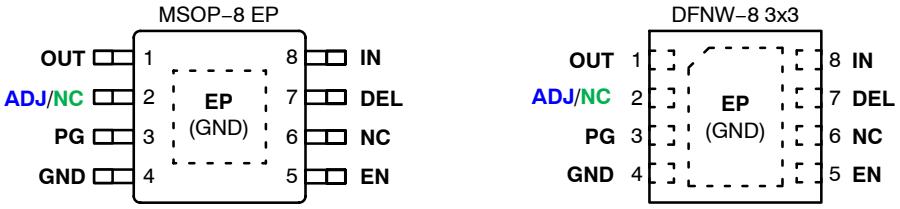
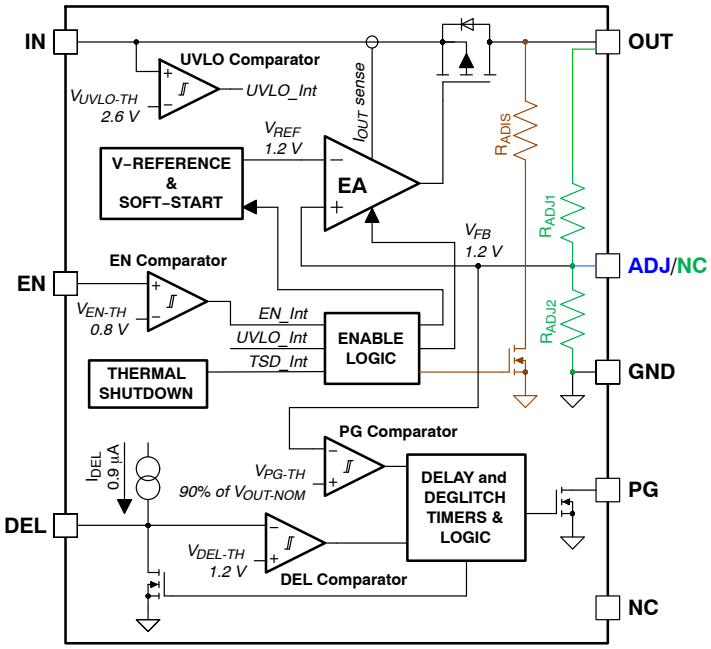


Figure 2. Pin Connections (Top view)



NOTES:
Blue objects are valid for ADJ version only.
Green objects are valid for FIX version only.
Brown objects are valid for active output discharge version only.
Black objects are common to all versions.

Figure 3. Internal Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No. WDFNW8 3x3	Pin No. MSOP8-EP	Pin Name	Description
1	1	OUT	Regulator output pin. A capacitor ≥ 1 μF (effective) must be connected from this pin to GND to assure stability.
2	2	ADJ/NC	This pin is used for adjustable version to set the output voltage by external resistor divider. For fixed voltage versions leave this pin floating.
3	3	PG	Power good output pin. High-Z level for power ok, low level for fail. If not used, could be left unconnected or shorted to GND.
4	4	GND	Power supply ground pin.
5	5	ENA	Chip enable pin (active “H”). Do not leave this pin floating.
6	6	NC	Not connected pin. Leave this pin floating or connect to GND.
7	7	DEL	PG delay pin. Connect a capacitor to GND to adjust the PG delay time. Leave this pin floating if the function is not used.
8	8	IN	Power supply input pin.
EP	EP	EP	Exposed pad. Must be connected to GND potential.

Table 2. ABSOLUTE MAXIMUM RATING

Ratings		Symbol	Value	Unit
IN Pin Voltage Range (Note 1)		V_{IN}	−0.3 to 70	V
OUT Pin Voltage Range	ADJ Version	V_{OUT}	−0.3 to [(V_{IN} + 0.3) or 70; whichever is lower]	V
	FIX Versions		−0.3 to [(V_{IN} + 0.3) or (3 × $V_{OUT-NOM}$); whichever is lower]	
OUT Pin Current (forced into the pin) (Note 4)		I_{OUT-F}	1	mA
EN Pin Voltage Range		V_{ENA}	−0.3 to (Vin + 0.3)	V
ADJ Pin Voltage Range		V_{ADJ}	−0.3 to 3.6	V
DEL Pin Voltage Range		V_{DEL}	−0.3 to 3.6	V
PG Pin Voltage Range		V_{PG}	−0.3 to (V_{in} + 0.3)	V
PG Pin Current		I_{PG}	5	mA
DEL Pin Current		I_{DEL}	5	μA
Maximum Junction Temperature		$T_{J(max)}$	150	°C
Storage Temperature Range		T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)		ESD_{HBM}	2	kV
ESD Capability, Charged Device Model (Note 2)		ESD_{CDM}	1	kV
Moisture Sensitivity Level		MSL	TBD	–
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 3)		T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. Operating the device outside its recommended conditions, but still within its maximum rated limits may not cause immediate damage. However, doing so can lead to reduced performance, unpredictable behavior, and potentially shorten the device’s lifespan or reliability.

NOTE: Pin voltages are related to GND pin.

1. Refer to ELECTRICAL CHARACTERISTIC and APPLICATION INFORMATION for Safe operating Area
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per ANSI/ESDA/JEDEC JS-001, EIA/JESD22-A114
   ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS-002, EIA/JESD22-C101
   Latchup Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D
4. Continuous current forced into OUT pin must be limited at both cases: when $V_{OUT-FORCED}$ > V_{IN} and when $V_{OUT-FOCED}$ > 0 V if LDO is disabled by EN pin (applicable to AD version only). Active discharge function is designed just to discharge output capacitor, not to continuously sink current.

THERMAL CHARACTERISTICS (Note 5)

Characteristic	Symbol	MSOP-8	DFNW8 3x3	Unit
Thermal Resistance, Junction-to-Air	R_{thJA}	38.7	35.4	°C/W
Thermal Resistance, Junction-to-Case (top)	R_{thJCt}	102.0	87.3	°C/W
Thermal Resistance, Junction-to-Case (bottom)	R_{thJCb}	14.7	10.3	°C/W
Thermal Resistance, Junction-to-Board (top)	R_{thJBt}	15.2	10.1	°C/W
Thermal Characterization Parameter, Junction-to-Case (top)	Psi_{JCt}	10.3	7.4	°C/W
Thermal Characterization Parameter, Junction-to-Board [FEM]	Psi_{JB}	15.5	10.2	°C/W

5. Measured according to JEDEC board specification (board 2S2P, Cu layer thickness 1 oz, Cu area 645 mm^2, no airflow). Detailed description of the board can be found in JESD51-7.

Table 3. ELECTRICAL CHARACTERISTICS $-40\ °C \le T_J \le 125\ °C$; $V_{IN} = V_{OUT-NOM} + 0.5\ V$ or 3.0 V (whichever is greater), $I_{OUT} = 10\ \mu A$, $C_{IN} = 1\ \mu F$, $C_{OUT} = 1\ \mu F$ (Note 6), ADJ pin connected to VOUT pin, unless otherwise noted. Typical values are at $T_A = +25\ °C$. (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
INPUT						
Operating Input Voltage		V_{IN}	3	–	65	V
Input Voltage UVLO Threshold	V_{IN} rising	$V_{UVLO-TH}$	1.7	2.6	3.0	V
Input Voltage UVLO Hysteresis	V_{IN} falling	$V_{UVLO-HY}$	0.01	0.3	0.5	V
OUTPUT						
Output Voltage Accuracy (Note 8)	$T_J = 25\ °C$	V_{OUT}	−0.5	V_{NOM25}	0.5	%
	$T_J = -40\ °C$ to 125 °C		−1.5	–	1.5	
ADJ Reference Voltage	ADJ version only	V_{ADJ}	–	1.2	–	V
ADJ Input Current	ADJ version only, $V_{ADJ} = 1.2\ V$	I_{ADJ}	−100	10	100	nA
Output Voltage Range	ADJ version only	$V_{OUT-ADJ}$	V_{ADJ}	–	20	V
Line Regulation	$V_{IN} = (V_{OUT-NOM} + 0.5\ V)$ to 65 V, $V_{IN} \ge 3.0\ V$	$\Delta V_O/\Delta V_I$	–	0.01	0.2	$\%V_{OUT}$
Load Regulation	$I_{OUT} = 10\ \mu A$ to 100 mA	$\Delta V_O/\Delta I_O$	–	0.1	0.4	$\%V_{OUT}$
Dropout Voltage (Note 9)	$I_{OUT} = 100$ mA, all $V_{OUT-NOM}$ versions	V_{DO}	–	265	500	mV
Output Current Limit	$V_{OUT-FORCED} = V_{OUT-NOM} - 100$ mV	I_{OLIM}	110	200	300	mA
Short Circuit Current	$V_{OUT} = 0\ V$	I_{OSC}	110	200	300	
Active Discharge Resistance	$V_{EN} = 0V$	R_{ADIS}	–	50	–	Ω
CURRENT CONSUMPTION						
Disable Current	$V_{EN} = 0\ V$, $V_{IN} = (V_{OUT-NOM} + 0.5\ V)$ to 65 V, $V_{IN} \ge 3.0\ V$	I_{DIS}	–	0.5	5	μA
Quiescent Current	$I_{OUT} = 0$ mA, $V_{IN} = (V_{OUT-NOM} + 0.5\ V)$ to 65 V, $V_{IN} \ge 3.0\ V$	I_Q	–	5	15	μA
Ground Current	$I_{OUT} = 100$ mA	I_{GND}	–	300	500	μA
ENABLE THRESHOLDS						
Enable Voltage Threshold	V_{EN} rising	V_{EN-TH}	0.3	0.8	1.2	V
Enable Voltage Hysteresis	V_{EN} falling	V_{EN-HY}	0.01	0.1	0.3	V
Enable Pin Current	$V_{EN} \le 65\ V$	I_{EN}	–	0.1	1	μA
PSRR AND NOISE						
Power Supply Ripple Rejection	$V_{OUT} = 3.3\ V$ (ADJ), $C_{FF} = 10$ nF, $C_{OUT} = 2.2\ \mu F$, $I_{OUT} = 100$ mA	PSRR				dB
	f = 100 Hz, 0.1 V_{p-p}		–	77	–	
	f = 1 kHz, 0.1 V_{p-p}		–	73	–	
	f = 100 kHz, 0.1 V_{p-p}		–	30	–	

Table 3. ELECTRICAL CHARACTERISTICS $-40\ °C \le T_J \le 125\ °C$; $V_{IN} = V_{OUT-NOM} + 0.5\ V$ or 3.0 V (whichever is greater), $I_{OUT} = 10\ \mu A$, $C_{IN} = 1\ \mu F$, $C_{OUT} = 1\ \mu F$ (Note 6), ADJ pin connected to VOUT pin, unless otherwise noted. Typical values are at $T_A = +25\ °C$. (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
PSRR AND NOISE						
Output Noise Voltage	V_{OUT} = 3.3 V (ADJ), C_{FF} = 10 nF, C_{OUT} = 2.2 μF, I_{OUT} = 100 mA	V_{NOISE}				μV_{rms}
	f = 10 Hz to 100 kHz		–	83	–	
	f = 10 Hz to 1 MHz		–	130	–	
POWER GOOD, DELAY						
Power Good V_{OUT} Threshold	V_{OUT} rising	V_{PG-THR}	85%	90%	95%	$V_{OUT-NOM}$
	V_{OUT} falling	V_{PG-THF}	83%	88%	93%	
Power Good V_{OUT} Hysteresis		V_{PG-HY}	–	2.5%	4%	
Power Good Voltage Low	V_{OUT} = 80% $V_{OUT-NOM}$, I_{PG} = 1 mA	V_{PG-LO}	–	0.05	0.25	V
Power Good Leakage Current	$V_{PG} = V_{OUT-NOM}$	I_{PG}	–	0.02	1	μA
Delay pin Current	V_{DEL} = 0 V	I_{DEL}	0.3	0.9	2	μA
Delay pin Threshold Voltage	V_{DEL} rising	V_{DEL-TH}	1.1	1.2	1.3	V
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		T_{SD}	–	170	–	°C
Thermal Shutdown Hysteresis		T_{SH}	–	15	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Effective capacitance, including the effect of DC bias, tolerance and temperature. See the Application Information section for more information.
7. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_J = T_A = 25\ °C$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
8. Typical value of output voltage at 25 °C is set during testing to value $V_{NOM25} = V_{NOM} * 1.003$ (what means +0.3% above V_{NOM}) to have symmetrical deviation of V_{OUT} to V_{NOM} over the whole temperature range. Note that V_{OUT} at 25 °C is at it's maximum. See V_{OUT} vs. Temperature chart below for details.
9. Dropout voltage is measured when the output voltage falls 100 mV below the nominal output voltage. ADJ version is measured with ADJ pin connected to resistor divider which sets V_{OUT} to 3.3 V. Limits are valid for all voltage versions.

TYPICAL CHARACTERISTICS

(V_{IN} = $V_{OUT-NOM}$ + 0.5 V or 3.0 V (whichever is greater), I_{OUT} = 10 μA, C_{IN} = 1 uF, C_{OUT} = 1 μF (effective capacitance), ADJ pin connected to OUT pin, T_J = 25 °C unless otherwise noted)

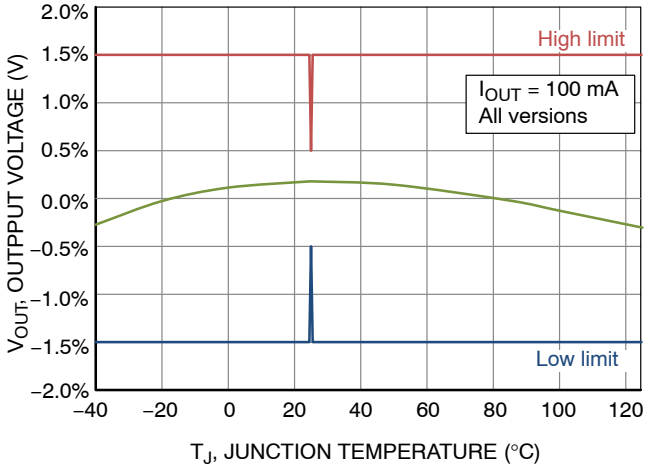


Figure 4. Output Voltage vs. Temperature

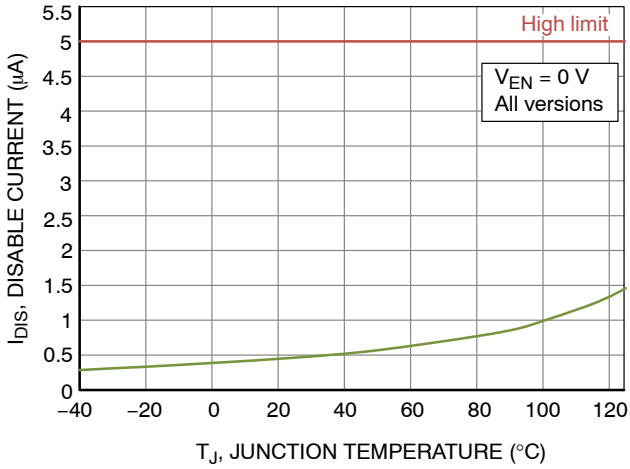


Figure 5. Disable Current vs. Temperature

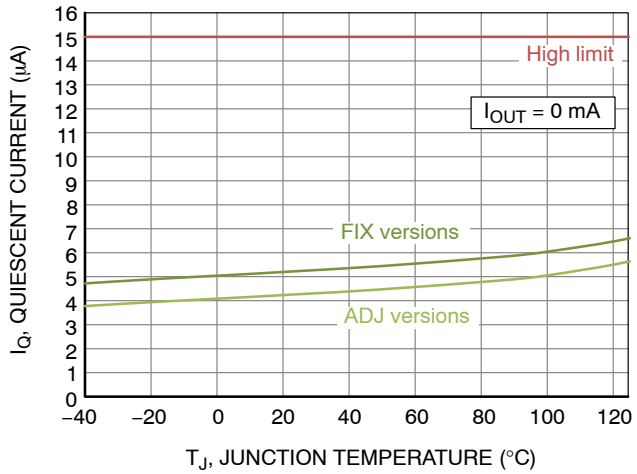


Figure 6. Quiescent Current vs. Temperature

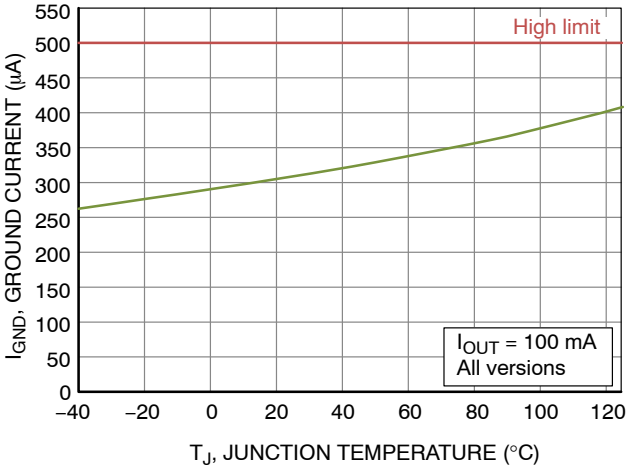


Figure 7. Ground Current vs. Temperature

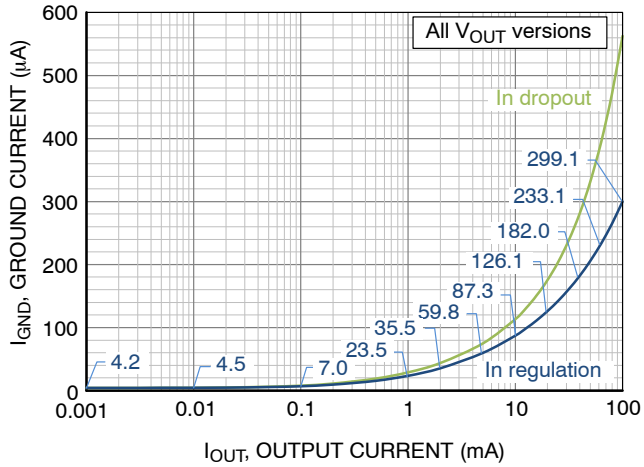


Figure 8. Ground Current vs. Output Current

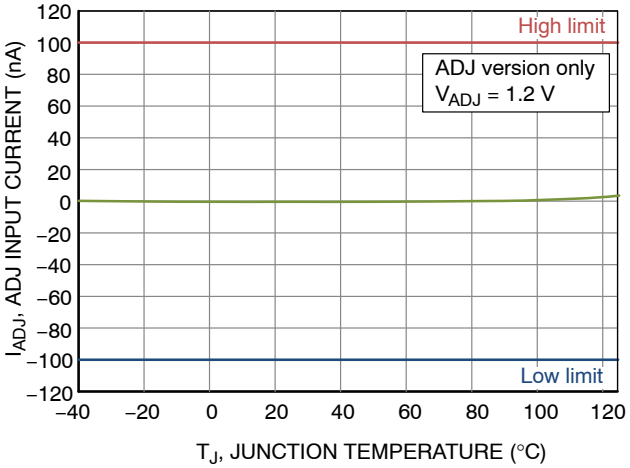


Figure 9. ADJ Input Current vs. Temperature

TYPICAL CHARACTERISTICS

(V_{IN} = $V_{OUT-NOM}$ + 0.5 V or 3.0 V (whichever is greater), I_{OUT} = 10 μA, C_{IN} = 1 uF, C_{OUT} = 1 μF (effective capacitance), ADJ pin connected to OUT pin, T_J = 25 °C unless otherwise noted)

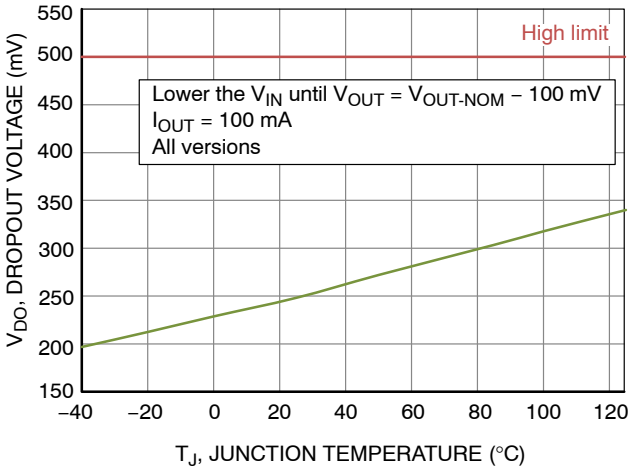


Figure 10. Dropout Voltage vs. Temperature

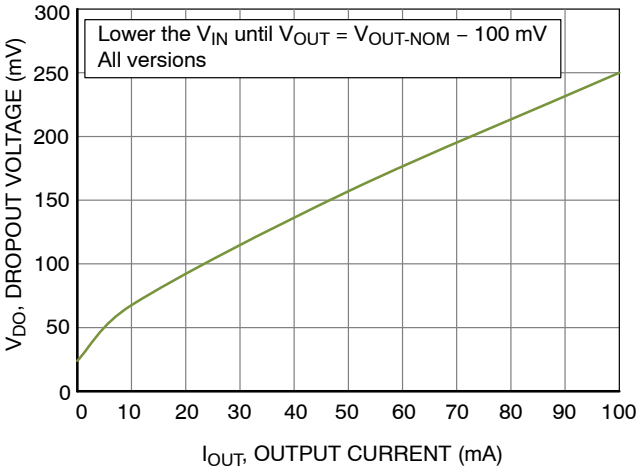


Figure 11. Dropout Voltage vs. Output Current

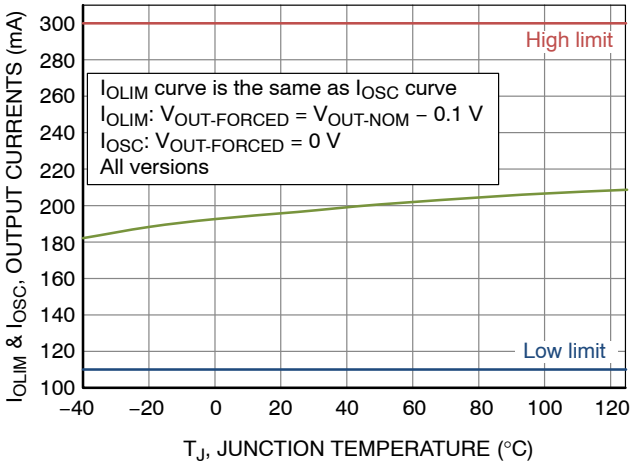


Figure 12. Output Current Limit and Short Circuit Current vs. Temperature

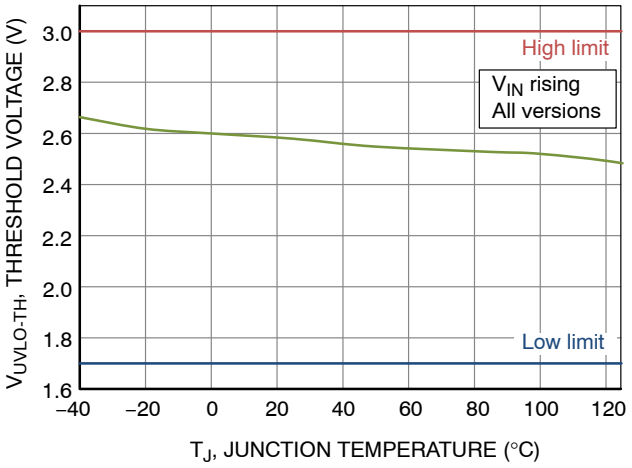


Figure 13. IN Voltage UVLO Threshold vs. Temperature

TYPICAL CHARACTERISTICS

(V_{IN} = $V_{OUT-NOM}$ + 0.5 V or 3.0 V (whichever is greater), I_{OUT} = 10 μA, C_{IN} = 1 uF, C_{OUT} = 1 μF (effective capacitance), ADJ pin connected to OUT pin, T_J = 25 °C unless otherwise noted)

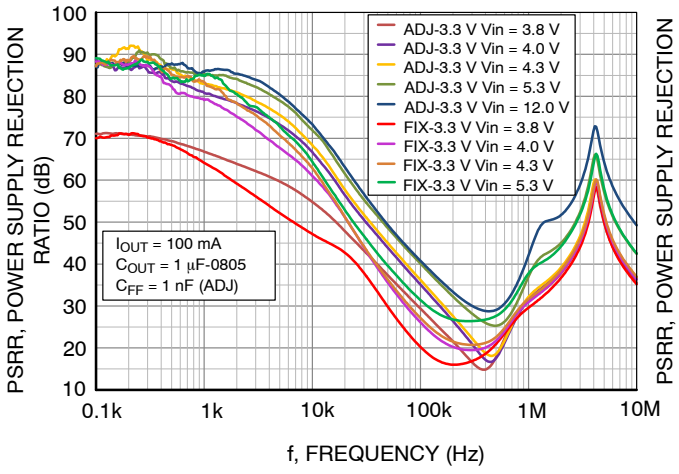


Figure 14. PSRR of ADJ-set-3.3 V & FIX-3.3 V vs. V_{IN} @ 1 μF

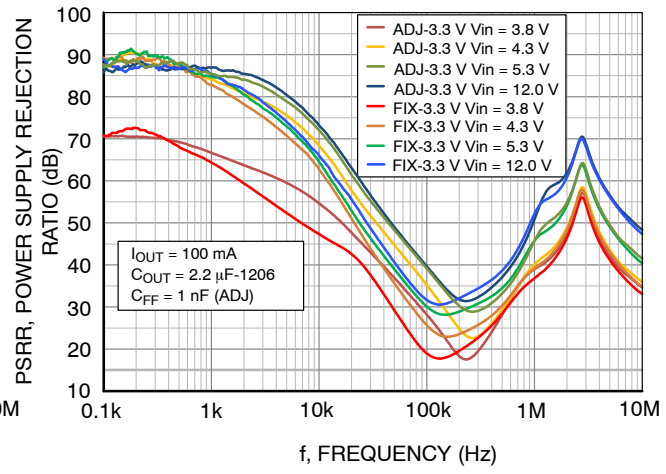


Figure 15. PSRR of ADJ-set-3.3 V & FIX-3.3 V vs. V_{IN} @ 2.2 μF

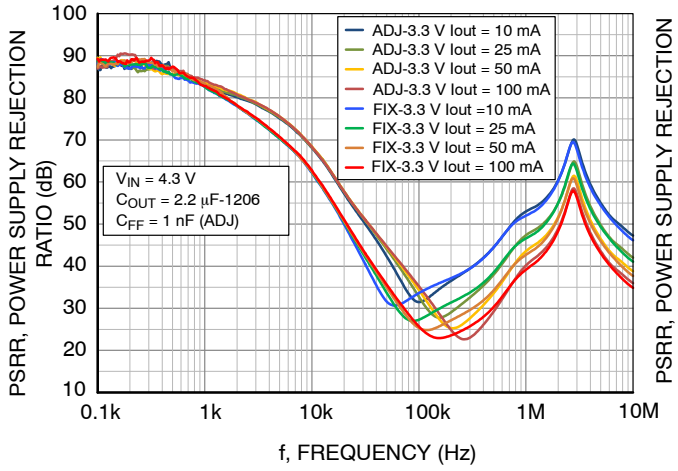


Figure 16. PSRR of ADJ-set-3.3 V & FIX-3.3 V vs. I_{OUT} @ 4.3 V, 2.2 μF

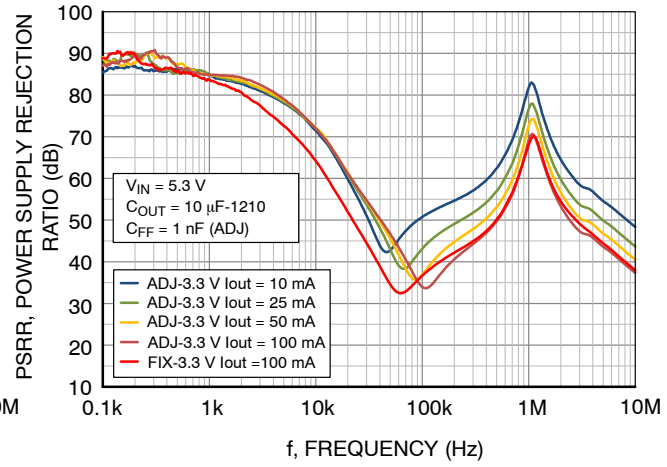


Figure 17. PSRR of ADJ-set-3.3 V & FIX-3.3 V vs. I_{OUT} @ 5.3 V, 10 μF

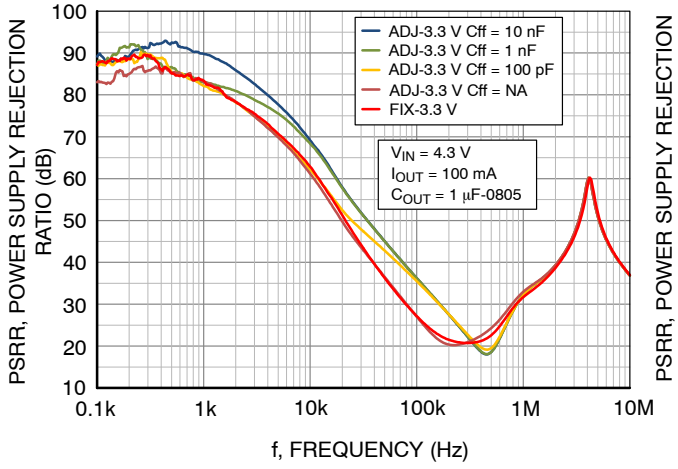


Figure 18. PSRR of ADJ-set-3.3 V vs. C_{FF} vs. FIX-3.3 V

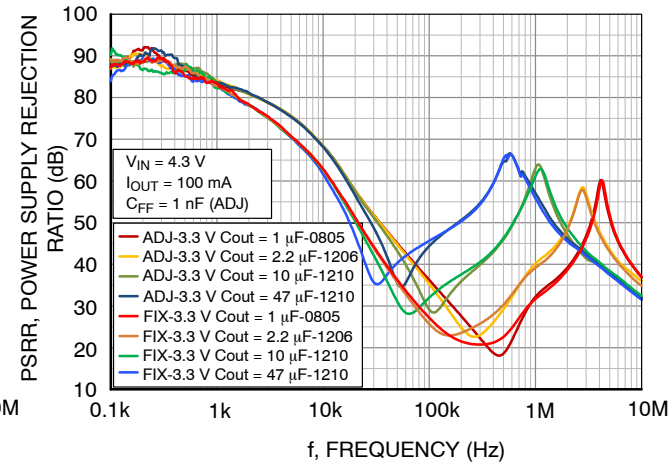


Figure 19. PSRR of ADJ-set-3.3 V & FIX-3.3 V vs. C_{OUT}

TYPICAL CHARACTERISTICS

(V_{IN} = $V_{OUT-NOM}$ + 0.5 V or 3.0 V (whichever is greater), I_{OUT} = 10 μA, C_{IN} = 1 uF, C_{OUT} = 1 μF (effective capacitance), ADJ pin connected to OUT pin, T_J = 25 °C unless otherwise noted)

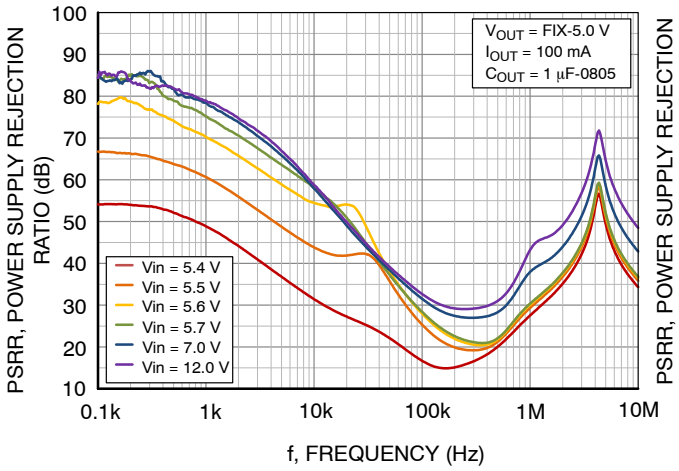


Figure 20. PSRR of FIX-5.0 V vs. V_{IN}

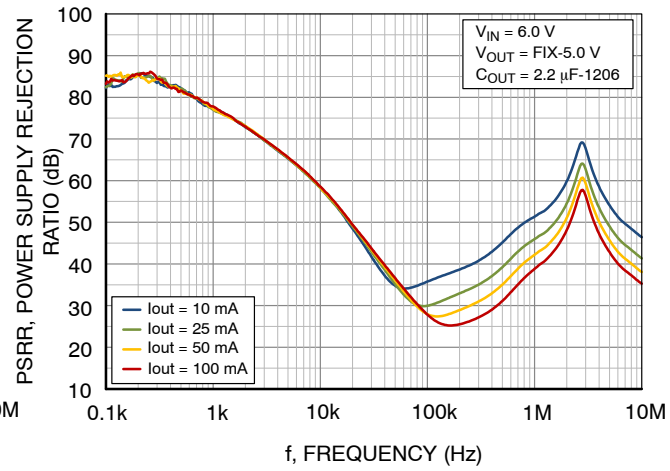


Figure 21. PSRR of FIX-5.0 V vs. I_{OUT}

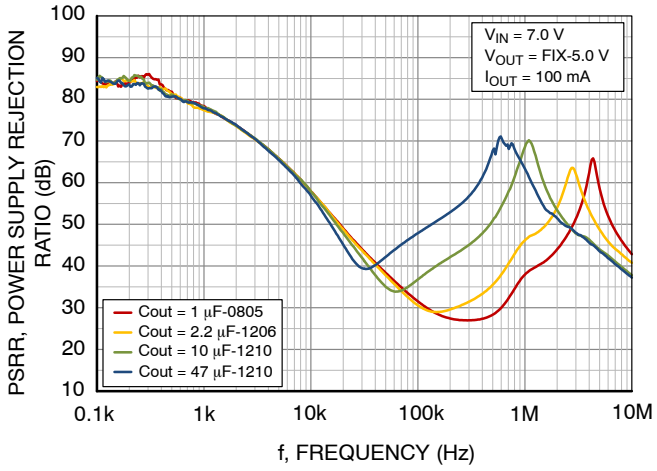


Figure 22. PSRR of FIX-5.0 V vs. C_{OUT}

TYPICAL CHARACTERISTICS

(V_{IN} = $V_{OUT-NOM}$ + 0.5 V or 3.0 V (whichever is greater), I_{OUT} = 10 μA, C_{IN} = 1 uF, C_{OUT} = 1 μF (effective capacitance), ADJ pin connected to OUT pin, T_J = 25 °C unless otherwise noted)

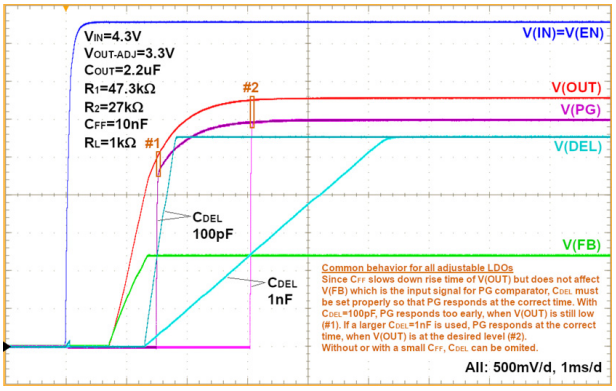


Figure 23. Startup by V_{IN}, ADJ-set-3.3 V, C_{DLY} Function

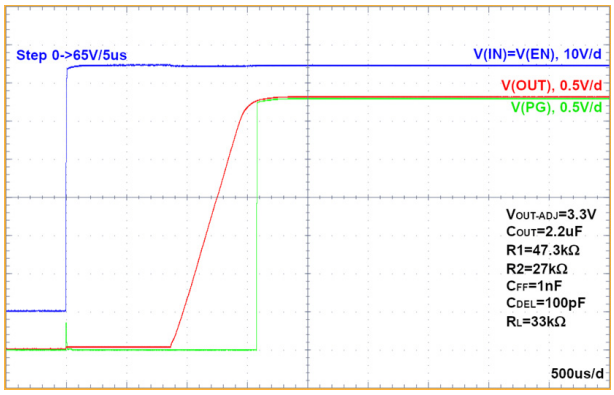


Figure 24. Startup by V_{IN}, 0 → 65 V / 5 μs

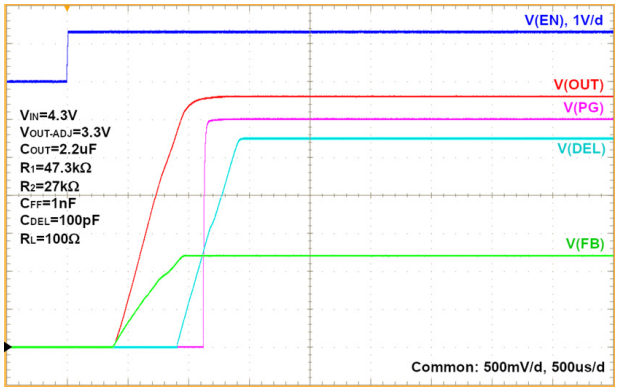


Figure 25. Startup by V_{EN}

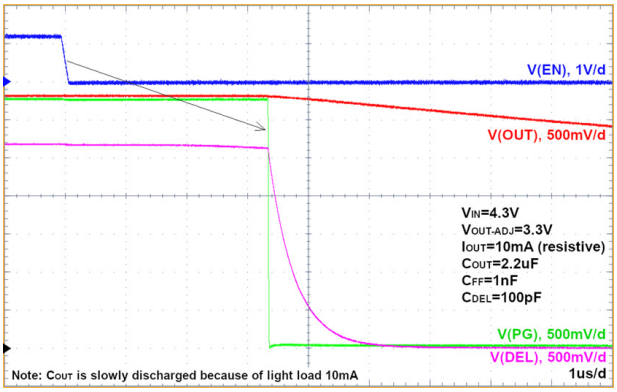


Figure 26. Shutdown by V_{EN}

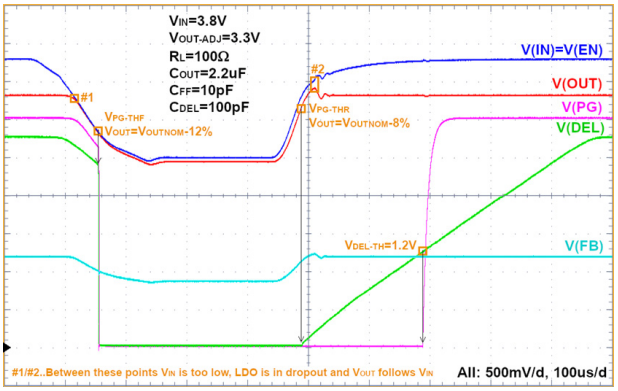


Figure 27. PG Behavior During V_{IN} Fail

TYPICAL CHARACTERISTICS

(V_{IN} = $V_{OUT-NOM}$ + 0.5 V or 3.0 V (whichever is greater), I_{OUT} = 10 μA, C_{IN} = 1 uF, C_{OUT} = 1 μF (effective capacitance), ADJ pin connected to OUT pin, T_J = 25 °C unless otherwise noted)

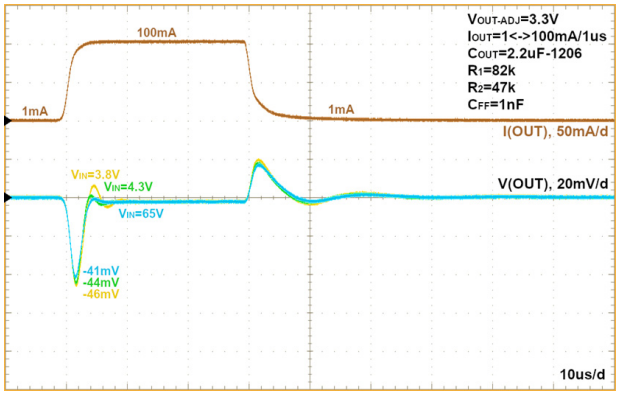


Figure 28. Load Trans. Response vs. V_{IN}

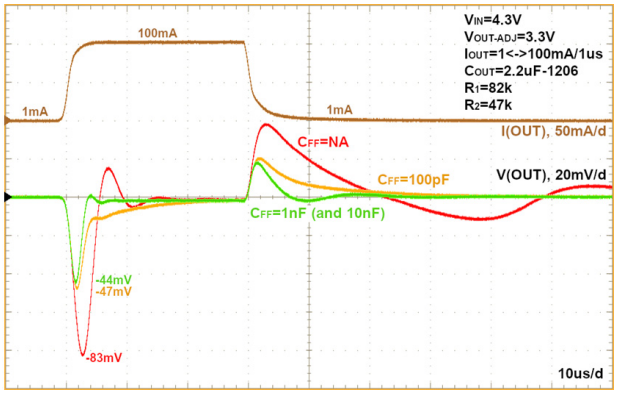


Figure 29. Load Trans. Response vs. C_{FF}

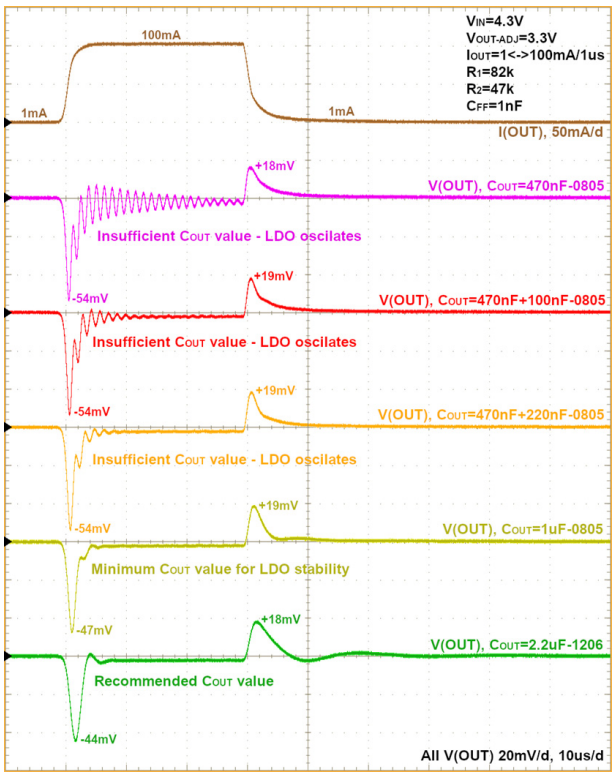


Figure 30. Load Trans Response vs. Smaller C_{OUTs}

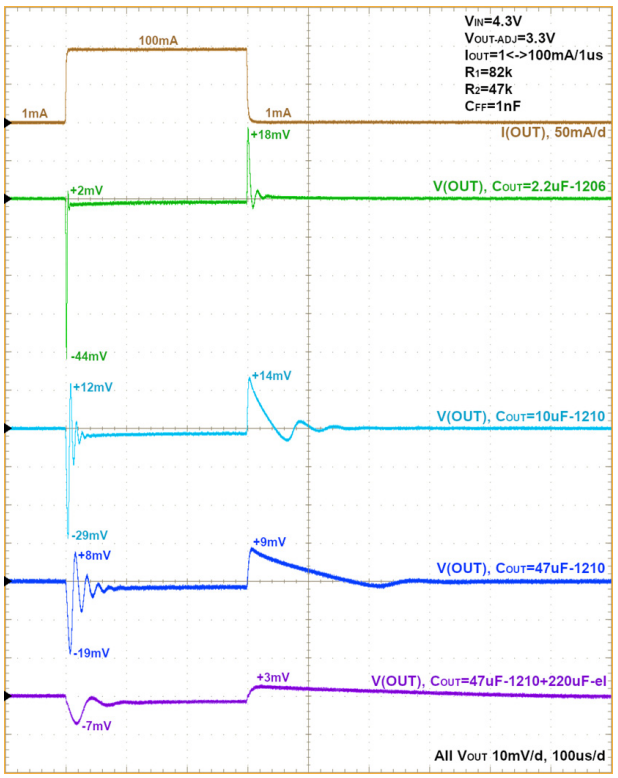


Figure 31. Load Trans. Response vs. Bigger C_{OUTs}

TYPICAL CHARACTERISTICS

(V_{IN} = $V_{OUT-NOM}$ + 0.5 V or 3.0 V (whichever is greater), I_{OUT} = 10 μA, C_{IN} = 1 uF, C_{OUT} = 1 μF (effective capacitance), ADJ pin connected to OUT pin, T_J = 25 °C unless otherwise noted)

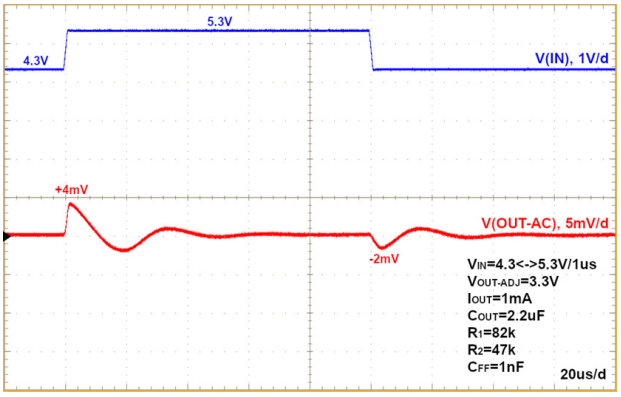


Figure 32. Line Trans. Response, 1 V Step, 1 mA

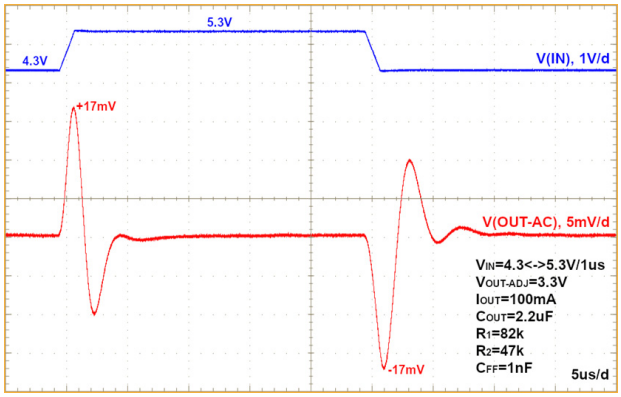


Figure 33. Line Trans. Response, 1 V Step, 100 mA

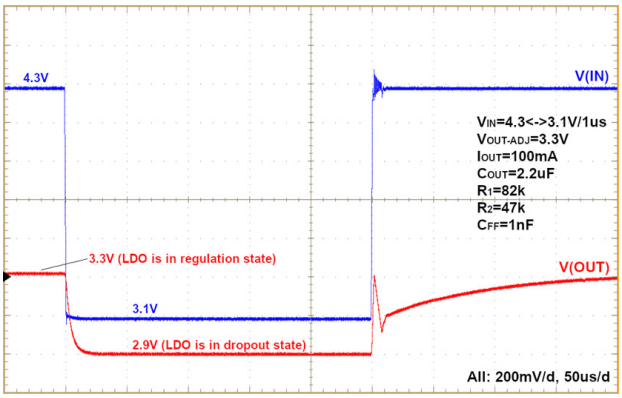


Figure 34. Line Trans. Response to/from Dropout

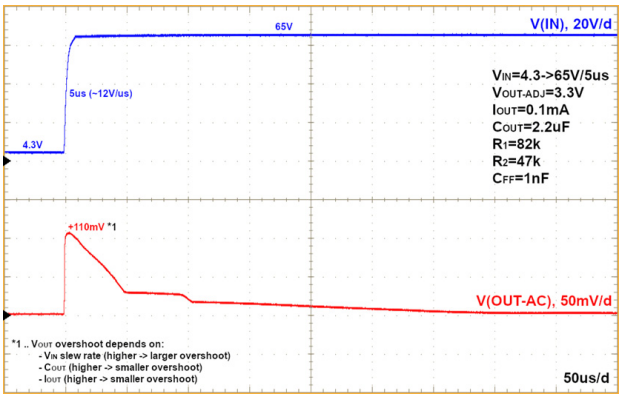


Figure 35. Line Trans. Response, Max. Step

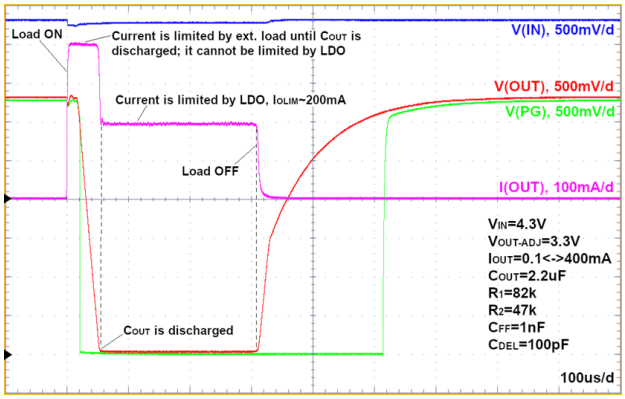


Figure 36. Output Overload by 400 mA

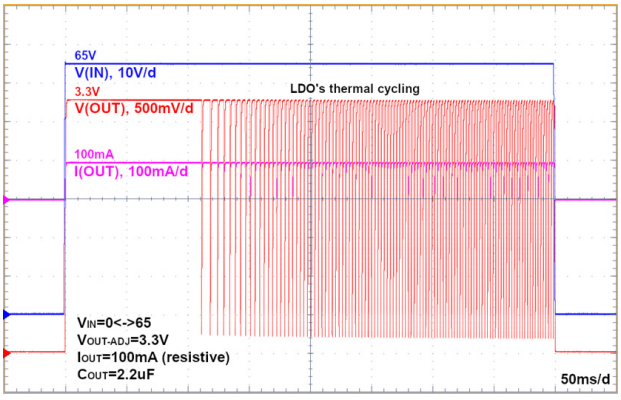


Figure 37. Thermal Overload by 65 V/100 mA

TYPICAL CHARACTERISTICS

(V_{IN} = $V_{OUT-NOM}$ + 0.5 V or 3.0 V (whichever is greater), I_{OUT} = 10 μA, C_{IN} = 1 uF, C_{OUT} = 1 μF (effective capacitance), ADJ pin connected to OUT pin, T_J = 25 °C unless otherwise noted)

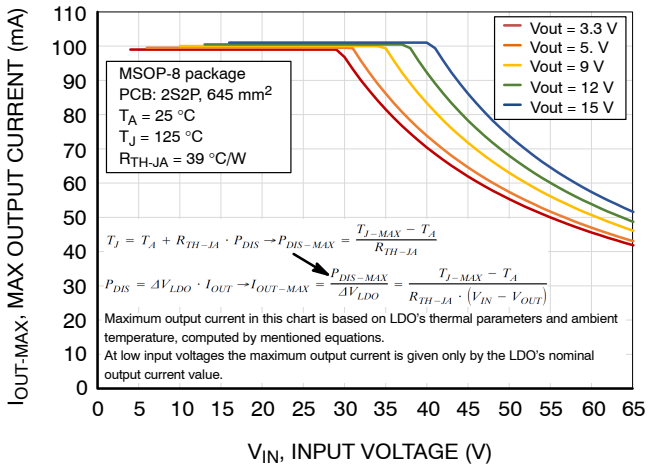


Figure 38. Maximum Output Current, MSOP-8

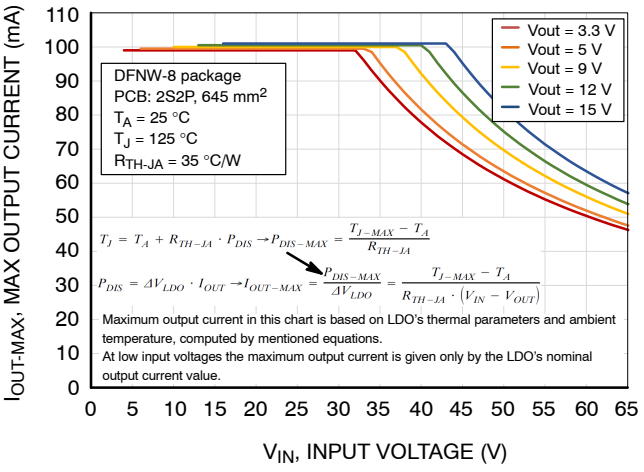


Figure 39. Maximum Output Current, DFNW-8

APPLICATIONS INFORMATION

Input Capacitor Selection (C_{in})

Input ceramic capacitor (X5R, X7R etc.) connected as close as possible to the input pin of NCP737 regulator is necessary. Higher capacitance and lower ESR will improve the overall dynamic parameters and minimize the impact of input traces. Minimum value is 1 μF and recommend value is the same as output capacitor value. Maximum value is not limited.

In cases when LDO's input power supply has poor load transient response or has high output impedance (ex: long connection wires) then the input capacitor needs to be significantly bigger (in range of tens of μF) to avoid of LDO's input voltage drop below the minimum level (given by the sum of output voltage and dropout voltage), otherwise the output voltage drop could happen.

Output Capacitor Selection (C_{OUT})

The LDO requires the output capacitor connected as close as possible to the output and ground pins. The LDO is designed to remain stable with output capacitor's effective capacitance (under operating conditions of DC bias and temperature) in range from 1 μF to 1000 μF and ESR from 1 mΩ to 100 mΩ (over frequency range from 100 kHz to 1 MHz). Recommended output capacitor value is 2.2 μF or higher. The ceramic X5R, X7R or better type is recommended due to its low capacitance variations over the specified temperature range, low ESR and ESL. When selecting the output capacitor, the value deviation caused by temperature and DC bias voltage needs to be considered. Especially for small package size capacitors below 0805 the effective capacitance drops rapidly with the applied DC bias voltage (refer the capacitor's datasheet for details).

Larger capacitance and lower capacitor ESR improve the load transient response, PSRR and output voltage noise.

Output Voltage

NCP737 part is available in several fixed output voltage versions (FIX) and adjustable version (ADJ). ADJ version allows connection of external feed forward capacitor (C_{FF}) which improves dynamic performance (PSRR, noise, transient response) but prolongs the startup time, see graphs in Typical Characteristics section.

Application with FIX version provides output voltage equal to LDO's nominal output voltage $V_{OUT-NOM}$ (given by OPN, see Ordering information table). Application with ADJ version allows adjustability of the output voltage by external resistor divider connected to OUT, ADJ and GND pins. Then the output voltage can be computed by the following equation:

$$V_{OUT} = V_{ADJ} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ADJ} \cdot R_1 \qquad \text{(eq. 1)}$$

Where:

V_{OUT} is output voltage of the circuit with resistor divider (adjustable application)

V_{ADJ} is the ADJ reference voltage (1.2 V)

I_{ADJ} is the ADJ pin input current

R_1 is the upper resistor in resistor divider

R_2 is the lower resistor in resistor divider

The typical value of IADJ is less than 10 nA, but the guaranteed max. value over the entire temperature range is 100 nA. For junction temperatures below 85 °C, I_{ADJ} is negligible and the values of R_1 and R_2 can be up to hundreds of kΩ. For higher junction temperatures, values should be below a hundred kΩ. Generally, when resistor divider current I_{R1R2} is 100x higher than I_{ADJ}, the V_{OUT} error caused by I_{ADJ} is less than 1%.

Recommended values of R_1 and R_2 are in range from 1 kΩ to about 300 kΩ. Higher resistor values are better from current consumption point of view.

Next table lists recommended resistor divider values (R_1 and R_2) selected from E24 series.

Table 4. EXAMPLES OF RESISTORS DIVIDER VALUES

V_{OUT}	R_1	R_2	V_{OUT2}	err	I_{R1R2}
[V]	[kΩ]	[kΩ]	[V]	[%]	[μA]
1.2	Short	None	1.200	0.00	N/A
2.5	39	36	2.500	0.00	33.3
3.3	82	47	3.294	−0.19	25.5
5.0	150	47	5.030	0.60	25.5
9.0	300	51	8.965	−0.39	23.5
10.0	220	30	10.000	0.00	40.0
12.0	270	30	12.000	0.00	40.0
15.0	150	13	15.046	0.31	92.3

NOTE: For T_J in range from −40 °C to 125 °C.

Where:

V_{OUT} [V] is desired output voltage

V_{OUT2} [V] is calculated output voltage

err [%] is difference between desired and calculated output voltage

I_{R1R2} [%] is current through R1 and R2

Computed by equation 1, I_{ADJ} neglected (for I_{ADJ} = 0).

Of course, the table above is just an example and other values of output voltage divider resistors are possible.

Startup

In the NCP737 device there are two main internal signals which triggers the startup process, the IN-pin undervoltage lockout (UVLO) signal and enable signal. The first one comes from UVLO comparator, which monitors if the IN-pin voltage is high enough, while the second one comes

from EN-pin comparator. Both comparators have embedded hysteresis to be insensitive to input noise. When both signals turn into high level, the startup process is initiated.

At adjustable application, when the feed-forward capacitor (C_{FF}) is used to improve dynamic behavior, it unintentionally influences the rise time and the shape of output voltage ramp-up, which is common behavior for all adjustable LDOs. When C_{FF} is very low (tens of pA) or not connected, the output voltage rises linearly. However, higher C_{FF} values slow down V_{OUT} rise time but do not affect V_{FB} which is the input signal to the PG comparator. It is then necessary to set C_{DEL} properly so that PG responds at the correct time. This and other startup behaviors are shown at Typical Characteristics section.

Thermal Protection

When the LDO junction temperature exceeds the thermal shutdown threshold value, the device internally disables itself. The IC remains in disabled state until the junction temperature drops by the thermal shutdown hysteresis value, at which point the LDO is re-enabled.

The thermal shutdown feature provides protection against overheating due to application failure and is not intended for normal work use.

Power Dissipation

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum power dissipation is dependent on the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature. The maximum power dissipation can be computed by one of the following equations:

$$P_{DIS} = \frac{T_J - T_A}{R_{\theta JA}} \qquad \text{(eq. 2)}$$

or

$$P_{DIS} = \frac{T_J - T_A}{R_{\theta JB}} \qquad \text{(eq. 3)}$$

Where:

- T_J is the desired junction temperature
- T_A is the ambient temperature
- T_B is the board temperature
- $R_{\theta JA}$ is junction to ambient thermal resistance
- $R_{\theta JB}$ is junction to board thermal resistance

If we substitute the maximum junction temperature for the junction temperature $T_J = T_{J(MAX)}$, we obtain a maximum allowable power dissipation $P_{DIS(MAX)}$. If higher than maximum power dissipation is applied ($P_{DIS} > P_{DIS(MAX)}$), the device will be overheated ($T_J > T_{J(MAX)}$).

We can substitute for the power dissipation the following equation:

$$P_{DIS} = (V_{IN} - V_{OUT}) \cdot I_{OUT} \qquad \text{(eq. 4)}$$

To obtain:

$$P_{DIS} = \frac{T_J - T_X}{R_{\theta JX}} = (V_{IN} - V_{OUT}) \cdot I_{OUT} \qquad \text{(eq. 5)}$$

And the express the output current:

$$I_{OUT} = \frac{T_J - T_X}{R_{\theta JX} \cdot (V_{IN} - V_{OUT})} \qquad \text{(eq. 6)}$$

Where:

- T_X is T_A resp. T_B
- $R_{\theta JX}$ is $R_{\theta JA}$ resp. $R_{\theta JB}$

And similarly, if we substitute the maximum junction temperature for the junction temperature $T_J = T_{J(MAX)}$, we obtain an equation for the maximum allowable load current $I_{OUT(MAX)}$.

$$I_{OUT(MAX)} = \frac{T_{J(MAX)} - T_X}{R_{\theta JX} \cdot (V_{IN} - V_{OUT})} \qquad \text{(eq. 7)}$$

Then, if higher load current than maximum load current is applied ($I_{OUT} > I_{OUT(MAX)}$), the device will be overheated ($T_J > T_{J(MAX)}$).

Maximum allowable output current graphs are shown in Typical Characteristics section.

PCB Layout Recommendations

To obtain good LDO's stability and the best transient, PSRR and output voltage noise performance, place both C_{IN} and C_{OUT} capacitors as close as possible to the device pins, make the PCB traces wide and short and place capacitors to the same PCB Cu layer as the LDO is (avoid connections through vias). The same rules should be applied to the connections between C_{OUT} and the load – the less parasitic impedance the better dynamic performance at the point of load.

Regarding high impedance ADJ and DEL pins, prevent capacitive coupling of their traces to any switching signals in the application.

EN input doesn't need any special care.

GND pin and exposed pad should be connected to PCB GND plane for the best power spreading out of the chip. NC pins could be connected the PCB GND plane as well.

ORDERING INFORMATION (Note 10)

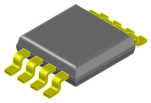
Part Number	Voltage Option ($V_{OUT-NOM}$)	OUT Active Discharge	Marking	Package	Shipping†
NCP737ADNADJR2G	ADJ	Yes	737AAD	MSOP8 EP 3x3 Pb-free	4000 / Tape & Reel
NCP737ADN330R2G	FIX 3.3 V	Yes	737A33		

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

10. To order DFNW8 3x3 package, other FIX voltage version or non output active discharge version, please contact your **onsemi** sales representative.

REVISION HISTORY

Revision	Description of Changes	Date
0	Application schematic, pinout diagrams and internal block diagram updated by higher quality pictures. Ordering information table – added making and shipping information.	5/22/2025
1	Updated DFNW Thermal Characteristics values.	9/19/2025
2	Added the graphs. Changed the Applications Information section.	5/29/2026



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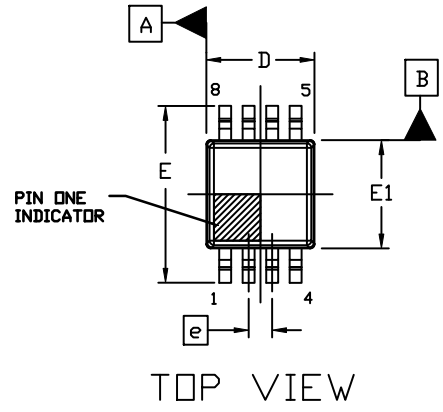
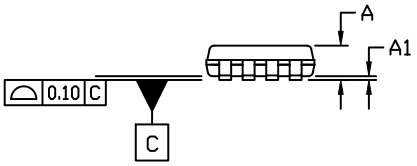
CASE 846AT
ISSUE O

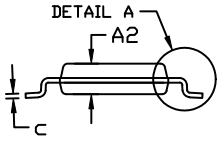
DATE 01 OCT 2020



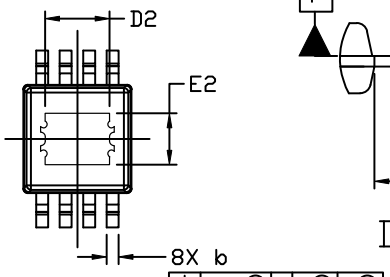
TOP VIEW



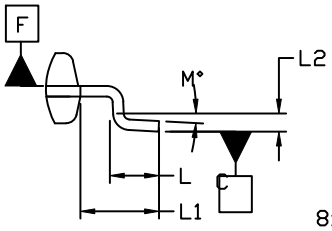
SIDE VIEW



END VIEW



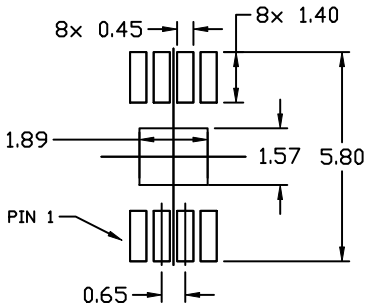
BOTTOM VIEW NOTE 3



DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS b AND c APPLY TO THE PLATED LEADS.
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. PIN 1 INDICATOR IS LOCATED HERE. MAY APPEAR AS A LASER MARKED, OR A MOLDED (CIRCLE OR HALF MOON), INDENT.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.10	0.15
A2	0.813	0.863	0.914
b	0.28	---	0.38
c	0.139	---	0.23
D	2.90	3.00	3.10
D2	1.50	1.70	1.80
E	4.775	4.876	4.978
E1	2.90	3.00	3.10
E2	1.14	1.40	1.50
e	0.65 BSC		
L	0.40	---	---
L1	0.94 REF		
L2	0.25 REF		
M	0°	---	8°



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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