

Linear Voltage Regulator - Ultra-Low Quiescent Current, Ultra-Low Noise, LDO

200 mA

NCP702

Noise sensitive applications such as Phase Locked Loops, Oscillators, Frequency Synthesizers, Low Noise Amplifiers and other Precision Instrumentation require very clean power supplies. The NCP702 is a 200 mA LDO that provides the engineer with a very stable, accurate voltage with ultra-low noise and very high Power Supply Rejection Ratio (PSRR), making it suitable for RF applications. The device doesn't require an additional noise bypass capacitor to achieve ultra-low noise performance. In order to optimize performance for battery operated portable applications, the NCP702 employs an Adaptive Ground Current feature for ultra-low ground current consumption during light-load conditions.

Features

- Operating Input Voltage Range: 2.0 V to 5.5 V
- Available in Fixed Voltage Options: 0.8 to 3.5 V
Contact Factory for Other Voltage Options
- Output Voltage Trimming Step: 2.5 mV
- Ultra-Low Quiescent Current of Typ. 10 μ A
- Ultra-Low Noise: 11 μ V_{RMS} from 100 Hz to 100 kHz
- Very Low Dropout: 140 mV Typical at 200 mA
- $\pm 2\%$ Accuracy Over Full Load/Line/Temperature
- High PSRR: 68 dB at 1 kHz
- Thermal Shutdown and Current Limit Protections
- Internal Soft-Start to Limit the Turn-On Inrush Current
- Stable with a 1 μ F Ceramic Output Capacitor
- Available in TSOP-5 and XDFN 1.5 x 1.5 mm Package
- Active Output Discharge for Fast Output Turn-Off
- These are Pb-Free Devices

Typical Applications

- PDAs, Mobile Phones, GPS, Smartphones
- Wireless Handsets, Wireless LAN, Bluetooth, Zigbee
- Portable Medical Equipment
- Other Battery Powered Applications

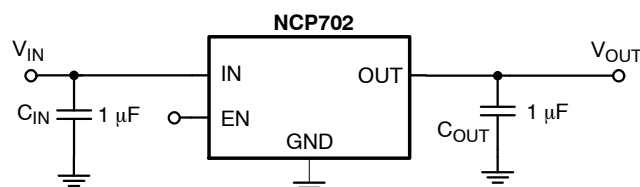
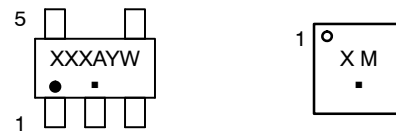


Figure 1. Typical Application Schematic

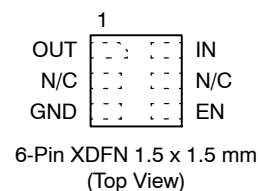
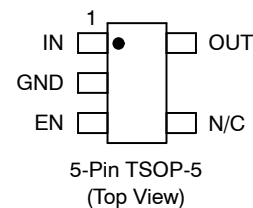


MARKING DIAGRAMS



- X, XXX = Specific Device Code
- M = Date Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 18 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 18.

NCP702

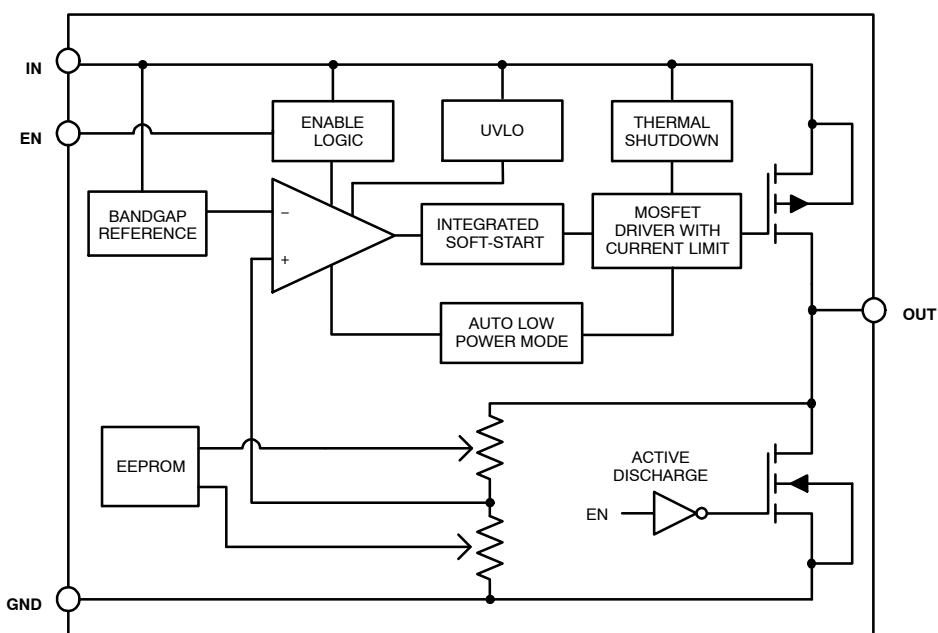


Figure 2. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

| Pin No. XDFN 6 | Pin No. TSOP-5 | Pin Name | Description |
|----------------|----------------|----------|--|
| 1 | 5 | OUT | Regulated output voltage pin. A small 1 μ F ceramic capacitor is needed from this pin to ground to assure stability. |
| 2 | 4 | N/C | Not connected. This pin can be tied to ground to improve thermal dissipation. |
| 3 | 2 | GND | Power supply ground. |
| 4 | 3 | EN | Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode. |
| 5 | | N/C | Not connected. This pin can be tied to ground to improve thermal dissipation. |
| 6 | 1 | IN | Input pin. It is recommended to connect a 1 μ F ceramic capacitor close to the device pin. |

Table 2. ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|--------------|----------------------------|--------------|
| Input Voltage (Note 1) | V_{IN} | -0.3 V to 6 V | V |
| Output Voltage | V_{OUT} | -0.3 V to $V_{IN} + 0.3$ V | V |
| Enable Input | V_{EN} | -0.3 V to $V_{IN} + 0.3$ V | V |
| Output Short Circuit Duration | t_{SC} | Indefinite | s |
| Maximum Junction Temperature | $T_{J(MAX)}$ | 150 | $^{\circ}$ C |
| Storage Temperature | T_{STG} | -55 to 150 | $^{\circ}$ C |
| ESD Capability, Human Body Model (Note 2) | ESD_{HBM} | 2000 | V |
| ESD Capability, Machine Model (Note 2) | ESD_{MM} | 200 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
 ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
 ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)
 Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

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Table 3. THERMAL CHARACTERISTICS (Note 3)

| Rating | Symbol | Value | Unit |
|---|---------------|-------|------|
| Thermal Characteristics, TSOP-5, Thermal Resistance, Junction-to-Air Thermal Characterization Parameter, Junction-to-Lead (Pin 2) | θ_{JA} | 224 | °C/W |
| | ψ_{JA} | 115 | |
| Thermal Characteristics, XDFN6 1.5 x 1.5 mm Thermal Resistance, Junction-to-Air Thermal Characterization Parameter, Junction-to-Board | θ_{JA} | 149 | °C/W |
| | ψ_{JB} | 81 | |

3. Single component mounted on 1 oz, FR4 PCB with 645 mm² Cu area.

Table 4. ELECTRICAL CHARACTERISTICS

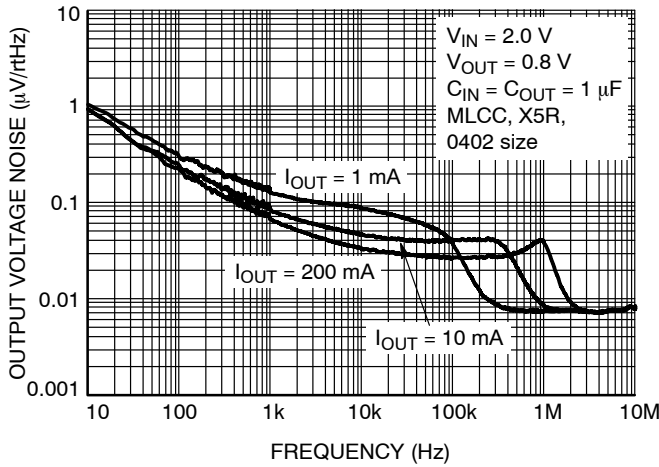
–40 °C ≤ T_J ≤ 125 °C; V_{IN} = V_{OUT(NOM)} + 0.3 V or 2.0 V, whichever is greater; V_{EN} = 0.9 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 μF.
Typical values are at T_J = +25 °C. Min/Max values are specified for T_J = –40 °C and T_J = 125 °C respectively. (Note 4)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---------------------------------------|------|-------------|-----|-------------------|
| Operating Input Voltage | | V _{IN} | 2.0 | | 5.5 | V |
| Undervoltage lock-out | V _{IN} rising | UVLO | 1.2 | 1.6 | 1.9 | V |
| Output Voltage Accuracy | V _{OUT} + 0.3 V ≤ V _{IN} ≤ 5.5 V, I _{OUT} = 0 – 200 mA | V _{OUT} | –2 | | +2 | % |
| Line Regulation | V _{OUT} + 0.3 V ≤ V _{IN} ≤ 4.5 V, I _{OUT} = 10 mA | Reg _{LINE} | | 290 | | μV/V |
| | V _{OUT} + 0.3 V ≤ V _{IN} ≤ 5.5 V, I _{OUT} = 10 mA | Reg _{LINE} | | 440 | | μV/V |
| Load Regulation | I _{OUT} = 0 mA to 200 mA | Reg _{LOAD} | | 13 | | μV/mA |
| Dropout voltage (Note 5) | I _{OUT} = 200 mA, V _{OUT(nom)} = 2.5 V | V _{DO} | | 140 | 200 | mV |
| Output Current Limit | V _{OUT} = 90% V _{OUT(nom)} | I _{CL} | 220 | 385 | 550 | mA |
| Quiescent current | I _{OUT} = 0 mA | I _Q | | 10 | 16 | μA |
| Ground current | I _{OUT} = 2 mA | I _{GND} | | 60 | | μA |
| | I _{OUT} = 200 mA | I _{GND} | | 160 | | μA |
| Shutdown current (Note 6) | V _{EN} ≤ 0.4 V | I _{DIS} | | 0.005 | | μA |
| | V _{EN} ≤ 0.4 V, V _{IN} = 4.5 V | I _{DIS} | | 0.01 | 1 | μA |
| EN Pin Threshold Voltage | V _{EN} Voltage increasing | V _{EN_HI} | 0.9 | | 0.4 | V |
| | V _{EN} Voltage decreasing | V _{EN_LO} | | | | |
| EN Pin Input Current | V _{EN} = V _{IN} = 5.5 V | I _{EN} | | 110 | 500 | nA |
| Turn-On Time (Note 7) | C _{OUT} = 1.0 μF, I _{OUT} = 1 mA | t _{ON} | | 300 | | μs |
| Output Voltage Overshoot on Start-up (Note 8) | V _{EN} = 0 V to 0.9 V, 0 ≤ I _{OUT} ≤ 200 mA | ΔV _{OUT} | | | 2 | % |
| Load Transient | I _{OUT} = 1 mA to 200 mA or I _{OUT} = 200 mA to 1 mA in 10 μs, C _{OUT} = 1 μF | ΔV _{OUT} | | –30/+3 0 | | mV |
| Power Supply Rejection Ratio | V _{IN} = 3 V, V _{OUT} = 2.5 V I _{OUT} = 150 mA | f = 100 Hz f = 1 kHz f = 10 kHz | PSRR | 70 | | dB |
| | | | | 68 | | |
| | | | | 53 | | |
| Output Noise Voltage | V _{OUT} = 2.5 V, V _{IN} = 3 V, I _{OUT} = 200 mA f = 100 Hz to 100 kHz | V _N | | 11 | | μV _{rms} |
| Active Discharge Resistance | V _{EN} < 0.4 V | R _{DIS} | | 1 | | kΩ |
| Thermal Shutdown Temperature | Temperature increasing from T _J = +25 °C | T _{SD} | | 160 | | °C |
| Thermal Shutdown Hysteresis | Temperature falling from T _{SD} | T _{SDH} | – | 20 | – | °C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

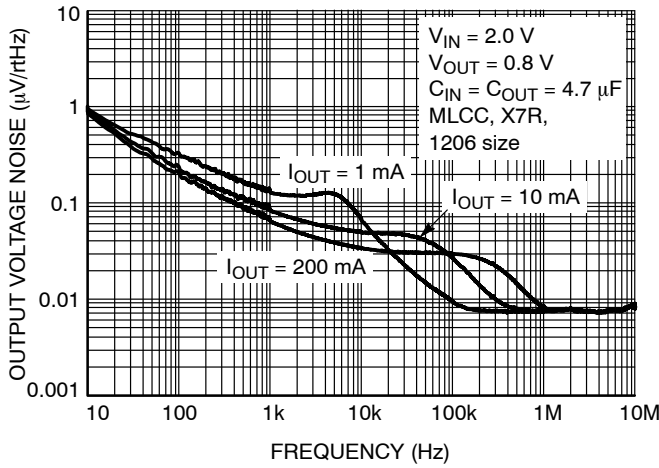
- Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_J = T_A = 25 °C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
- Characterized when V_{OUT} falls 100 mV below the regulated voltage at V_{IN} = V_{OUT(NOM)} + 0.3 V.
- Shutdown Current is the current flowing into the IN pin when the device is in the disable state.
- Turn-On time is measured from the assertion of EN pin to the point when the output voltage reaches 0.98 V_{OUT(NOM)}
- Guaranteed by design.

TYPICAL CHARACTERISTICS



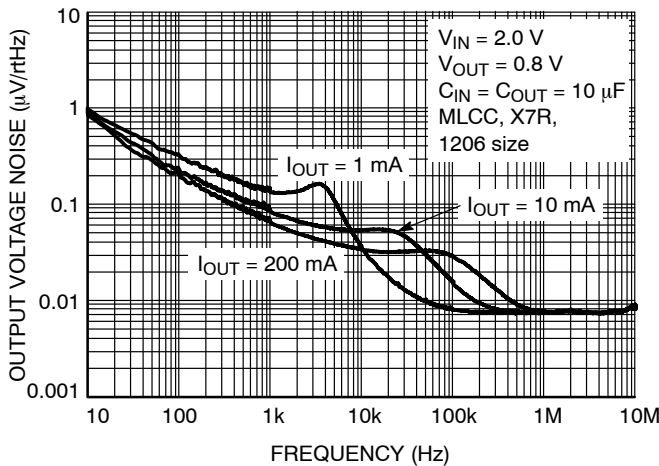
| I _{OUT} | RMS Output Noise | |
|------------------|------------------|------------------|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 21.74 | 21.17 |
| 10 mA | 14.62 | 14.07 |
| 200 mA | 10.74 | 10.02 |

Figure 3. Output Voltage Noise Spectral Density for V_{OUT} = 0.8 V, C_{OUT} = 1 μF



| I _{OUT} | RMS Output Noise | |
|------------------|------------------|------------------|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 14.16 | 13.43 |
| 10 mA | 14.20 | 13.70 |
| 200 mA | 10.99 | 10.48 |

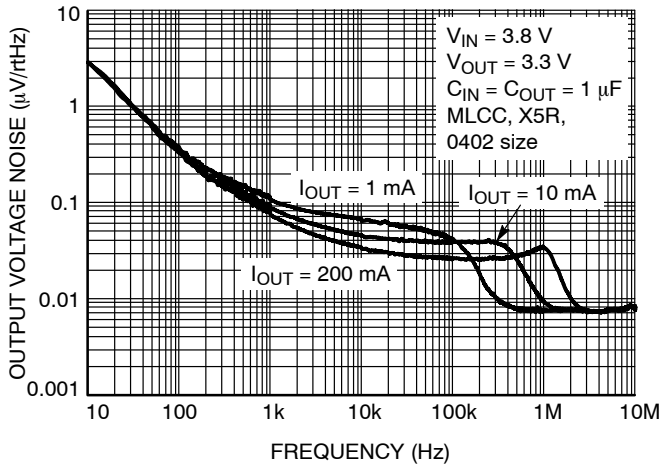
Figure 4. Output Voltage Noise Spectral Density for V_{OUT} = 0.8 V, C_{OUT} = 4.7 μF



| I _{OUT} | RMS Output Noise | |
|------------------|------------------|------------------|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 12.94 | 12.11 |
| 10 mA | 12.78 | 12.25 |
| 200 mA | 11.33 | 10.83 |

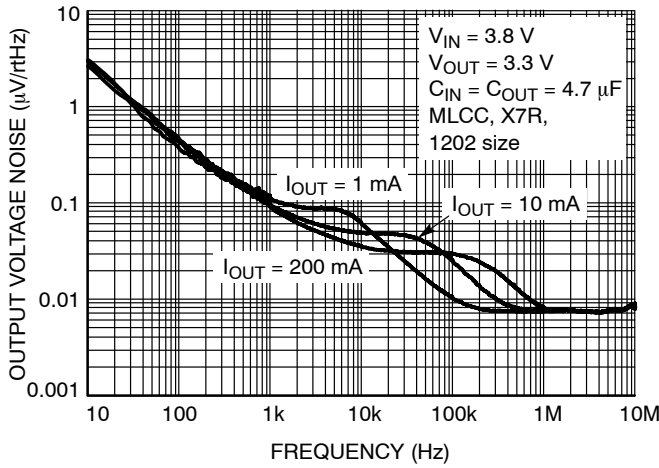
Figure 5. Output Voltage Noise Spectral Density for V_{OUT} = 0.8 V, C_{OUT} = 10 μF

TYPICAL CHARACTERISTICS



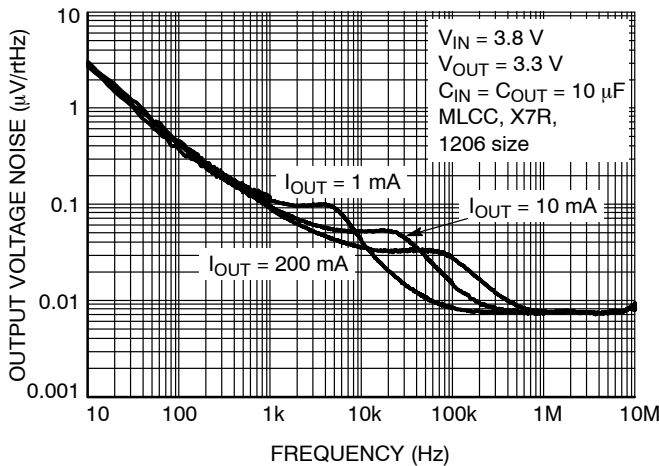
| I _{OUT} | RMS Output Noise | |
|------------------|------------------|------------------|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 20.28 | 17.87 |
| 10 mA | 16.73 | 13.90 |
| 200 mA | 13.70 | 10.21 |

Figure 6. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, C_{OUT} = 1 μF



| I _{OUT} | RMS Output Noise | |
|------------------|------------------|------------------|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 15.76 | 11.82 |
| 10 mA | 17.09 | 13.88 |
| 200 mA | 14.51 | 11.47 |

Figure 7. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, C_{OUT} = 4.7 μF



| I _{OUT} | RMS Output Noise | |
|------------------|------------------|------------------|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 14.87 | 10.57 |
| 10 mA | 16.00 | 12.65 |
| 200 mA | 14.89 | 11.84 |

Figure 8. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, C_{OUT} = 10 μF

TYPICAL CHARACTERISTICS

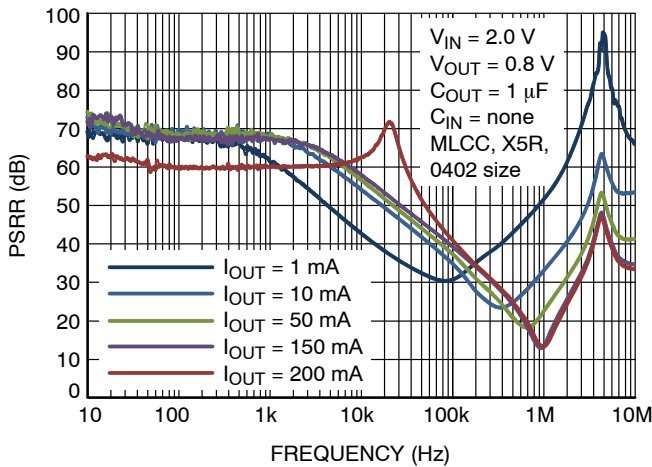


Figure 9. Power Supply Rejection Ratio, $V_{OUT} = 0.8\text{ V}$, $C_{OUT} = 1\ \mu\text{F}$

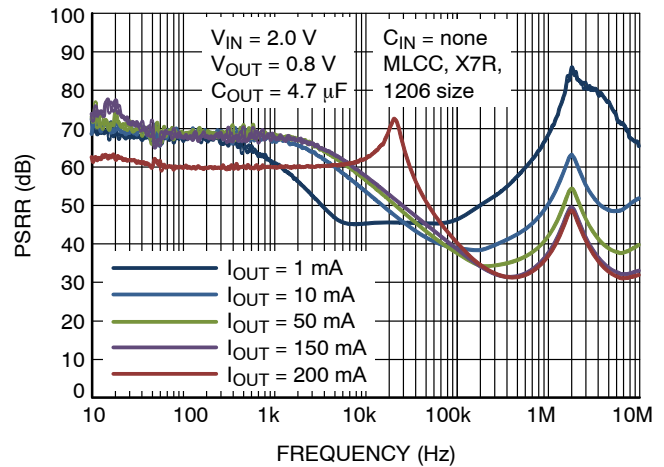


Figure 10. Power Supply Rejection Ratio, $V_{OUT} = 0.8\text{ V}$, $C_{OUT} = 4.7\ \mu\text{F}$

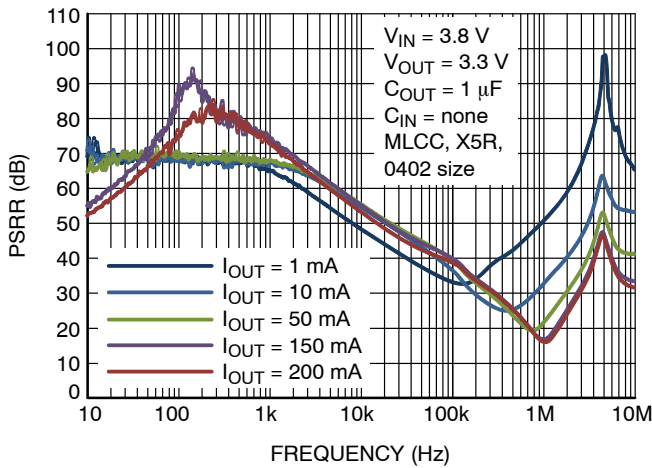


Figure 11. Power Supply Rejection Ratio, $V_{OUT} = 3.3\text{ V}$, $C_{OUT} = 1\ \mu\text{F}$

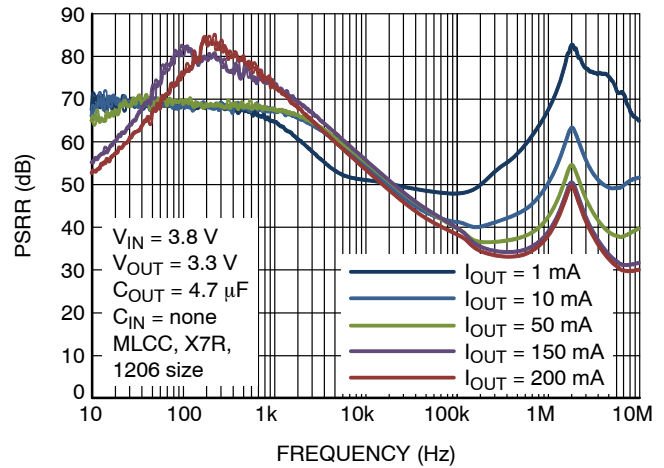


Figure 12. Power Supply Rejection Ratio, $V_{OUT} = 3.3\text{ V}$, $C_{OUT} = 4.7\ \mu\text{F}$

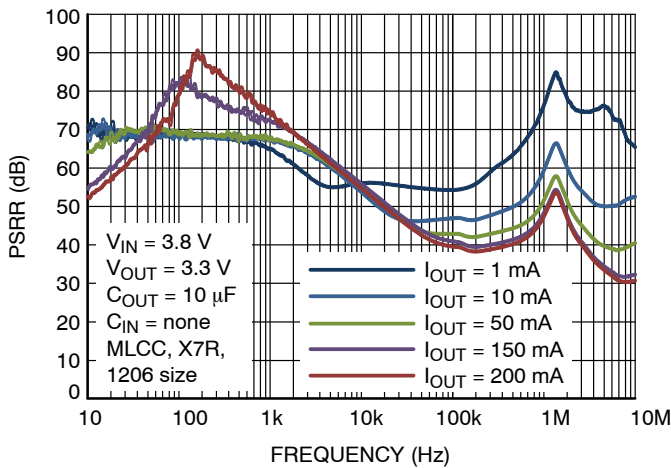


Figure 13. Power Supply Rejection Ratio, $V_{OUT} = 3.3\text{ V}$, $C_{OUT} = 10\ \mu\text{F}$

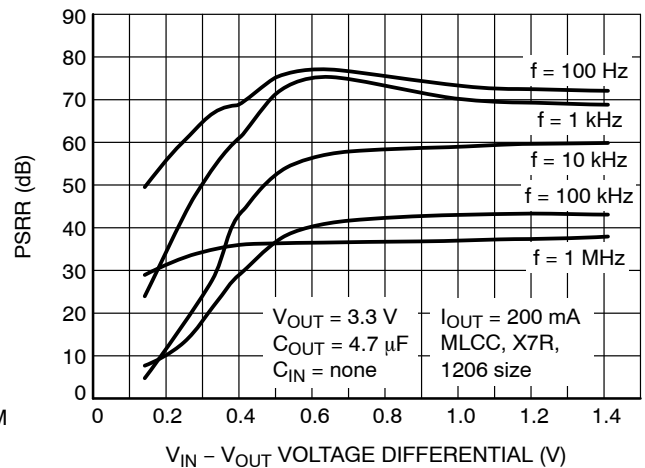


Figure 14. PSRR vs. Voltage Differential, $C_{OUT} = 4.7\ \mu\text{F}$, $I_{OUT} = 200\text{ mA}$

TYPICAL CHARACTERISTICS

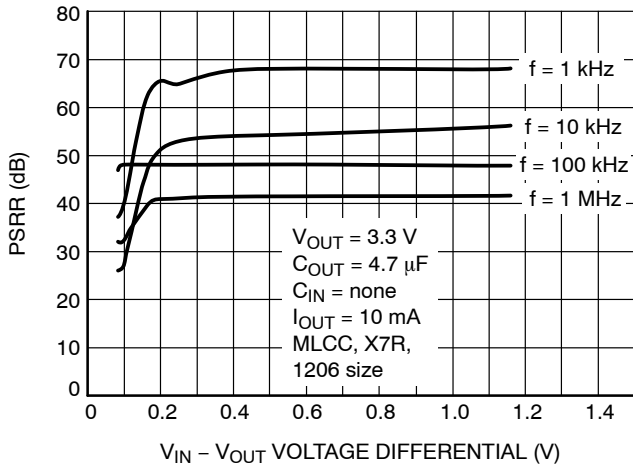


Figure 15. PSRR vs. Voltage Differential, $C_{OUT} = 4.7 \mu F$, $I_{OUT} = 10 \text{ mA}$

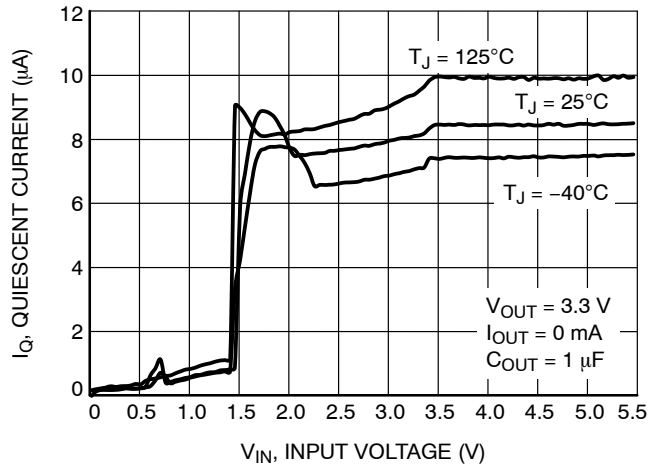


Figure 16. Quiescent Current vs. Input Voltage, $V_{OUT} = 3.3 \text{ V}$

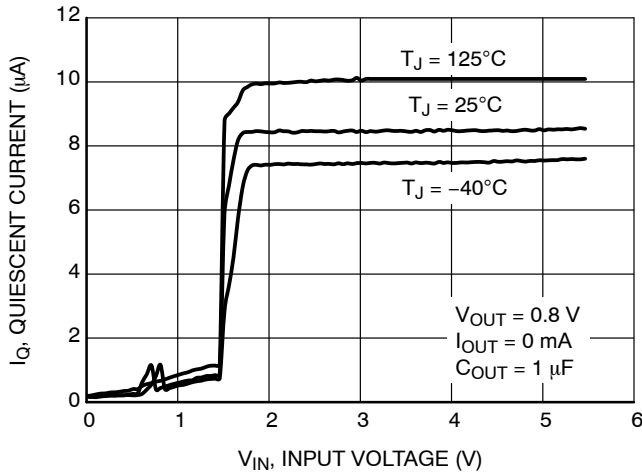


Figure 17. Quiescent Current vs. Input Voltage, $V_{OUT} = 0.8 \text{ V}$

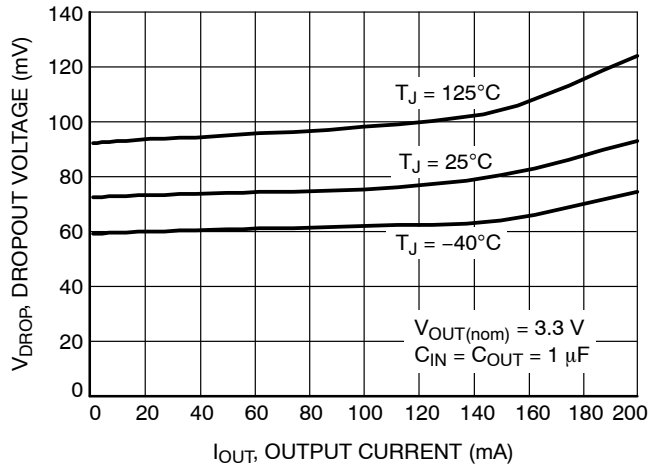


Figure 18. Dropout Voltage vs. Output Current, $V_{OUT} = 3.3 \text{ V}$

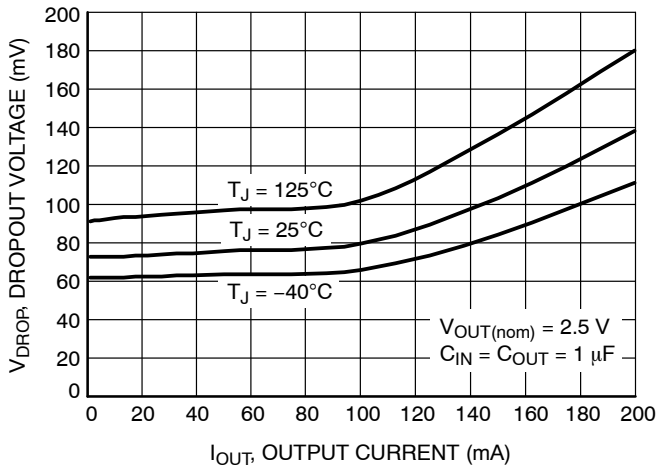


Figure 19. Dropout Voltage vs. Output Current, $V_{OUT} = 2.5 \text{ V}$

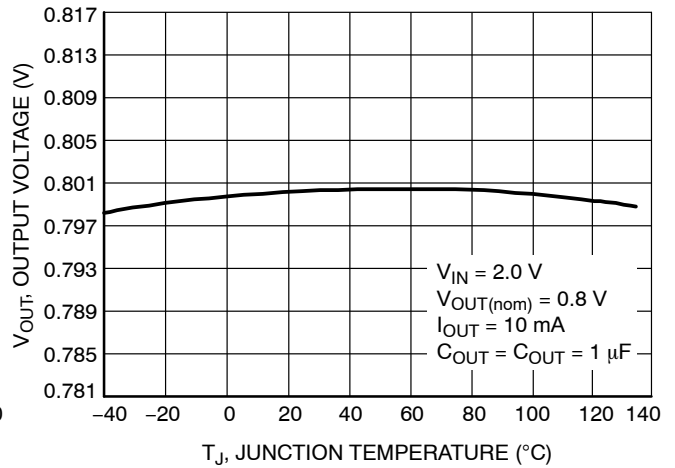


Figure 20. Output Voltage vs. Temperature, $V_{OUT} = 0.8 \text{ V}$

TYPICAL CHARACTERISTICS

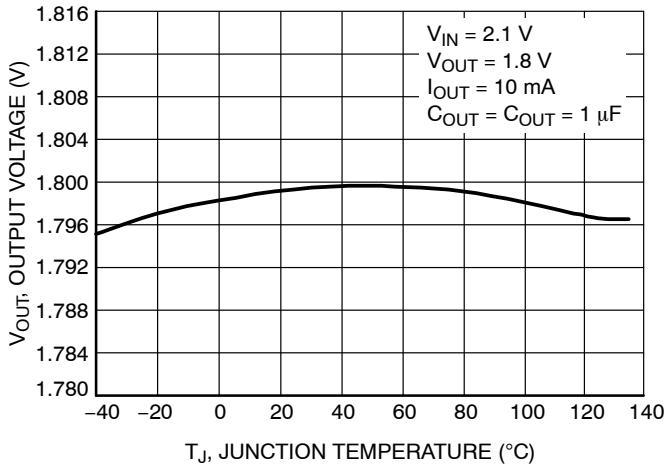


Figure 21. Output Voltage vs. Temperature, $V_{OUT} = 1.8\text{ V}$

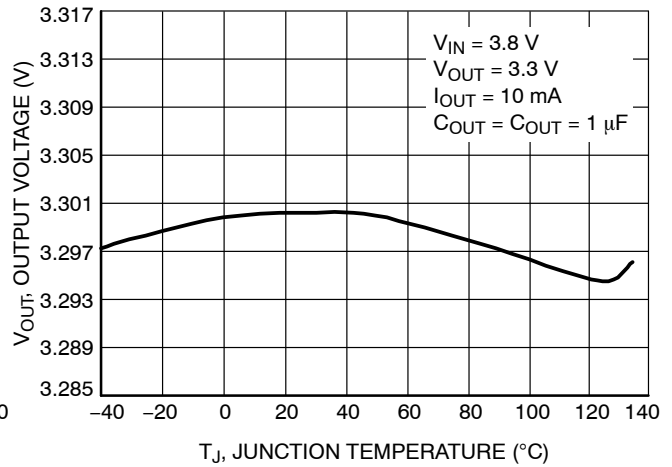


Figure 22. Output Voltage vs. Temperature, $V_{OUT} = 3.3\text{ V}$

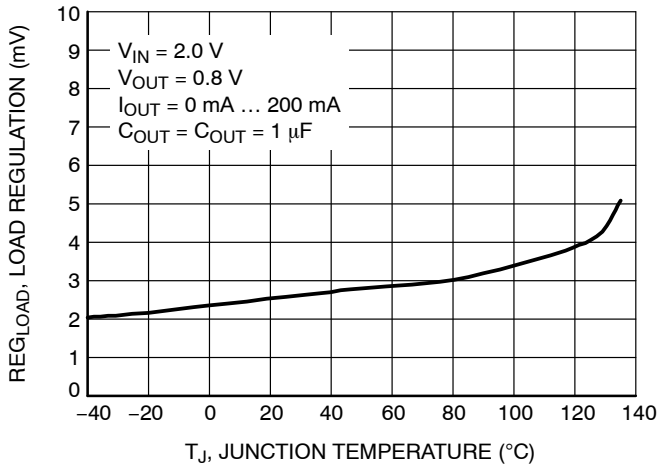


Figure 23. Load Regulation vs. Temperature, $V_{OUT} = 0.8\text{ V}$

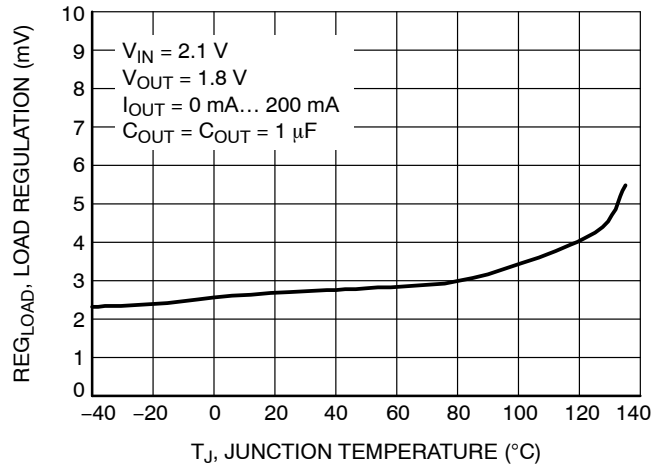


Figure 24. Load Regulation vs. Temperature, $V_{OUT} = 1.8\text{ V}$

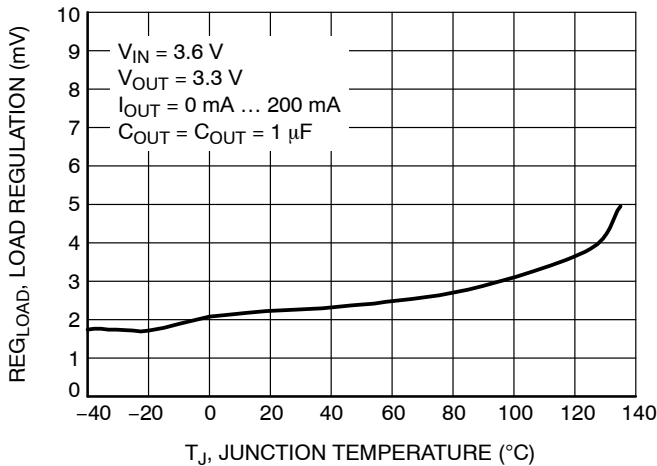


Figure 25. Load Regulation vs. Temperature, $V_{OUT} = 3.3\text{ V}$

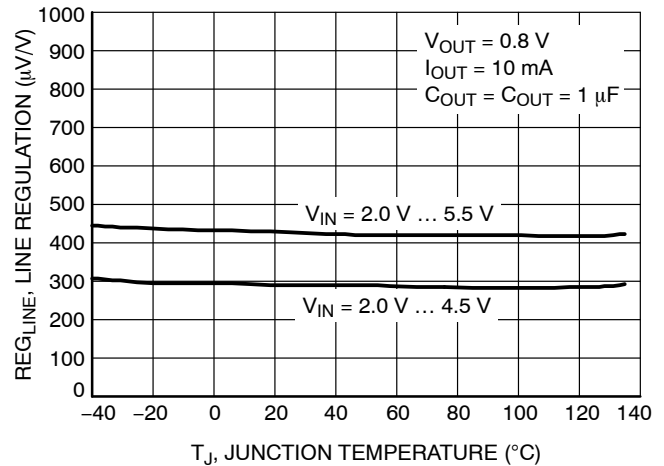


Figure 26. Line Regulation vs. Temperature, $V_{OUT} = 0.8\text{ V}$

TYPICAL CHARACTERISTICS

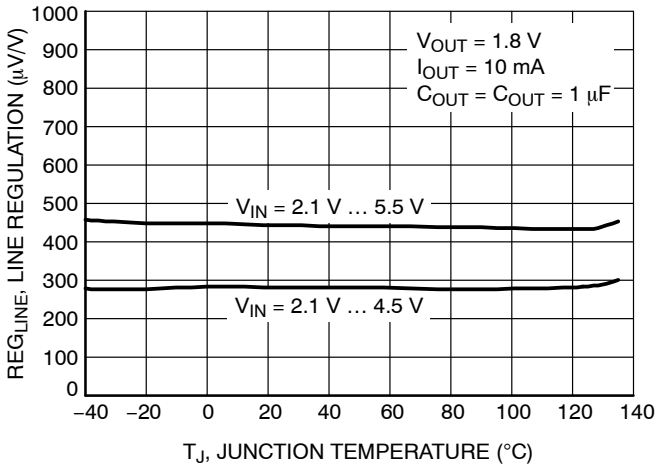


Figure 27. Line Regulation vs. Temperature, $V_{OUT} = 1.8\text{ V}$

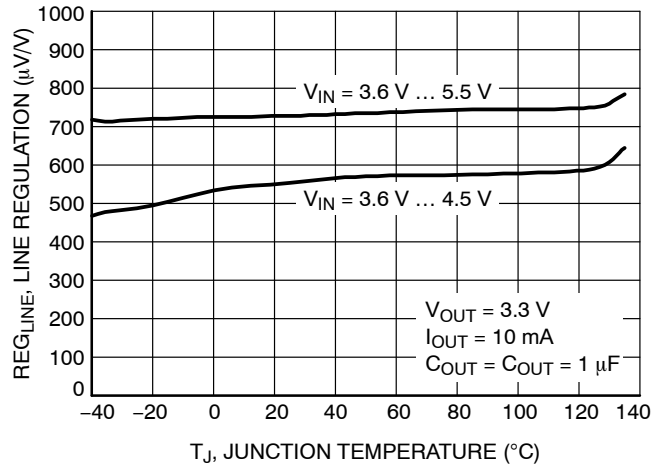


Figure 28. Line Regulation vs. Temperature, $V_{OUT} = 3.3\text{ V}$

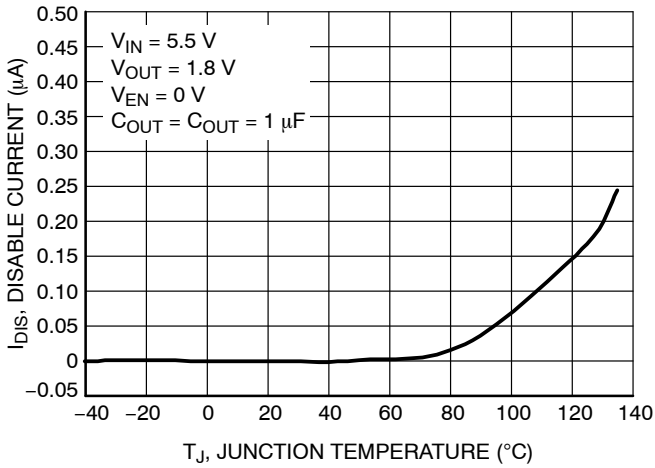


Figure 29. Disable Current vs. Temperature, $V_{OUT} = 1.8\text{ V}$

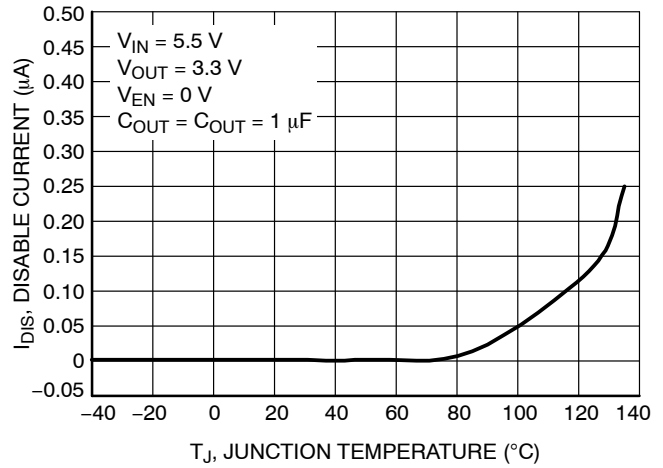


Figure 30. Disable Current vs. Temperature, $V_{OUT} = 3.3\text{ V}$

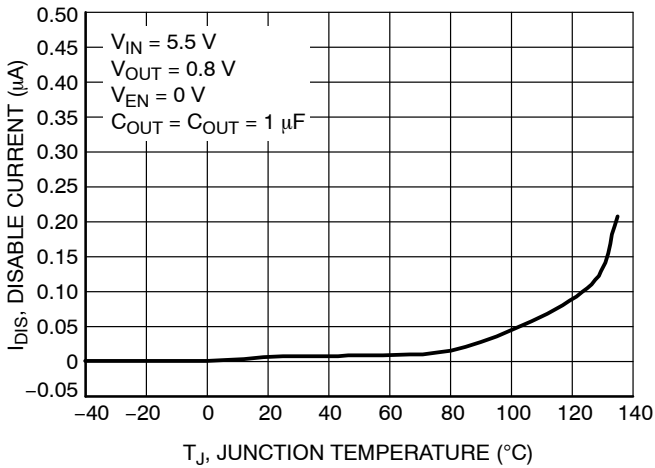


Figure 31. Disable Current vs. Temperature, $V_{OUT} = 0.8\text{ V}$

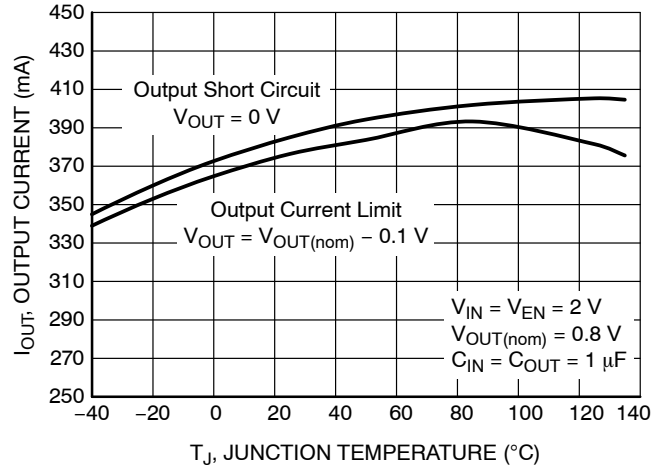


Figure 32. Output Current Limit vs. Temperature, $V_{OUT} = 0.8\text{ V}$

TYPICAL CHARACTERISTICS

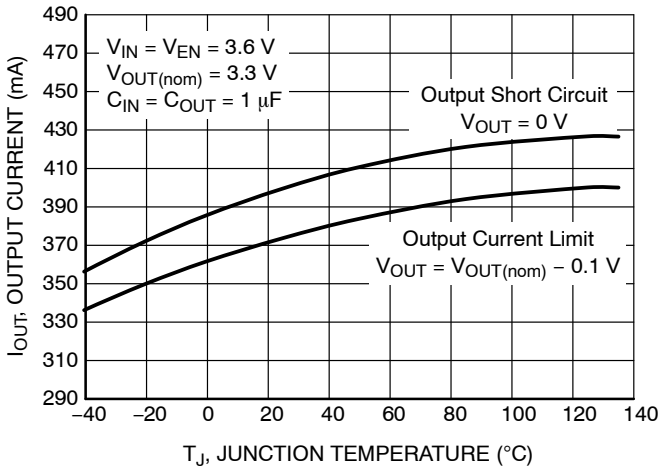


Figure 33. Output Current Limit vs. Temperature, $V_{OUT} = 3.3\text{ V}$

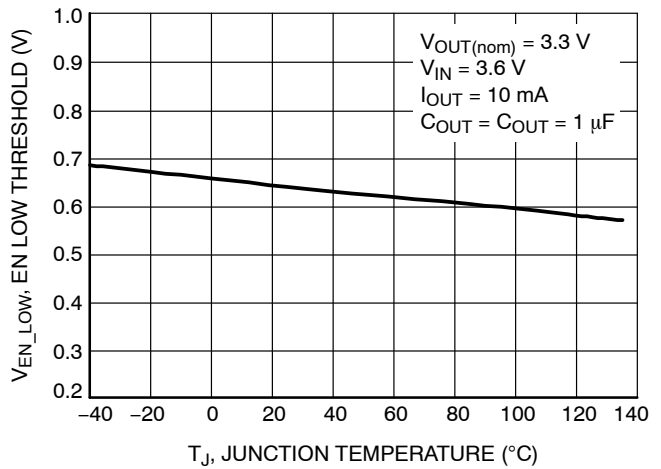


Figure 34. Enable Low Threshold Voltage

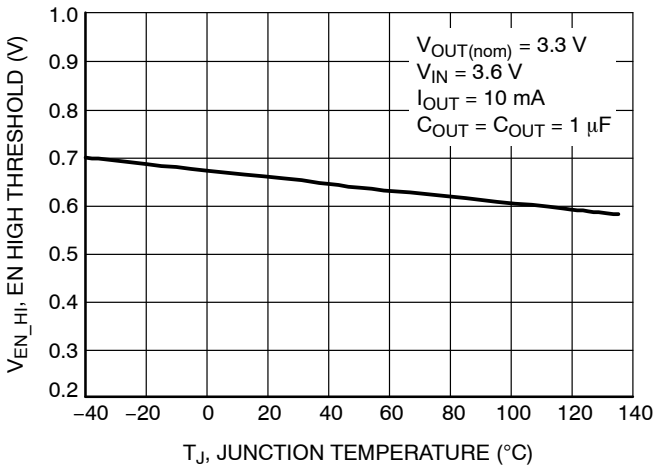


Figure 35. Enable High Threshold Voltage

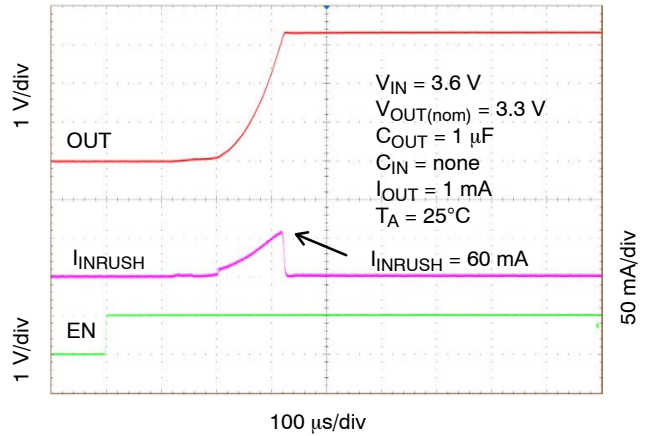


Figure 36. Enable Turn-On Response, $V_{OUT} = 3.3\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$

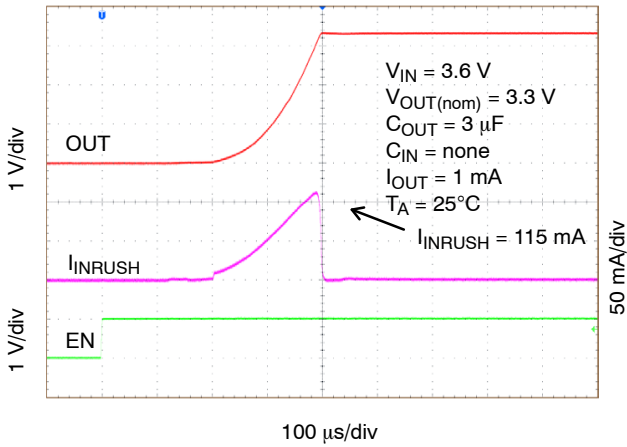


Figure 37. Enable Turn-On Response, $V_{OUT} = 3.3\text{ V}$, $C_{OUT} = 3\text{ }\mu\text{F}$

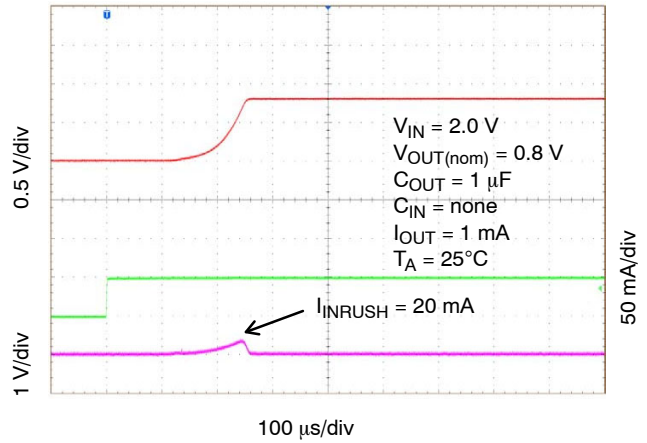


Figure 38. Enable Turn-On Response, $V_{OUT} = 0.8\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$

TYPICAL CHARACTERISTICS

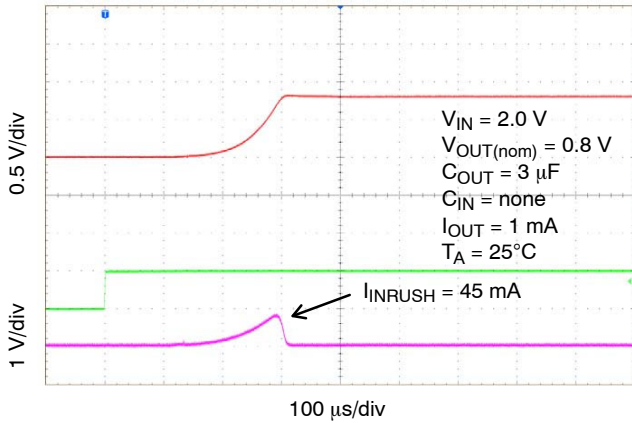


Figure 39. Enable Turn-On Response, $V_{OUT} = 0.8\text{ V}$, $C_{OUT} = 3\ \mu\text{F}$

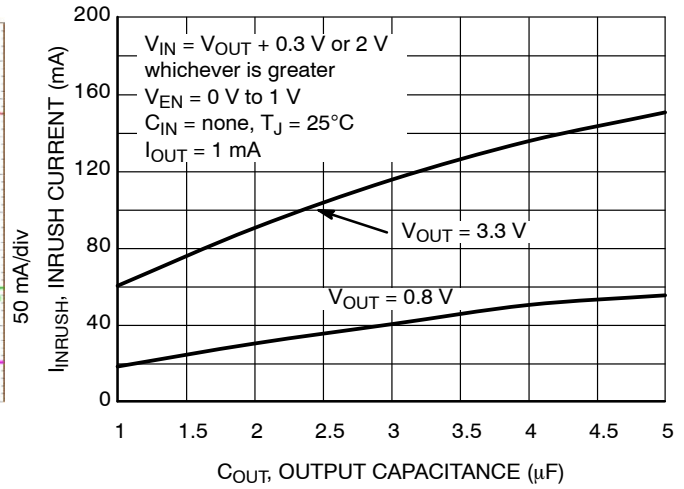


Figure 40. Turn-On Inrush Current vs. Output Capacitance

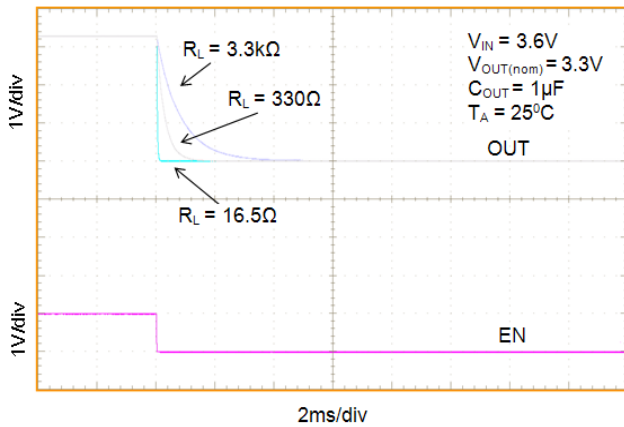


Figure 41. Enable Turn-Off Response, $V_{OUT} = 3.3\text{ V}$, $C_{OUT} = 1\ \mu\text{F}$

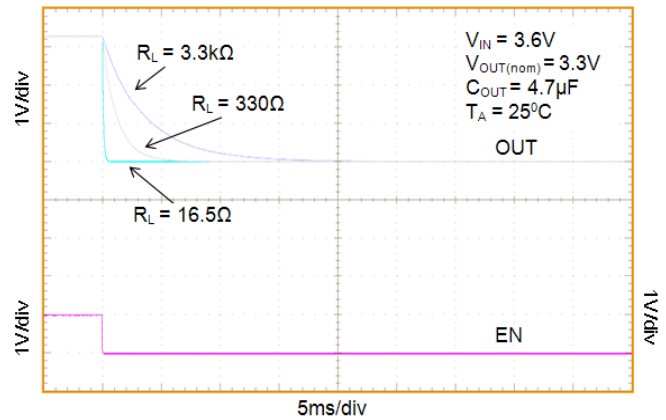


Figure 42. Enable Turn-Off Response, $V_{OUT} = 3.3\text{ V}$, $C_{OUT} = 4.7\ \mu\text{F}$

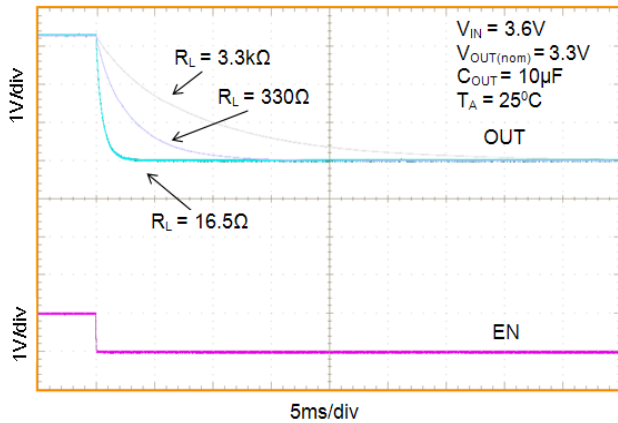


Figure 43. Enable Turn-Off Response, $V_{OUT} = 3.3\text{ V}$, $C_{OUT} = 10\ \mu\text{F}$

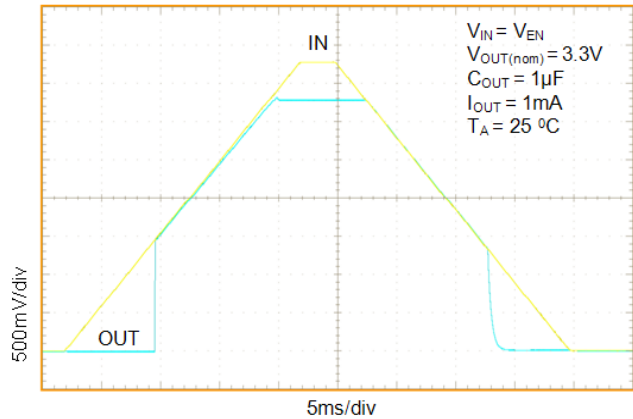


Figure 44. Slow Input Voltage Turn-On/Turn-Off, $V_{OUT} = 3.3\text{ V}$

TYPICAL CHARACTERISTICS

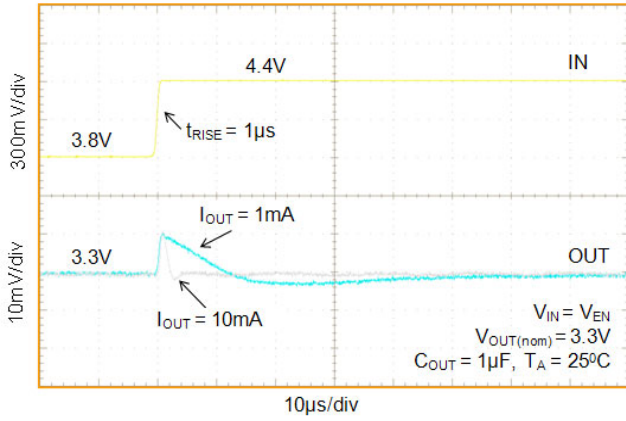


Figure 45. Line Transient Response - Rising Edge, $V_{OUT} = 3.3\text{ V}$

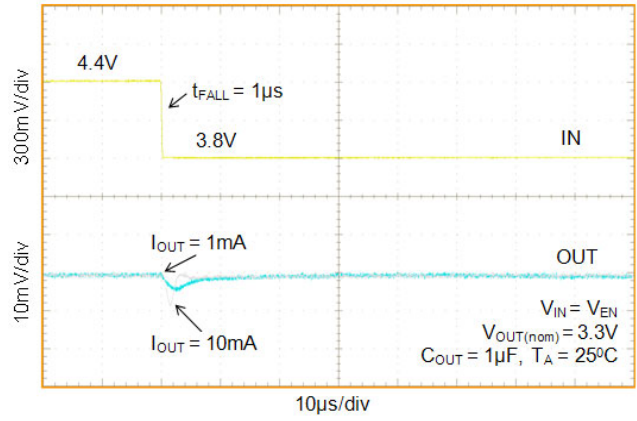


Figure 46. Line Transient Response - Falling Edge, $V_{OUT} = 3.3\text{ V}$

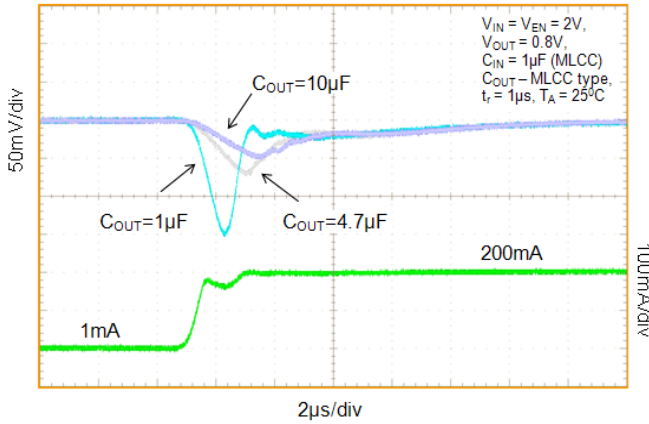


Figure 47. Load Transient Response - Rising Edge, $I_{OUT} = 1\text{ mA} - 200\text{ mA}$, $V_{OUT} = 0.8\text{ V}$

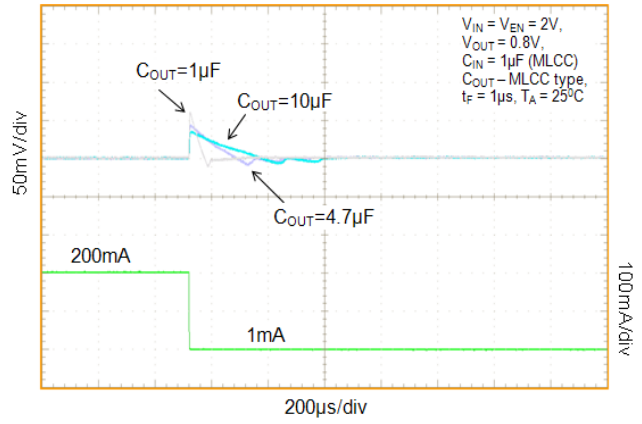


Figure 48. Load Transient Response - Falling Edge, $I_{OUT} = 1\text{ mA} - 200\text{ mA}$, $V_{OUT} = 0.8\text{ V}$

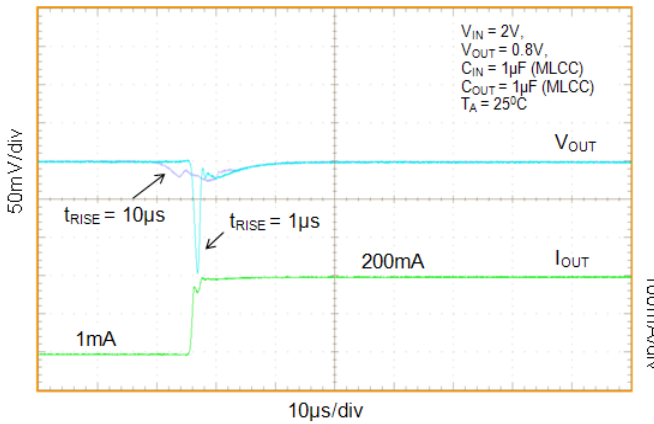


Figure 49. Load Transient Response - Rising Edge, $I_{OUT} = 1\text{ mA} - 200\text{ mA}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

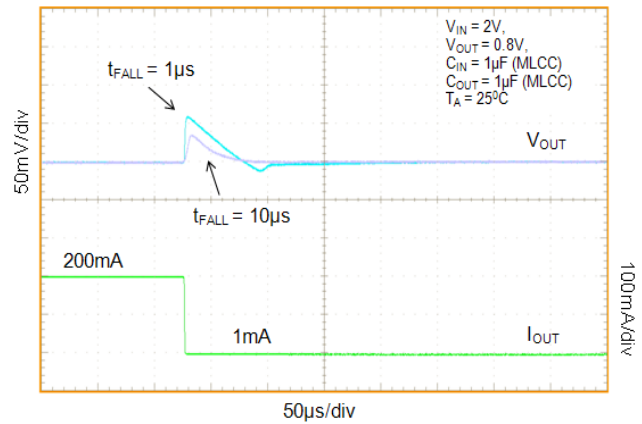


Figure 50. Load Transient Response - Falling Edge, $I_{OUT} = 1\text{ mA} - 200\text{ mA}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

TYPICAL CHARACTERISTICS

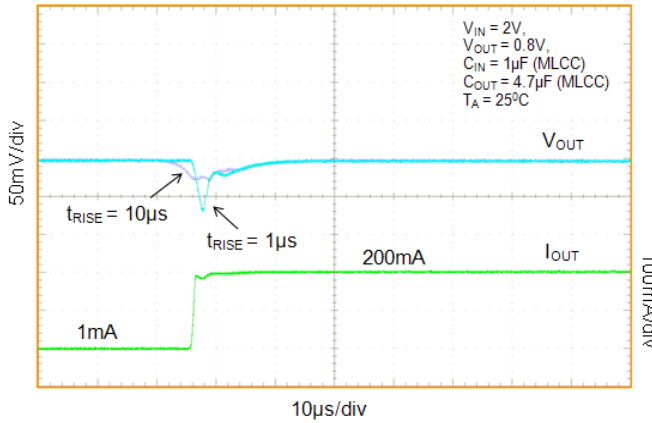


Figure 51. Load Transient Response – Rising Edge, $I_{OUT} = 1\text{ mA} - 200\text{ mA}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$

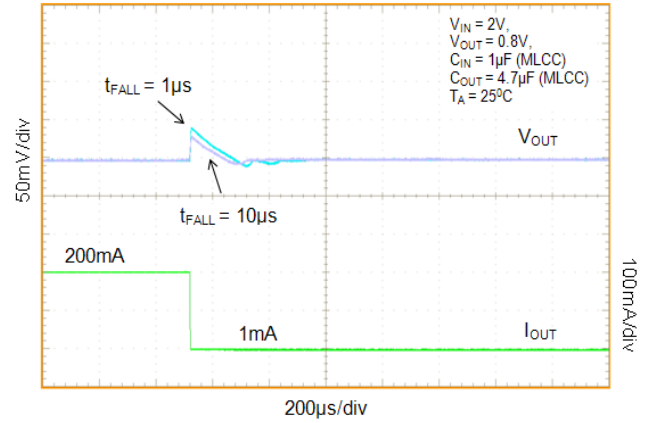


Figure 52. Load Transient Response – Falling Edge, $I_{OUT} = 1\text{ mA} - 200\text{ mA}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$

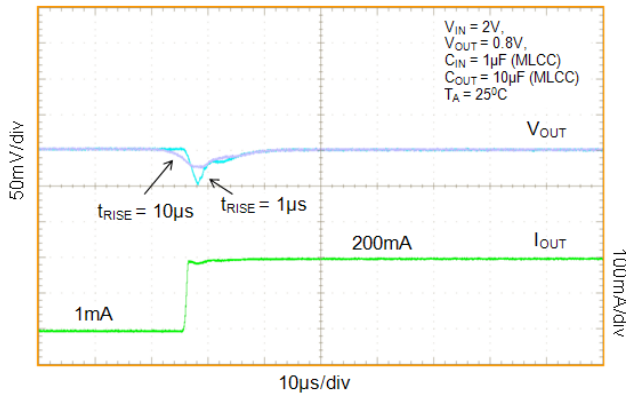


Figure 53. Load Transient Response – Rising Edge, $I_{OUT} = 1\text{ mA} - 200\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$

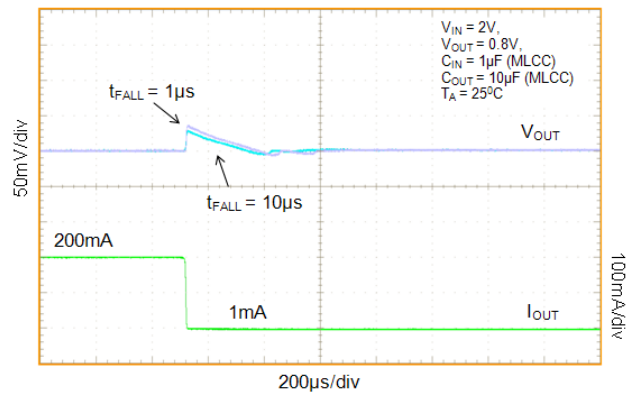


Figure 54. Load Transient Response – Falling Edge, $I_{OUT} = 1\text{ mA} - 200\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$

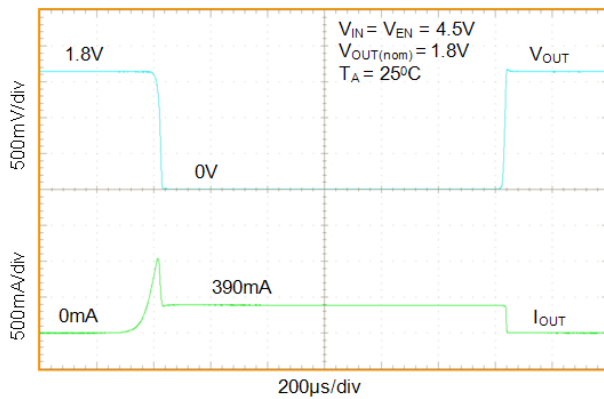


Figure 55. Output Short Circuit Response

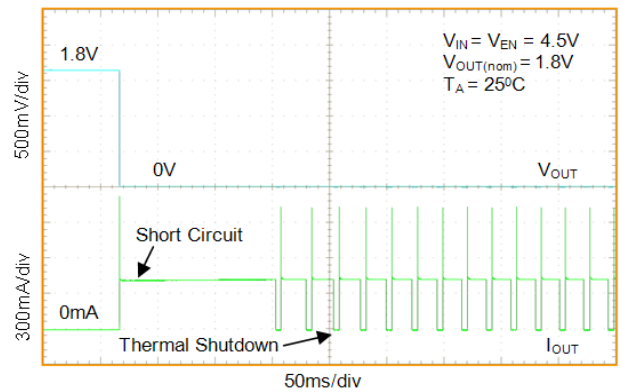


Figure 56. Cycling between Output Short Circuit and Thermal Shutdown

TYPICAL CHARACTERISTICS

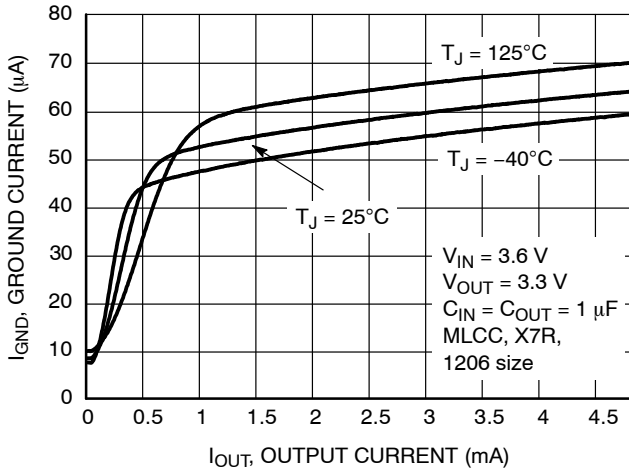


Figure 57. Ground Current vs. Output Current, $I_{OUT} = 0 \text{ mA to } 5 \text{ mA}$

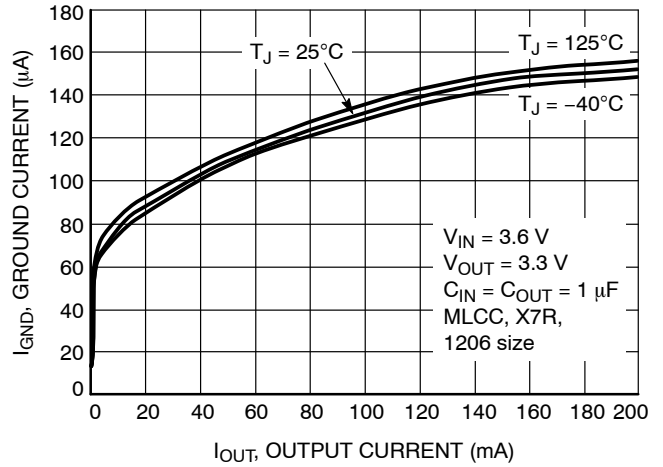


Figure 58. Ground Current vs. Output Current, $I_{OUT} = 0 \text{ mA to } 200 \text{ mA}$

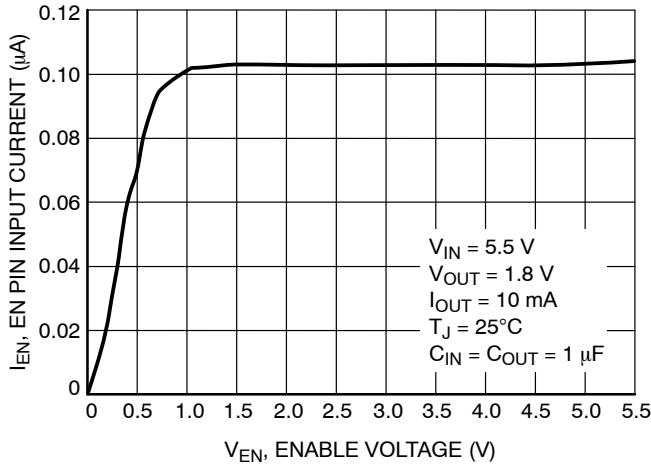


Figure 59. EN Pin Input Current vs. Enable Pin Voltage

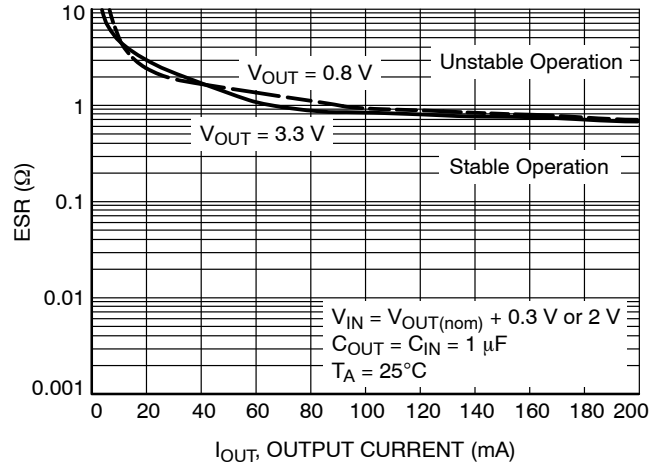


Figure 60. Output Capacitor ESR vs. Output Current

APPLICATIONS INFORMATION

General

The NCP702 is a high performance 200 mA Low Dropout Linear Regulator. This device delivers excellent noise and dynamic performance.

Thanks to its adaptive ground current feature the device consumes only 10 μ A of quiescent current at no-load condition.

The regulator features ultra-low noise of 11 μ V_{RMS}, PSRR of 68 dB at 1 kHz and very good load/line transient performance. Such excellent dynamic parameters and small package size make the device an ideal choice for powering the precision analog and noise sensitive circuitry in portable applications. The LDO achieves this ultra low noise level output without the need for a noise bypass capacitor.

A logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as typ. 10 nA from the IN pin.

The LDO achieves ultra-low output voltage noise without the need for additional noise bypass capacitor.

The device is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design.

Input Capacitor Selection (C_{IN})

It is recommended to connect a minimum of 1 μ F Ceramic X5R or X7R capacitor close to the IN pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage.

There is no requirement for the min./max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input

capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Larger input capacitor may be necessary if fast and large load transients are encountered in the application.

Output Decoupling (C_{OUT})

The NCP702 is designed to be stable with a small 1.0 μ F ceramic capacitor on the output. To assure proper operation it is strongly recommended to use min. 1.0 μ F capacitor with the initial tolerance of $\pm 10\%$, made of X7R or X5R dielectric material types.

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 700 m Ω .

Larger output capacitors could be used to improve the load transient response or high frequency PSRR as shown in typical characteristics. The initial tolerance requirements can be wider than $\pm 10\%$ when using capacitors larger than 1 μ F.

It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature. The tantalum capacitors are generally more costly than ceramic capacitors.

The table on this page lists the capacitors which were used during the IC evaluation.

No-load Operation

The regulator remains stable and regulates the output voltage properly within the $\pm 2\%$ tolerance limits even with no external load applied to the output.

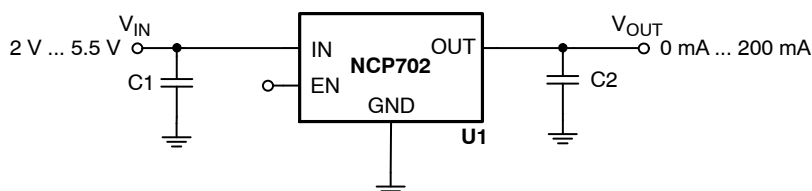


Figure 61. Typical Applications Schematics

LIST OF CAPACITORS USED DURING THE NCP702 EVALUATION:

| Symbol | Manufacturer | Part Number | Description |
|--------|---------------|--------------------|---|
| C1, C2 | Kemet | C0402C105K8PACTU | 1 μ F Ceramic $\pm 10\%$, 10 V, 0402, X5R |
| | TDK | C1005X5R1A105K | - - |
| | Murata | GRM155R61A105KE15D | - - |
| | AVX | 0402ZD105KAT2A | - - |
| | Multicomp | MCCA000571 | 1 μ F Ceramic $\pm 10\%$, 50 V, 1206, X7R |
| | Panason - ECG | ECJ-0EB0J475M | 4.7 μ F Ceramic $\pm 20\%$, 6.3 V, 0402, X5R |

APPLICATIONS INFORMATION

Enable Operation

The NCP702 uses the EN pin to enable/disable its output and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned-off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 1 k Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN} .

If the EN pin voltage >0.9 V the device is guaranteed to be enabled. The NCP702 regulates the output voltage and the active discharge transistor is turned-off.

The EN pin has internal pull-down current source with typ. value of 110 nA which assures that the device is turned-off when the EN pin is not connected. A built-in 2 mV of hysteresis in the EN prevents from periodic on/off oscillations that can occur due to noise.

In the case where the EN function isn't required the EN pin should be tied directly to IN.

Undervoltage Lockout

The internal UVLO circuitry assures that the device becomes disabled when the V_{IN} falls below typ. 1.5 V. When the V_{IN} voltage ramps-up the NCP702 becomes enabled, if V_{IN} rises above typ. 1.6 V. The 100 mV hysteresis prevents on/off oscillations that can occur due to noise on V_{IN} line.

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases where the extended reverse current condition is anticipated the device may require additional external protection.

Output Current Limit

Output Current is internally limited within the IC to a typical 380 mA. The NCP702 will source this amount of current measured with the output voltage 100 mV lower than

the nominal V_{OUT} . If the Output Voltage is directly shorted to ground ($V_{OUT} = 0$ V), the short circuit protection will limit the output current to 390 mA (typ). The current limit and short circuit protection will work properly up to $V_{IN} = 5.5$ V at $T_A = 25$ °C. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold ($T_{SD} - 160$ °C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold ($T_{SDU} - 140$ °C typical). Once the IC temperature falls below the 140 °C the LDO is enabled again. The thermal shutdown feature provides protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCP702 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125 °C.

The maximum power dissipation the NCP702 can handle is given by:

$$P_{D(MAX)} = \frac{[125 - T_A]}{\theta_{JA}} \quad (\text{eq. 1})$$

The power dissipated by the NCP702 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}(I_{GND@I_{OUT}}) + I_{OUT}(V_{IN} - V_{OUT}) \quad (\text{eq. 2})$$

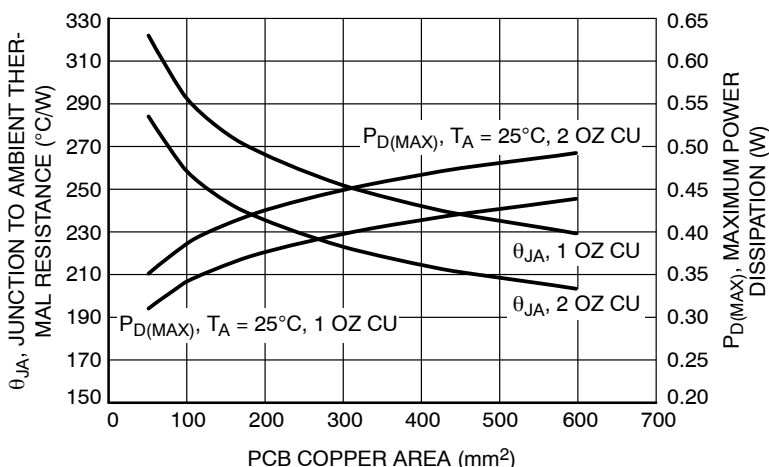


Figure 62. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area (TSOP5)

NCP702

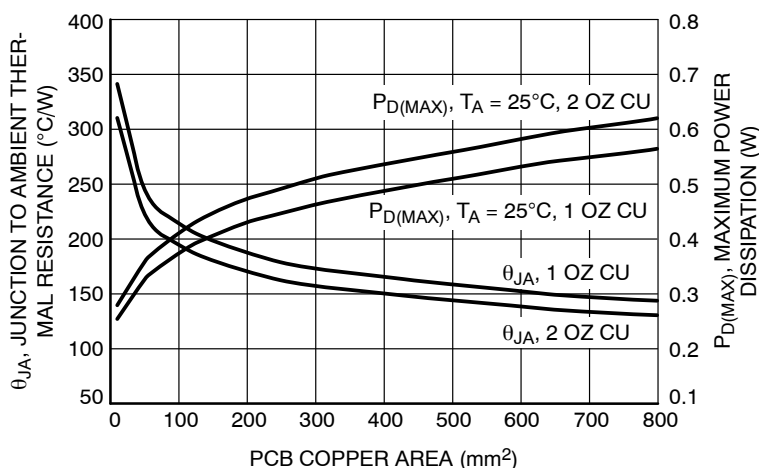


Figure 63. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area (XDFN6)

Load Regulation

The NCP702 features very good load regulation of maximum 2.6 mV in the 0 mA to 200 mA range. In order to achieve this very good load regulation a special attention to PCB design is necessary. The trace resistance from the OUT pin to the point of load can easily approach 100 m Ω which will cause a 20 mV voltage drop at full load current, deteriorating the excellent load regulation.

Line Regulation

The IC features very good line regulation of 0.44 mV/V measured from $V_{IN} = V_{OUT} + 0.3 \text{ V}$ to 5.5 V. For battery operated applications it may be important that the line regulation from $V_{IN} = V_{OUT} + 0.3 \text{ V}$ up to 4.5 V is only 0.29 mV/V.

Power Supply Rejection Ratio

The NCP702 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Output Noise

The IC is designed for ultra-low noise output voltage. Figures 3 – 8 illustrate the noise performance for different V_{OUT} , I_{OUT} , C_{OUT} . Generally the noise performance in the indicated frequency range improves with increasing output current, although even at $I_{OUT} = 1 \text{ mA}$ the noise levels are below 22 μV_{RMS} .

Turn-On Time

The turn-on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on $V_{OUT(NOM)}$, C_{OUT} , T_A . The turn-on time temperature dependence is shown below:

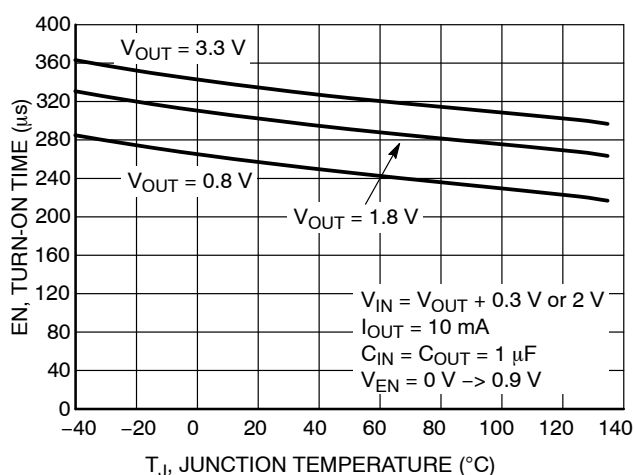


Figure 64. Turn-On Time vs. Temperature

Internal Soft-Start

The Internal Soft-Start circuitry will limit the inrush current during the LDO turn-on phase. Please refer to Figure 43 for typical inrush current values for given output capacitance.

The soft-start function prevents from any output voltage overshoots and assures monotonic ramp-up of the output voltage.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated by the formula given in Equation 2.

NCP702

ORDERING INFORMATION

| Device | Voltage Option | Marking | Package | Shipping † |
|---------------|----------------|---------|--------------------|--------------------|
| NCP702MX30TCG | 3.0 V | 3 | XDFN6 (Pb-Free) | 3000 / Tape & Reel |
| NCP702SN30T1G | 3.0 V | A7R | TSOP5 (Pb-Free) | 3000 / Tape & Reel |
| NCP702SN33T1G | 3.3 V | A7T | | |

DISCONTINUED (Note 9)

| | | | | |
|---------------|-------|-----|--------------------|--------------------|
| NCP702MX18TCG | 1.8 V | P | XDFN6 (Pb-Free) | 3000 / Tape & Reel |
| NCP702MX28TCG | 2.8 V | 2 | XDFN6 (Pb-Free) | 3000 / Tape & Reel |
| NCP702MX33TCG | 3.3 V | 4 | XDFN6 (Pb-Free) | 3000 / Tape & Reel |
| NCP702SN18T1G | 1.8 V | A7J | TSOP5 (Pb-Free) | 3000 / Tape & Reel |
| NCP702SN28T1G | 2.8 V | AD2 | TSOP5 (Pb-Free) | 3000 / Tape & Reel |
| NCP702SN31T1G | 3.1 V | A7P | TSOP5 (Pb-Free) | 3000 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

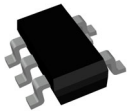
9. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

NCP702

REVISION HISTORY

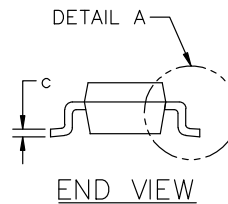
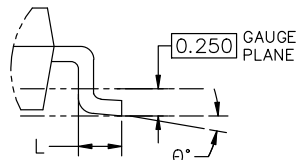
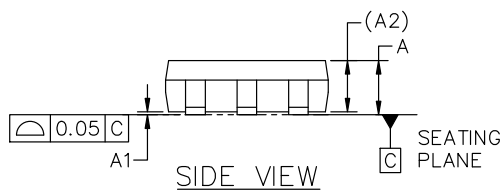
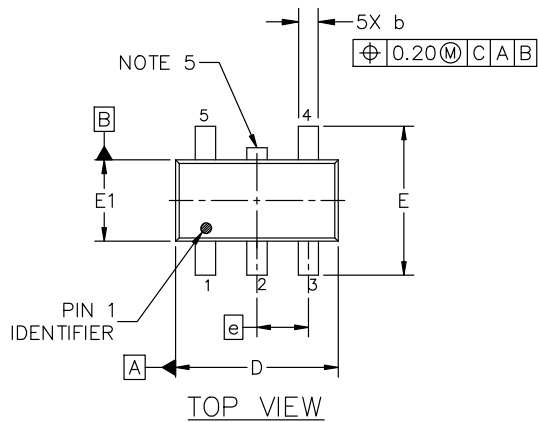
| Revision | Description of Changes | Date |
|----------|---|----------|
| 4 | Rebranded the Data Sheet to onsemi format. NCP702MX18TCG, NCP702MX28TCG, NCP702MX33TCG, NCP702SN18T1G, NCP702SN28T1G, NCP702SN31T1G OPNs Marked as Discontinued. | 2/4/2026 |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



TSOP-5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

DATE 01 APR 2024

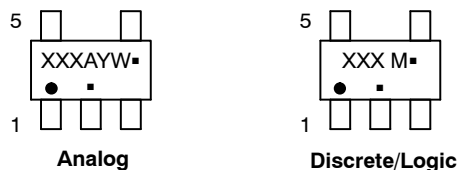


NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 0.900 | 1.000 | 1.100 |
| A1 | 0.010 | 0.055 | 0.100 |
| A2 | 0.950 REF. | | |
| b | 0.250 | 0.375 | 0.500 |
| c | 0.100 | 0.180 | 0.260 |
| D | 2.850 | 3.000 | 3.150 |
| E | 2.500 | 2.750 | 3.000 |
| E1 | 1.350 | 1.500 | 1.650 |
| e | 0.950 BSC | | |
| L | 0.200 | 0.400 | 0.600 |
| θ | 0° | 5° | 10° |

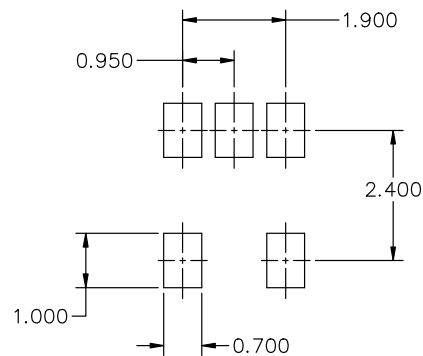
GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package
- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

| | | |
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