

# High Side Gate Driver

## 130 V, 2.0 A / 3.0 A

### NCP51313

NCP51313 is a 130 V high side driver with 2.0 A source and 3.0 A sink drive capability for DC–DC power supplies and inverters. NCP51313 offers best in class propagation delay, low quiescent current and low switching current at high frequencies of operation. This device is tailored for highly efficient power supplies operating at high frequencies. NCP51313 is offered in two versions, NCP51313A/B. NCP51313A has a typical 50 ns propagation delay, while NCP51313B has a typical propagation delay of 20 ns. NCP51313 comes in standard SO8 package.

#### Features

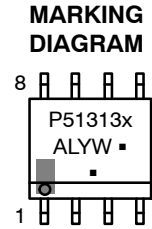
- High Voltage Range: Up to 130 V
- NCP51313A: Typical 50 ns Propagation Delay
- NCP51313B: Typical 20 ns Propagation Delay
- Very Low Quiescent and Operating Currents
- Typ 11 ns Rise / 10 ns Fall Time under 1 nF Load
- 2.0 A Source / 3.0 A Sink Currents
- Under–Voltage Lockout for  $V_{CC}$  and  $V_B$
- 3.3 V and 5 V Input Logic Compatible
- High  $dv/dt$  Immunity up to 50 V/ns
- High Negative Transient Immunity on Bridge Pin
- These are Pb–Free Devices

#### Applications

- DC–DC Converters
- Class–D Audio Amplifiers
- Motor Controls



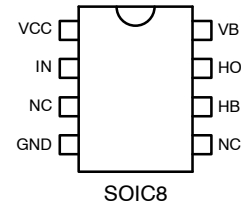
**SOIC–8 NB**  
**CASE 751–07**



P51313 = Specific Device Code  
 x = A or B  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb–Free Package

(NOTE: Microdot may be in either location)

#### PINOUT INFORMATION



#### ORDERING INFORMATION

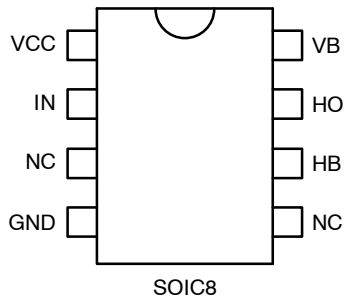
| Device                    | Input Filter | Package         | Shipping†          |
|---------------------------|--------------|-----------------|--------------------|
| NCP51313ADR2G             | Yes          | SOIC8 (Pb–Free) | 2500 / Tape & Reel |
| NCP51313BDR2G (on demand) | No           | SOIC8 (Pb–Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

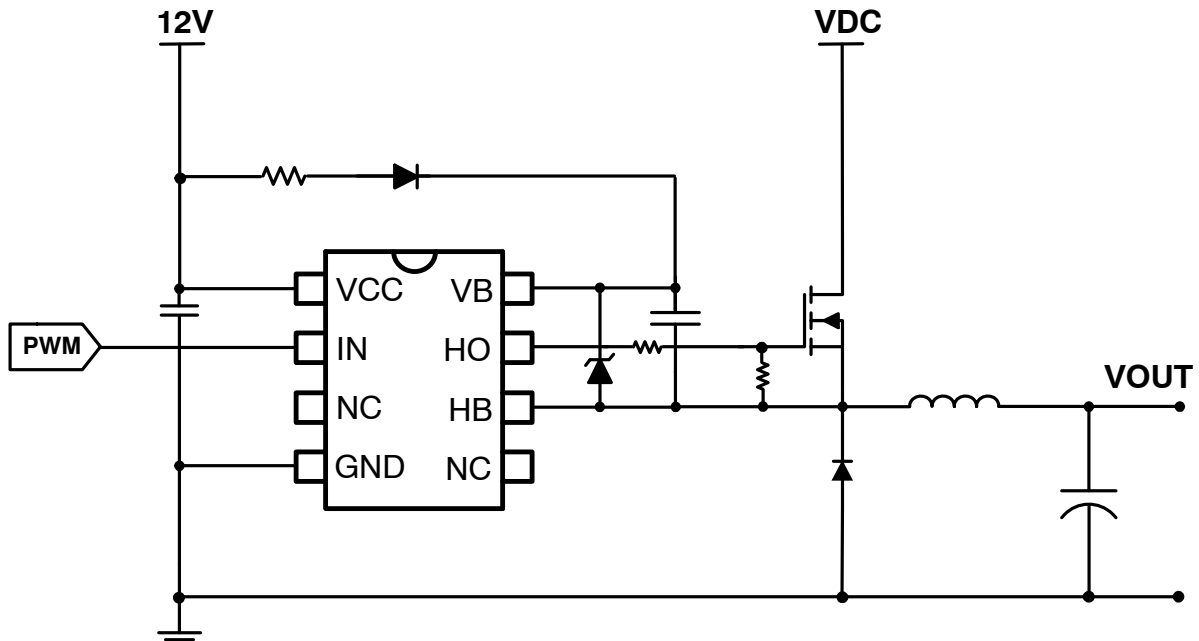
# NCP51313

**Table 1. PIN DESCRIPTION SO8 PACKAGE**

| Pin Out SO8 | Name | Function                 |
|-------------|------|--------------------------|
| 1           | VCC  | Logic supply             |
| 2           | IN   | Input                    |
| 3           | NC   | Not connected            |
| 4           | GND  | Ground reference         |
| 5           | NC   | Not connected            |
| 6           | HB   | High side supply return  |
| 7           | HO   | High side output         |
| 8           | VB   | High side voltage supply |



**Figure 1. Pinout**



**Figure 2. Typical Application Schematic**



**Table 4. RECOMMENDED OPERATING CONDITIONS**

| Symbol                          | Parameter                            | Min             | Max             | Unit |
|---------------------------------|--------------------------------------|-----------------|-----------------|------|
| V <sub>CC</sub>                 | Input Voltage Range                  | 8               | 19              | V    |
| V <sub>B</sub> -V <sub>HB</sub> | High Side Floating Voltage           | 8               | 19              | V    |
| V <sub>HB</sub>                 | High Side Bridge Pin Voltage         | -2              | 110             | V    |
| V <sub>HO</sub>                 | High Side Output Voltage             | V <sub>HB</sub> | V <sub>B</sub>  | V    |
| V <sub>IN</sub>                 | Input Voltage IN Pin                 | -3              | V <sub>CC</sub> | V    |
| T <sub>J</sub>                  | Operating Junction Temperature Range | -40             | 125             | °C   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 5. ELECTRICAL CHARACTERISTICS** (-40°C < T<sub>J</sub> < 125°C, V<sub>CC</sub> = V<sub>B</sub> = 12 V, V<sub>HB</sub> = GND, output is loaded with 1 nF, all voltages are referenced to GND, unless otherwise noted, Typical values are at T<sub>J</sub> = 25°C.)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|--------|-----------|----------------|-----|-----|-----|------|
|--------|-----------|----------------|-----|-----|-----|------|

**SUPPLY SECTION**

|                        |                                               |                                                             |   |     |     |    |
|------------------------|-----------------------------------------------|-------------------------------------------------------------|---|-----|-----|----|
| I <sub>CC1</sub>       | V <sub>CC</sub> Switching Current Consumption | f <sub>SW</sub> = 100 kHz                                   | - | 100 | 150 | μA |
| I <sub>B1</sub>        | V <sub>B</sub> Switching Current Consumption  | f <sub>SW</sub> = 100 kHz                                   | - | 1.6 | 2.3 | mA |
| I <sub>B1_noload</sub> | V <sub>B</sub> Switching Current Consumption  | f <sub>SW</sub> = 100 kHz, C <sub>LOAD</sub> = 0 nF         | - | 0.2 | 0.5 | mA |
| I <sub>CC2</sub>       | V <sub>CC</sub> Quiescent Current Consumption | f <sub>SW</sub> = 0 kHz, V <sub>IN</sub> = 0 V              | - | 100 | 150 | μA |
| I <sub>B2</sub>        | V <sub>B</sub> Quiescent Current Consumption  | f <sub>SW</sub> = 0 kHz, V <sub>IN</sub> = 0 V              | - | 85  | 150 | μA |
| I <sub>HV_LEAK</sub>   | Leakage Current on High Voltage Pins to GND   | V <sub>VB</sub> = V <sub>HO</sub> = V <sub>HB</sub> = 130 V | - | 2   | 5   | μA |

**INPUT SECTION**

|                    |                            |                       |     |     |     |    |
|--------------------|----------------------------|-----------------------|-----|-----|-----|----|
| V <sub>INL</sub>   | Input Falling Threshold    |                       | 0.8 | 1.0 | 1.3 | V  |
| V <sub>INH</sub>   | Input Rising Threshold     |                       | 1.0 | 1.7 | 2.3 | V  |
| V <sub>INHYS</sub> | Input Voltage Hysteresis   |                       | 0.2 | 0.7 | -   | V  |
| R <sub>IN</sub>    | Input Pulldown Resistance  | V <sub>IN</sub> = 5 V | 100 | 175 | 250 | kΩ |
| I <sub>IN+</sub>   | Logic H Input Bias Current | V <sub>IN</sub> = 5 V | -   | 30  | 50  | μA |
| I <sub>IN-</sub>   | Logic L Input Bias Current | V <sub>IN</sub> = 0 V | -   | -   | 2   | μA |

**UVLO SECTION**

|                      |                                                  |                                                                               |     |     |     |    |
|----------------------|--------------------------------------------------|-------------------------------------------------------------------------------|-----|-----|-----|----|
| V <sub>CCCon</sub>   | V <sub>CC</sub> UVLO Start_Up Voltage Threshold  | V <sub>CC</sub> Rising                                                        | 5.8 | 6.4 | 7.0 | V  |
| V <sub>CCoff</sub>   | V <sub>CC</sub> UVLO Shut_Down Voltage Threshold | V <sub>CC</sub> Falling                                                       | 5.3 | 5.9 | 6.5 | V  |
| V <sub>CChyst</sub>  | V <sub>CC</sub> Hysteresis                       |                                                                               | 0.2 | 0.5 | -   | V  |
| V <sub>Bon</sub>     | V <sub>B</sub> UVLO Start_Up Voltage Threshold   | V <sub>Bon</sub> = V <sub>B</sub> - V <sub>HB</sub> , V <sub>B</sub> Rising   | 5.8 | 6.4 | 7.0 | V  |
| V <sub>Boff</sub>    | V <sub>B</sub> UVLO Shut_Down Voltage Threshold  | V <sub>Boff</sub> = V <sub>B</sub> - V <sub>HB</sub> , V <sub>B</sub> Falling | 5.3 | 5.9 | 6.5 | V  |
| V <sub>Bhyst</sub>   | V <sub>B</sub> Hysteresis                        |                                                                               | 0.2 | 0.5 | -   | V  |
| t <sub>startup</sub> | High Side Startup Time                           | Time between V <sub>B</sub> > V <sub>Bon</sub> & 1 <sup>st</sup> HO Pulse     | -   | -   | 10  | μs |

**OUTPUT SECTION**

|                       |                                                   |                                                               |   |      |      |   |
|-----------------------|---------------------------------------------------|---------------------------------------------------------------|---|------|------|---|
| I <sub>HOsource</sub> | Output High Short Circuit Pulsed Current (Note 4) | V <sub>HO</sub> = 0 V, PW = 300 ns                            | - | 2.0  | -    | A |
| I <sub>HOsink</sub>   | Output Low Short Circuit Pulsed Current (Note 4)  | V <sub>HO</sub> = V <sub>B</sub> , PW = 300 ns                | - | 3.0  | -    | A |
| R <sub>OH</sub>       | Output Resistance Source                          | I <sub>HO</sub> = 30 mA                                       | - | 2.0  | 7.0  | Ω |
| R <sub>OL</sub>       | Output Resistance Sink                            | I <sub>HO</sub> = 30 mA                                       | - | 1.0  | 5.0  | Ω |
| V <sub>HOH</sub>      | High Level Output Voltage                         | V <sub>BIAS</sub> - V <sub>HO</sub> @ I <sub>HO</sub> = 20 mA | - | 0.06 | 0.25 | V |
| V <sub>HOL</sub>      | Low Level Output Voltage                          | V <sub>HO</sub> @ I <sub>HO</sub> = 20 mA                     | - | 0.04 | 0.15 | V |

**OUTPUT RISE AND FALL TIME**

|                |                                            |                       |   |    |    |    |
|----------------|--------------------------------------------|-----------------------|---|----|----|----|
| t <sub>r</sub> | Output Voltage Rise Time (from 10% to 90%) | V <sub>IN</sub> = 3 V | - | 11 | 30 | ns |
| t <sub>f</sub> | Output Voltage Fall Time (from 90% to 10%) | V <sub>IN</sub> = 0 V | - | 10 | 25 | ns |

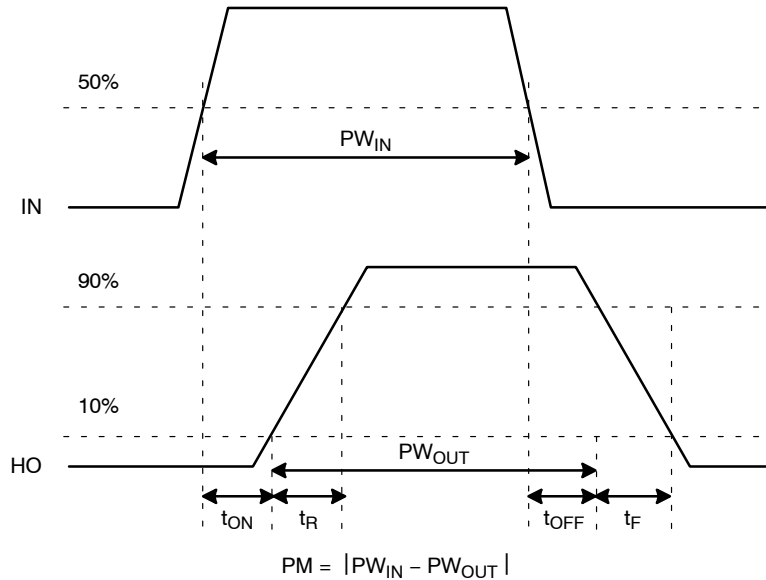
# NCP51313

**Table 5. ELECTRICAL CHARACTERISTICS** ( $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ ,  $V_{CC} = V_B = 12\text{ V}$ ,  $V_{HB} = \text{GND}$ , output is loaded with 1 nF, all voltages are referenced to GND, unless otherwise noted, Typical values are at  $T_J = 25^{\circ}\text{C}$ .)

| Symbol                                       | Parameter                  | Test Condition                                                      | Min | Typ | Max | Unit |
|----------------------------------------------|----------------------------|---------------------------------------------------------------------|-----|-----|-----|------|
| <b>PROPAGATION DELAY NCP51313A</b>           |                            |                                                                     |     |     |     |      |
| $t_{\text{ON}}$                              | Turn On Propagation Delay  | HB = 0 V, 50 V or 130 V, Cload = 0 nF, $V_{\text{IN}} = 3\text{ V}$ | –   | 50  | 100 | ns   |
| $t_{\text{OFF}}$                             | Turn Off Propagation Delay | HB = 0 V, 50 V or 130 V, Cload = 0 nF                               | –   | 50  | 100 | ns   |
| $t_{\text{FLT}}$                             | Minimum Input Filter Time  | $V_{\text{IN}} = 3\text{ V}$                                        | 20  | 30  | –   | ns   |
| <b>PROPAGATION DELAY NCP51313B</b>           |                            |                                                                     |     |     |     |      |
| $t_{\text{ON}}$                              | Turn On Propagation Delay  | HB = 0 V, 50 V or 130 V, Cload = 0 nF, $V_{\text{IN}} = 3\text{ V}$ | –   | 20  | 40  | ns   |
| $t_{\text{OFF}}$                             | Turn Off Propagation Delay | HB = 0 V, 50 V or 130 V, Cload = 0 nF                               | –   | 20  | 40  | ns   |
| <b>OUTPUT PULSE WIDTH MATCHING NCP51313A</b> |                            |                                                                     |     |     |     |      |
| PM                                           | Output Mismatching         | $V_{\text{IN}} = 3\text{ V}$ , 1 $\mu\text{s}$ pulse width          | –   | 0   | 20  | ns   |
| <b>OUTPUT PULSE WIDTH MATCHING NCP51313B</b> |                            |                                                                     |     |     |     |      |
| PM                                           | Output Mismatching         | $V_{\text{IN}} = 3\text{ V}$ , 1 $\mu\text{s}$ pulse width          | –   | 0   | 10  | ns   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Parameter guaranteed by design.



**Figure 4. Propagation Delay, Rise and Fall Times, PM**

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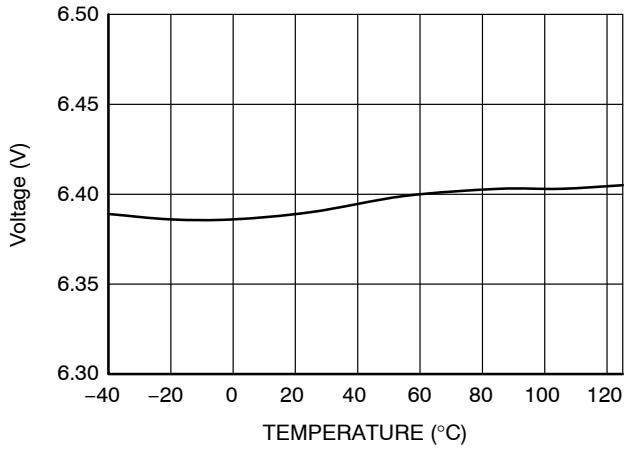


Figure 5. V<sub>CCon</sub> vs. Temperature

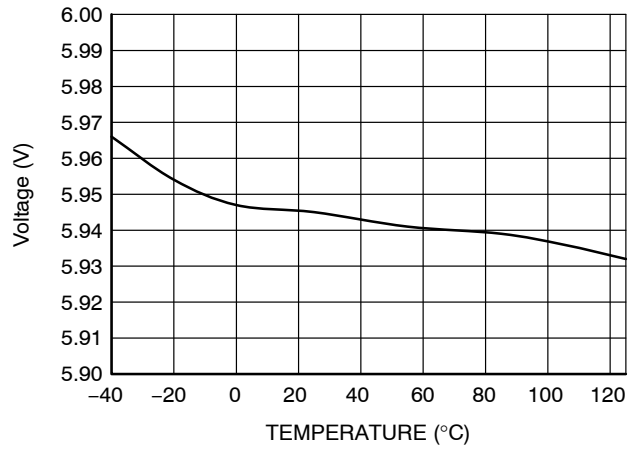


Figure 6. V<sub>CCoff</sub> vs. Temperature

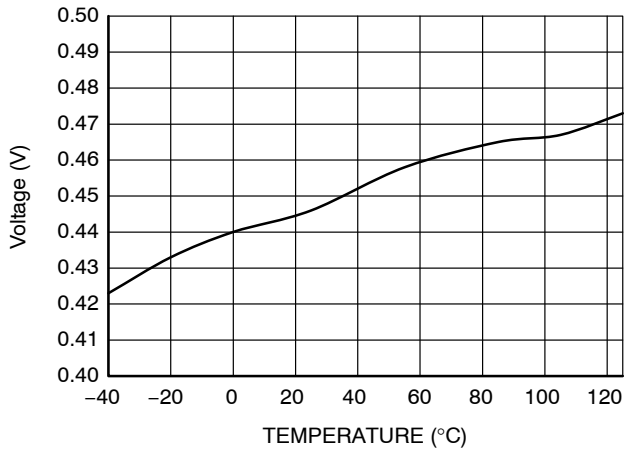


Figure 7. V<sub>CChyst</sub> vs. Temperature

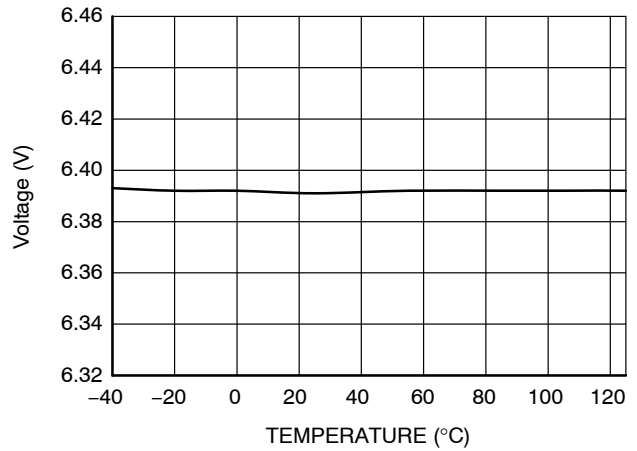


Figure 8. V<sub>Bon</sub> vs. Temperature

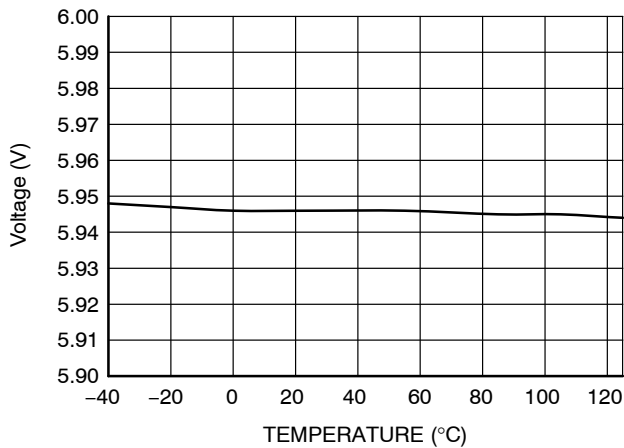


Figure 9. V<sub>Boff</sub> vs. Temperature

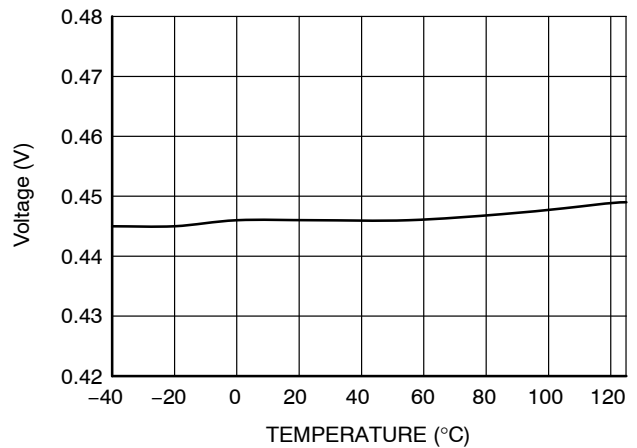


Figure 10. V<sub>Bhyst</sub> vs. Temperature

# NCP51313

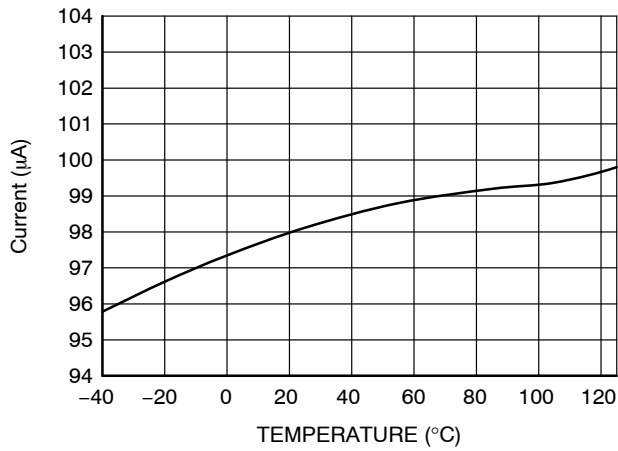


Figure 11.  $I_{CC1}$  vs. Temperature

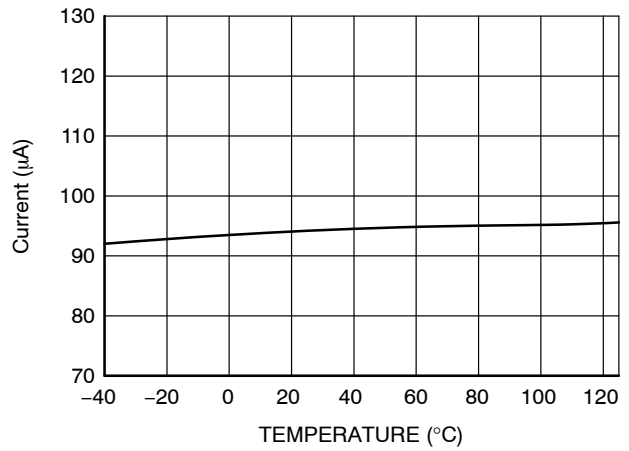


Figure 12.  $I_{CC2}$  vs. Temperature

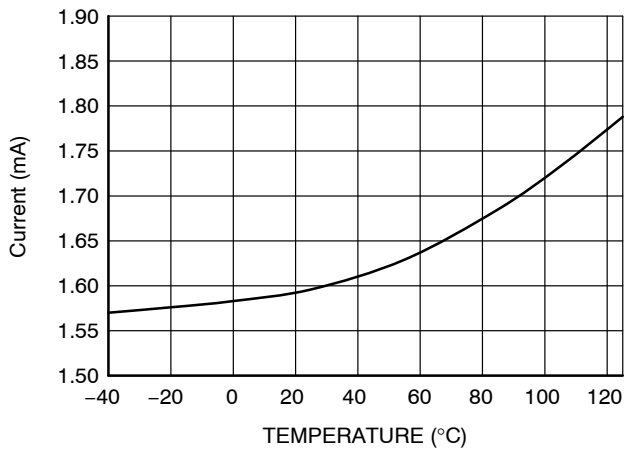


Figure 13.  $I_{B1}$  vs. Temperature

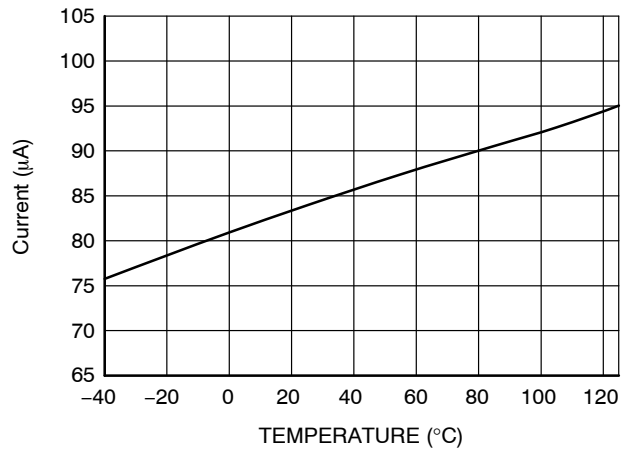


Figure 14.  $I_{B2}$  vs. Temperature

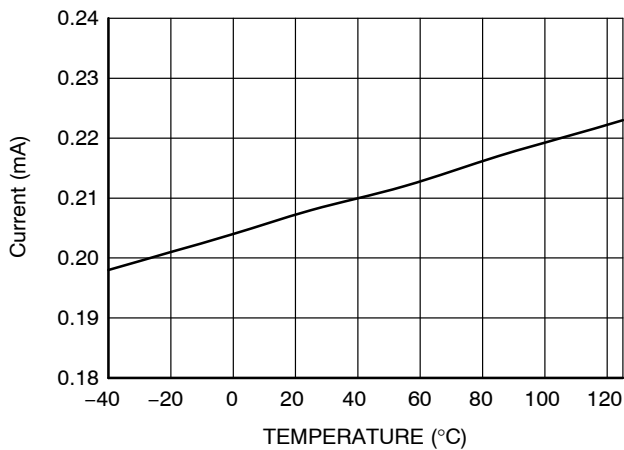


Figure 15.  $I_{B1\_noload}$  vs. Temperature

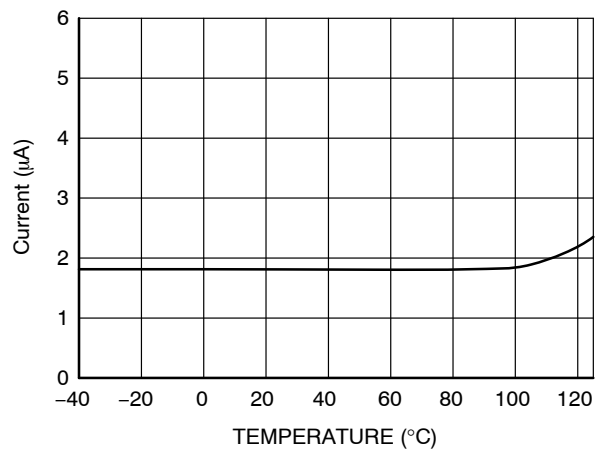


Figure 16.  $I_{HV\_LEAK}$  vs. Temperature

# NCP51313

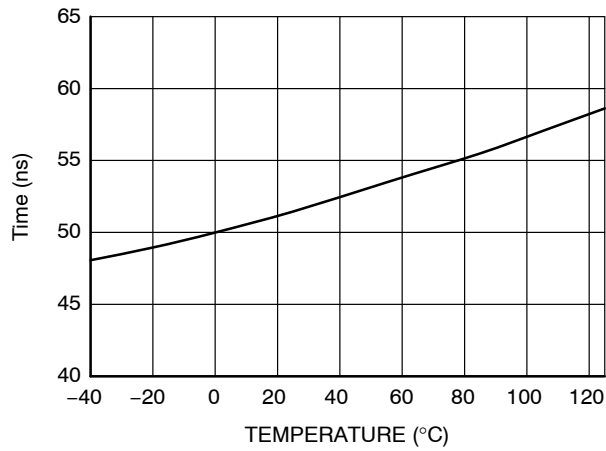


Figure 17.  $t_{ON}$  vs. Temperature

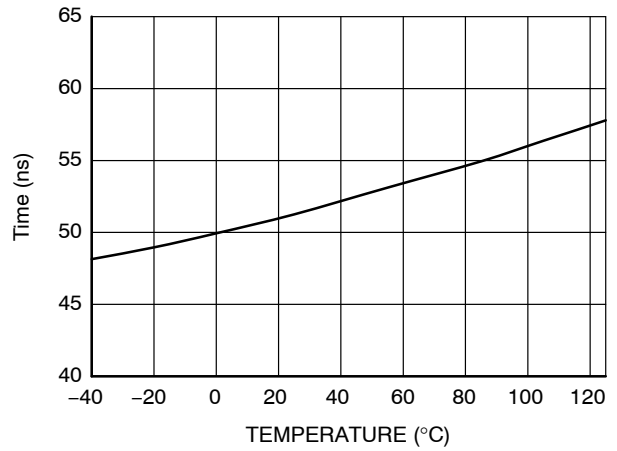


Figure 18.  $t_{OFF}$  vs. Temperature

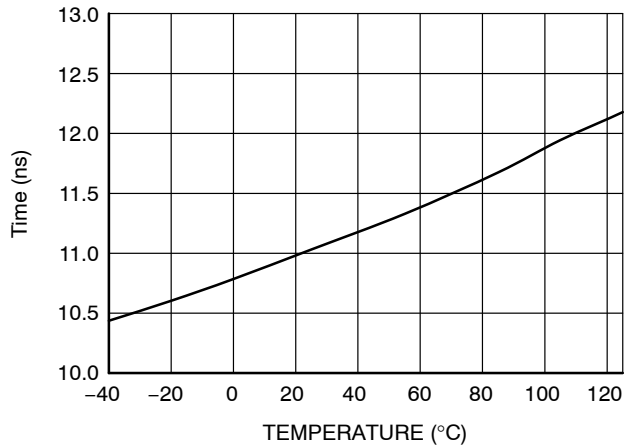


Figure 19.  $t_r$  vs. Temperature

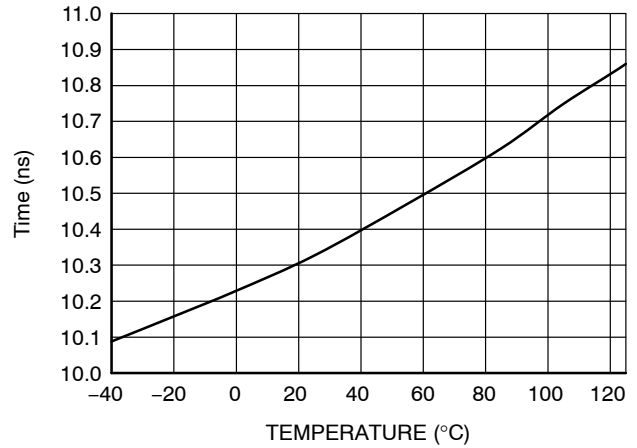


Figure 20.  $t_f$  vs. Temperature

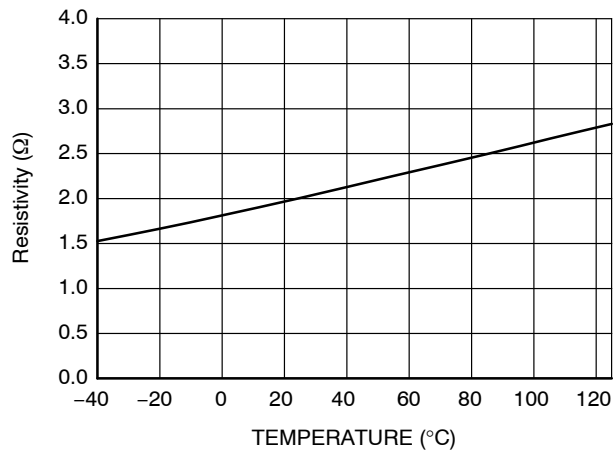


Figure 21.  $R_{OH}$  vs. Temperature

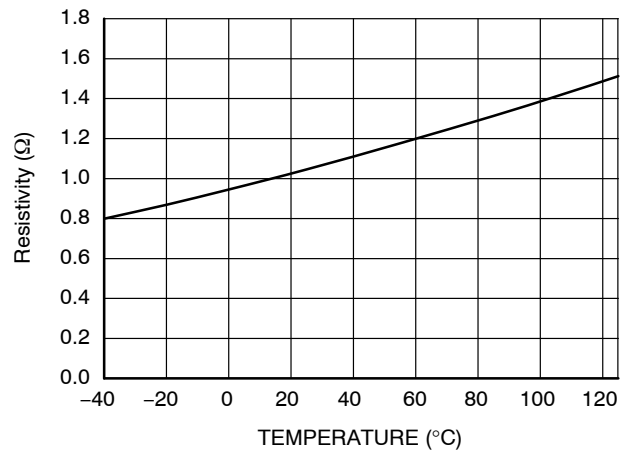


Figure 22.  $R_{OL}$  vs. Temperature

# NCP51313

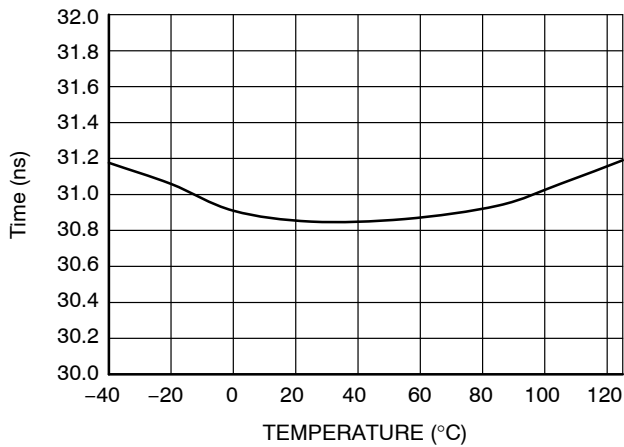


Figure 23.  $t_{FLT}$  vs. Temperature

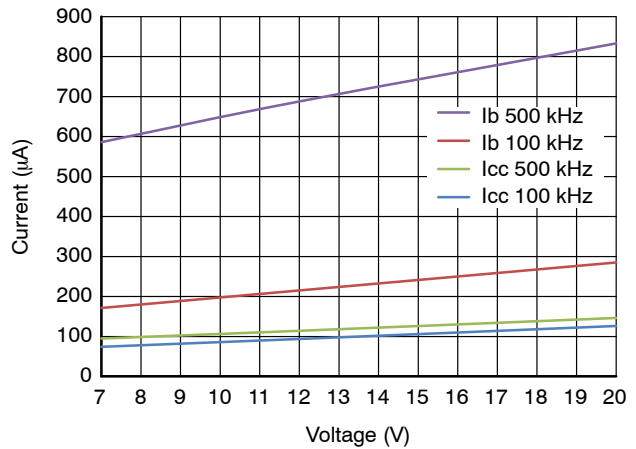


Figure 24. Current Consumption vs. Voltage, Load = 0 pF

## GENERAL DESCRIPTION

For some popular topologies high-side drivers are needed which perform the function of both buffer and level shifter. These devices can drive the gate of the topside MOSFETs whose source node is a dynamically changing node. The bias for the high side driver in these devices is usually provided through a bootstrap circuit.

In a bid to make modern power supplies more compact and efficient, power supply designers are increasingly opting for high frequency operations. High frequency operation causes higher losses in the drivers, hence reducing the efficiency of the power supply.

NCP51313 is a 130 V high side driver for DC-DC power supplies and inverters. NCP51313 offers best in class propagation delay, low quiescent current and low switching current at high frequencies of operation. This device thus

enables highly efficient power supplies operating at high frequencies.

NCP51313 is offered in two versions, NCP51313A/B. NCP51313A has a typical 50 ns propagation delay, while NCP51313B has propagation delay of 20 ns.

NCP51313 has one input pin  $I_N$  compatible with both CMOS and TTL logic allowing it to be used in a variety of applications. This device also includes features wherein, in case of floating input, the logic is still defined. NCP51313 has under voltage lock out feature which ensures operation at correct  $V_{CC}$  and  $V_B$  voltage levels. The output stage of NCP51313 has 2.0 A sourcing and 3.0 A sinking current which can effectively charge a 1 nF load in 11 ns and discharge a 1 nF load in 10 ns typically.

# NCP51313

## FEATURES

### Input Stage

NCP51313 has one input pin IN. The input stages of NCP51313 are TTL and CMOS compatible. This ensures that the input of NCP51313 can be driven with 3.3 V or 5 V logic signals from analog or digital PWM controllers or logic gates.

The input pin has Schmitt trigger to avoid noise induced logic errors. The hysteresis on the input pin is typically 0.7 V. This high value ensures good noise immunity.

NCP51313 comes with an important feature wherein output (HO) stays low in case the input pin is floating. At the input pin there is an internal pull down resistor to define its

logic value in case the pin is left open or NCP51313 is driven by open drain signal.

NCP51313 input pin is also tolerant to negative voltage below the GND pin level as long as it is within the absolute maximum ratings value (see Table 2). This tolerance allows the use of transformer as an isolation barrier for input pulses.

NCP51313A features a noise rejection function to ensure that any pulse glitch shorter than 30 ns typically will not change HO level. These features are well illustrated in the Figure 25.

NCP51313B has no such filters in the input stages. The timing diagram of NCP51313B is Figure 26.

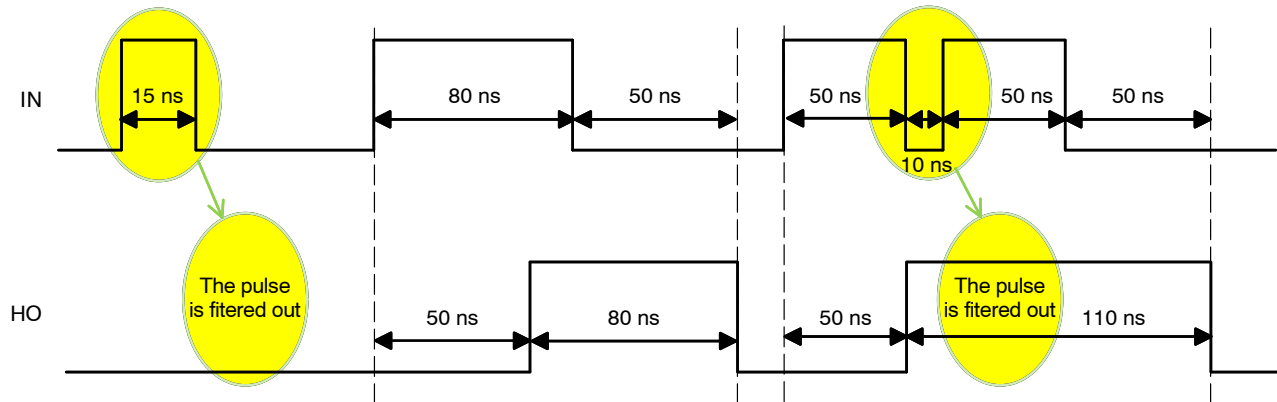


Figure 25. Input Filter (NCP51313A)

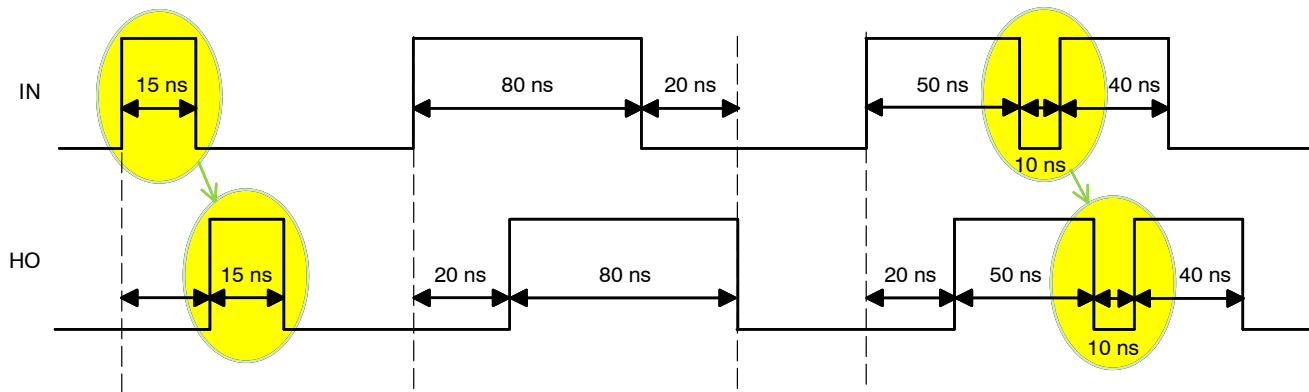
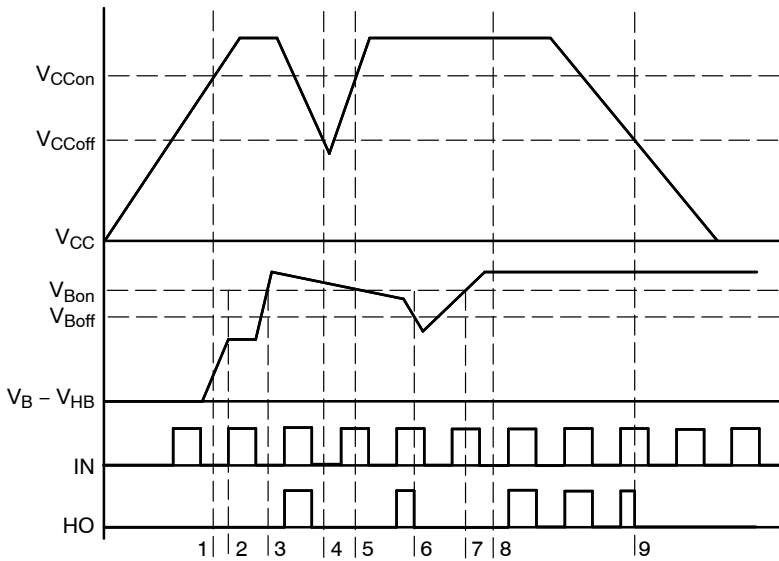


Figure 26. No Input Filter (NCP51313B)

# NCP51313



Legend:

Let's assume, the driver is used in HB configuration.

1. Vcc crossed Vcon level. No action. A low side MOSFET is (or has been) turned on, current flows from Vcc to Cboot via bootstrap diode.
2. Cboot is not fully charged after first pulse. HO stays low.
3. Vb cross Vbon level. IN is in L, output stays in L. Vb and Vcc are above Vxon levels, pulses can pass the driver.
4. Vccoff level is crossed, no pulses can pass the driver.
5. Vcon level crossed, Vbon has been crossed earlier, the current pulse is not transferred.
6. Vboff level is crossed while HO is H. HO is set to L immediately.
7. Vbon level crossed. Current (ongoing) pulse is ignored.
8. Vcc and Vb voltage are above Vxon level, all pulses can pass the driver. Steady state conditions.
9. Vccoff level is crossed while HO is in H. HO is set to L immediately. From now on, no pulse will pass the driver.

Figure 27. UVLO Timing Diagram

## Under Voltage Lock-out

NCP51313 has under voltage lockout protection. The function of the UVLO circuits is to ensure that there is enough supply voltages ( $V_{CC}$  and  $V_B$ ) to correctly bias driver circuit. This also ensures that the gate of external MOSFET is driven at an optimum voltage.

If the  $V_{CC}$  or  $V_B$  is below the  $V_{CC}$  UVLO voltage, high side driver output (HO) remains low. Both the  $V_{CC}$  and  $V_B$  UVLO

circuits are provided with hysteresis feature. This hysteresis feature avoids errors due to ground noise in the power supply. The hysteresis also ensures continuous operation in case of a small drop in the bias voltage. This drop in the bias can happen when device starts switching MOSFET and the operating current of the device increases. The UVLO feature of the device is explained in the Figure 27.

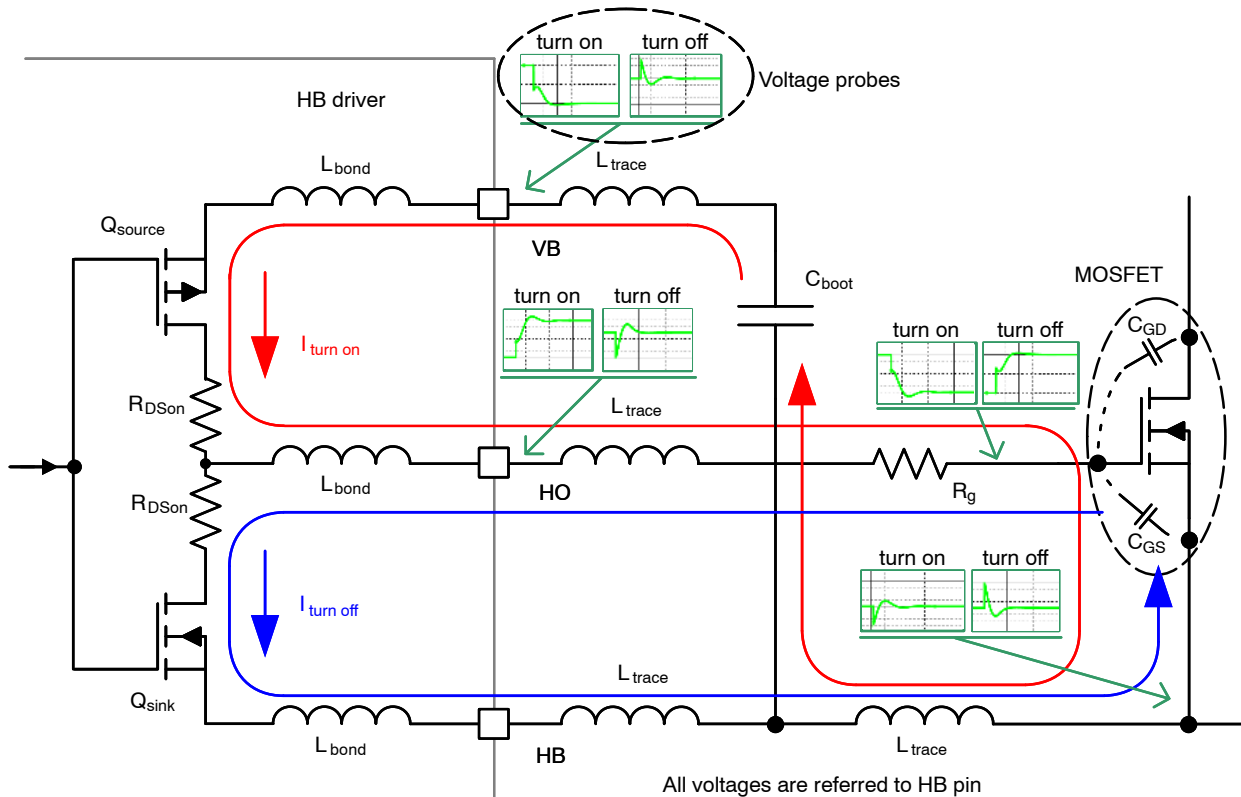


Figure 28. NCP51313 Turn ON-OFF Paths

# NCP51313

## Output Stages

The NCP51313 is equipped with a floating driver. The output stage of NCP51313 has 2.0 A source and 3.0 A sink current capability which can effectively charge a 1 nF load in 11 ns and discharge a 1 nF load in 10 ns typically.

Figure 28 shows the output stage structure and the charging and discharging path of the external power MOSFET and the bias supply  $V_B$ , the energy to charge the gate capacitance  $C_{GS}$ . When a logic high is received from input stage,  $Q_{source}$  turns on and  $V_B$  starts to charge  $C_{GS}$  through  $R_g$ . Once the  $C_{GS}$  is charged the external power MOSFET is conductive.

When a logic low signal is received from the input stage,  $Q_{source}$  turns off and  $Q_{sink}$  turns on providing discharge path for gate terminal. As seen in the figure, there are parasitic inductances in charging and discharging path of the  $C_{GS}$ . This can result in a little dip in the bias voltage  $V_B$ . If the  $V_B$  drops below  $UVLO$  the power supply can shut down the device.

## Short Propagation Delay

NCP51313 boasts of industry best propagation delay between input and output. NCP51313A has a typical of

50 ns propagation delay. The best in class propagation delay in NCP51313 makes it suitable for high frequency operation.

Since NCP51313B doesn't have the input filter included, the propagation delay is even shorter. NCP51313B offers 20 ns propagation delay between input and output.

The device allows 100 % duty cycle operation. The HO can be continuously in H or L state. In such case it is necessary to have a floating source to supply floating driver when using the driver under 100% DC.

## Negative Transient Immunity (NTI) Operating Conditions

In any HB switching applications the HB node is often pulled under the ground during the switching operation because of parasitic inductances and inductive load. These negative spikes may lead to malfunction or damage of the circuit.

The capability of NCP51313 to operate under negative voltage conditions is reported in NTI graph using below test set up.

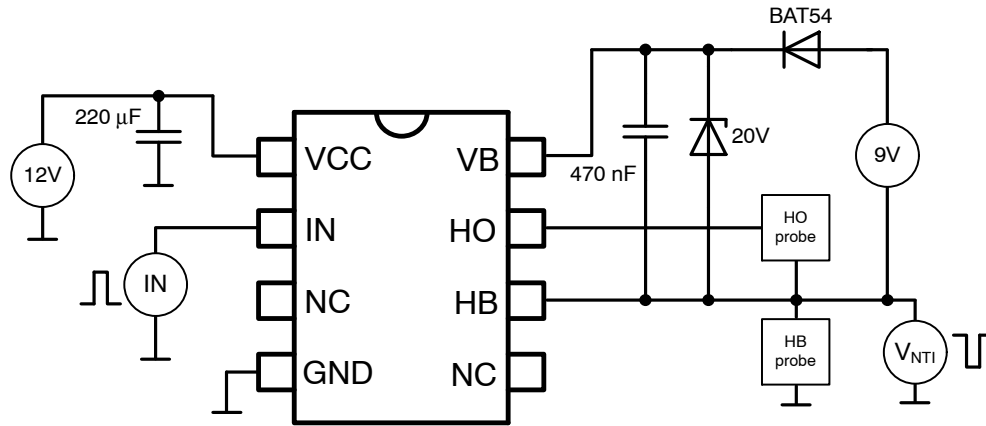


Figure 29. NTI Test Set Up

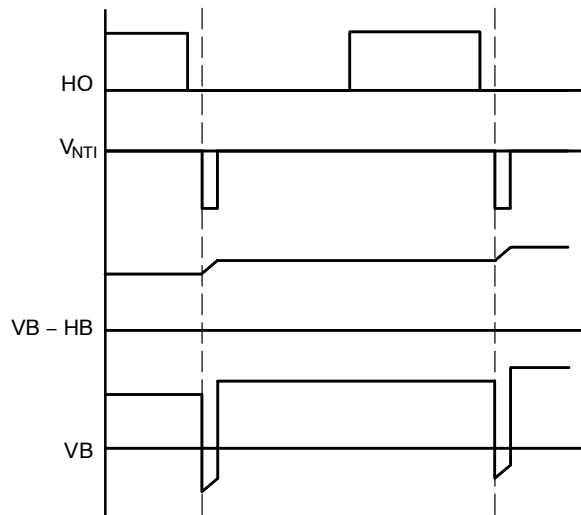
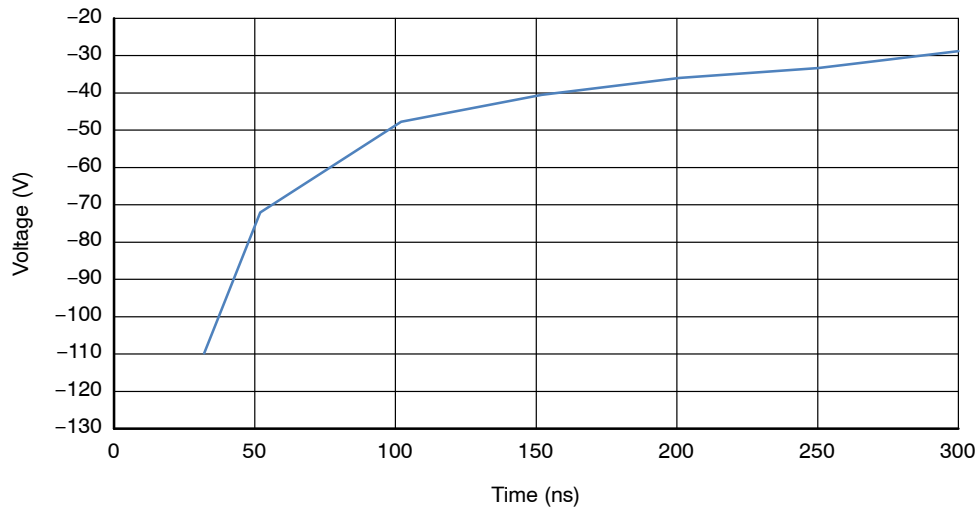


Figure 30. Timing Diagram

## NCP51313

NCP51313 robustness against negative spikes is shown in Figure 31. The result is a curve which shows negative

voltage level for specific pulse width under which driver could still operate properly.



**Figure 31. Indicative Negative Transient Immunity**

### IMPORTANT NOTE:

Even though above figure shows that NCP51313 is able to handle negative transient voltage conditions, it is highly recommended that the application circuit design is such that

it removes or at least always limit the negative transient voltage on VB pin as much as possible via careful PCB layout and proper component selection.

COMPONENT SELECTION

**C<sub>boot</sub> Capacitor Value Calculation**

NCP51313 has one floating driver for driving high side external MOSFET. The bias for the high side driver is

usually provided through a bootstrap circuit. A typical bootstrap circuit is shown in the Figure 32.

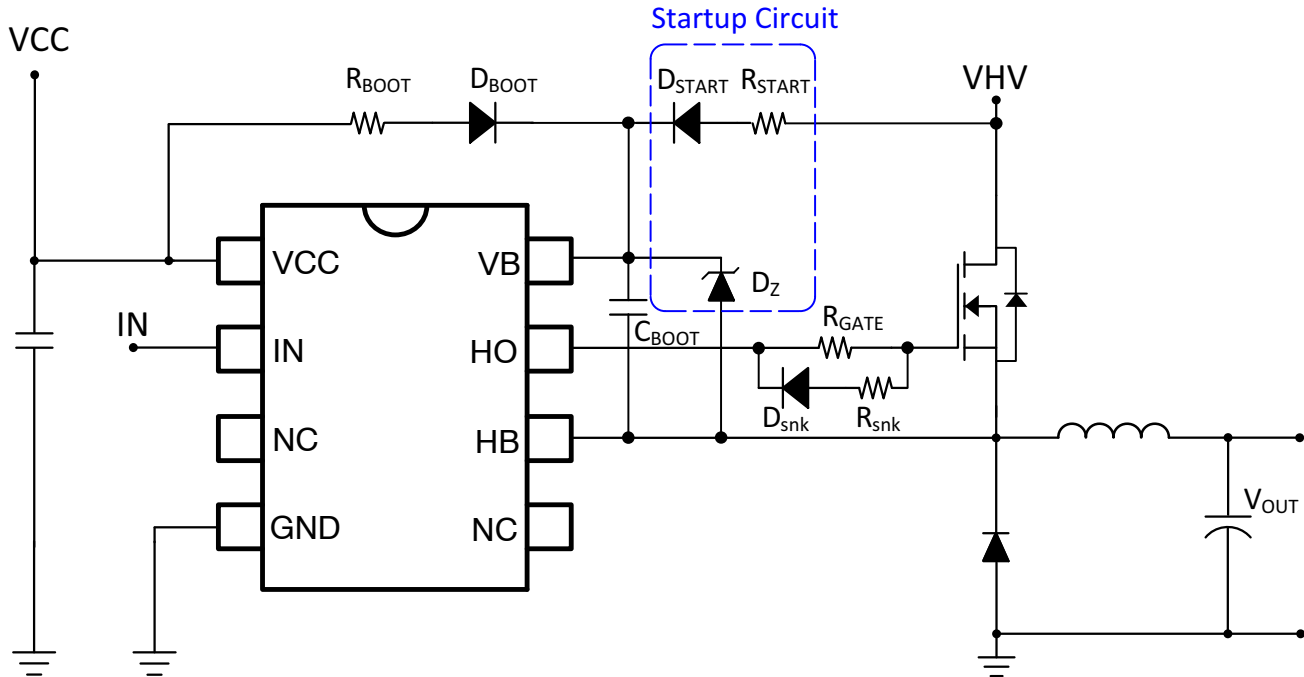


Figure 32. Bootstrap with Startup Circuit

The high side driver is biased by the C<sub>BOOT</sub> (bootstrap capacitor). As can be seen in the circuit, C<sub>BOOT</sub> will charge only when HB goes to GND level. Low value of C<sub>BOOT</sub> can result in a little dip in the bias voltages V<sub>B</sub>. If the V<sub>B</sub> drops below UVLO level the power supply can shut down the driver. Therefore choosing the right value of C<sub>boot</sub> is very important for a robust design.

In the beginning of the operation, HO cannot response if C<sub>BOOT</sub> is not charged above V<sub>Bon</sub> level, referenced to voltage between VB and HB pin.

Therefore, if there is no initial charging switch on low side, an additional start-up circuit should be considered for high side driver to ensure starting of the operation.

The start-up circuit, as shown in the Figure 32, consists of a startup resistor (R<sub>START</sub>), a startup diode (D<sub>START</sub>), and a Zener diode (D<sub>Z</sub>). In this startup circuit, startup diode D<sub>START</sub> serves as a second bootstrap diode used for charging the bootstrap capacitor (C<sub>BOOT</sub>) at power up. Bootstrap capacitor (C<sub>BOOT</sub>) is charged to the Zener diode of D<sub>Z</sub>, which is supposed to be higher than the driver's supply voltage (V<sub>CC</sub>) during normal operation. The charge current of the bootstrap capacitor and the Zener current are limited by the startup resistor. For best efficiency, the value of startup resistor should be selected to limit the current to a low value, since the bootstrap path through the startup diode is permanently in the circuit.

Expected voltage on C<sub>BOOT</sub> pin in steady state condition is depicted in Figure 33.

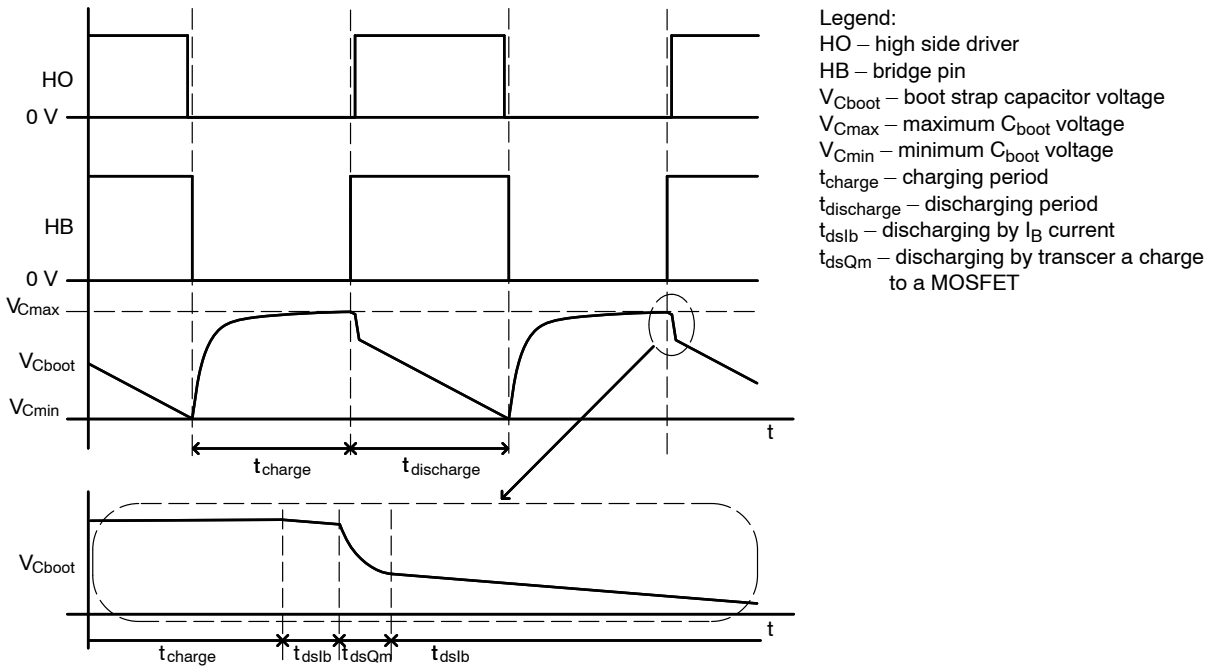


Figure 33. Boot Strap Capacitor Charging and Discharging

The curves are valid for ZVS (Zero Voltage Switching) observed in LLC applications. For hard switch the curves are slightly different, but from charge on  $C_{boot}$  point of view more favorable. Under the hard switch conditions the energy to charge  $Q_g$  (from zero voltage to  $V_{th}$  of the MOSFET) is taken from  $V_{CC}$  capacitor (through an external boot strap diode) so the voltage drop on  $C_{boot}$  is smaller. For the calculation of  $C_{boot}$  value the ZVS conditions are taken account.

The switching cycle is divided into two parts, the charging ( $t_{charge}$ ) and the discharging ( $t_{discharge}$ ) of the  $C_{boot}$  capacitor. The discharging can be divided even more to discharging by floating driver current consumption  $I_{B2}$  ( $t_{dslib}$ ), and to discharging by transferring energy from  $C_{boot}$  to gate terminal of the MOSFET ( $t_{dsQm}$ ) and discharging by leakage current of the bootstrap diode (not taken account). Discharging by  $I_{B2}$  becoming more dominant when driver runs at lower frequencies and/or during skip mode operation. To calculate  $C_{boot}$  value, follow these steps:

1. For example, let's have a MOSFET with  $Q_g = 49 \text{ nC}$ ,  $V_{CC} = 10 \text{ V}$ .
2. Charge stored in  $C_{boot}$  necessary to cover the period the  $C_{boot}$  is not supplied from  $V_{CC}$  line (which is basically the period the high side MOSFET is turned on). Let's say the application is switching at 100 kHz, 50 % duty cycle, which means the upper MOSFET is conductive for 5  $\mu\text{s}$ . It means the  $C_{boot}$  is discharged by  $I_{B2}$  current (100  $\mu\text{A}$  typ) for 5  $\mu\text{s}$ , so the charge consumed by floating driver is:

$$Q_b = I_{B2} \cdot t_{discharge} = 10 \mu \cdot 5 \mu = 500 \text{ pC} \quad (\text{eq. 1})$$

3. Total charge loss during one switching cycle is sum of charge to supply the high side driver and MOSFET's gate charge:

$$Q_{tot} = Q_g + Q_b = 49 \text{ n} + 500 \text{ p} = 49.5 \text{ nC} \quad (\text{eq. 2})$$

4. Let's determine acceptable voltage ripple on  $C_{boot}$  to 1 % of nominal value, which is 100 mV. To cover charge losses from eq. 2.

$$C_{boot} = \frac{Q_{tot}}{V_{ripple}} = \frac{49.5 \text{ n}}{0.1} = 495 \text{ nF} \quad (\text{eq. 3})$$

- $Q_g$  is equivalent gate charge of the MOSFET
- $I_{B2}$  is the boot quiescent current
- $t_{discharge}$  is the on time for HO
- $V_{ripple}$  is the allowed ripple voltage in the bootstrap capacitor

It is recommended to use a larger value so as to cover any variations in the gate charge and voltage with temperature.

**R<sub>boot</sub> Resistor Value Calculation**

To keep the application running properly, it is necessary to charge the  $C_{boot}$  again. This is done by external diode from  $V_{CC}$  line to  $V_B$  pin. In serial with the diode a resistor is placed to reduce the current peaks from  $V_{CC}$  line. The resistor value selection is critical for proper function of the high side driver. If too small high current peaks are drawn from  $V_{CC}$  line, if too high the capacitor will not be charged to appropriate level and the high side driver can be disabled by internal UVLO protection.

First of all keep in mind the capacitor is charged through the external bootstrap diode, so it can be charged to a maximum voltage level of  $V_{CC} - V_f$ . The resistor value is calculated using this equation:

$$R_{boot} = \frac{C_{charge}}{C_{boot} \cdot \ln\left(\frac{V_{max} - V_{Cmin}}{V_{max} - V_{Cmax}}\right)} = \frac{5 \mu}{1 \mu \cdot \ln\left(\frac{9.4 - 9.25}{9.4 - 9.35}\right)} \approx 4.6 \Omega \quad (\text{eq. 4})$$

Where:

- $t_{charge}$  time period the Cboot is being charged, usually the period the low side MOSFET is turned on,
- $C_{boot}$  boot strap capacitor value
- $V_{max}$  maximum voltage the  $C_{boot}$  capacitor can be theoretically charged to. Usually the  $V_{CC} - V_f$ . The  $V_f$  is forward voltage of used diode
- $V_{Cmin}$  the voltage level the capacitor is charge from
- $V_{Cmax}$  the voltage level the capacitor is charged to. It is necessary to determine the target voltage for charging, because in theory, when a capacitor is charged from a voltage source through a resistor, the capacitor can never reach the voltage of the source. In this particular case a 50 mV difference (between the voltage behind the diode and  $V_{Cmax}$ ) is used.

The resistor value obtained from eq. 4 does not count with the quiescent current  $I_{B2}$  of the high side driver. This current will create another voltage drop of:

$$B_{IB2\_drop} = R_{boot} \cdot I_{B2} = 4.6 \cdot 100 \mu \approx 460 \mu V \quad (\text{eq. 5})$$

The current consumed by high side driver will be higher, because the  $I_{B2}$  is valid when the device is not switching. While switching, losses by charging and discharging internal transistors as well as the level shifters will be added. This current will increase with frequency.

The additional 460  $\mu V$  drop will be added to  $V_{Cmax}$  value. The additional 460  $\mu V$  drop can be either accepted or the  $R_{boot}$  value can be recalculated to eliminate this additional drop.

The resistor  $R_{boot}$  calculated in eq. 4 is valid under steady state conditions. During start and/or skip operation the starting point voltage value is different (lower) and it takes more time to charge the boot strap capacitor. More over it is not counted with temperature and voltage variability during normal operation or the dynamic resistance of the boot strap diode (approximately 0.34  $\Omega$  for MURA160). From these reasons the resistor value should be decreased especially with respect to skip operation.

Boot strap resistor loss calculation.

$$P_{Rboot} \approx Q_{tot} \cdot V_{max} \cdot f \approx 49.5 n \cdot 9.4 \cdot 100 k \approx 46.3 mW \quad (\text{eq. 6})$$

Boot strap diode loss calculation.

$$P_{Dboot} \approx Q_{tot} \cdot V_f \cdot f \approx 49.5 n \cdot 0.6 \cdot 100 k \approx 3 mW \quad (\text{eq. 7})$$

Please keep in mind the value is temperature and voltage dependent. Especially  $C_{boot}$  voltage can be higher than calculated value. Also keep in mind, the Boot strap resistor power dissipation calculated in eq. 6 is valid for steady state conditions. For first Cboot charging, the power loss (the current) is much higher.

$$I_{Rboot} = \frac{C_{Vcc} - V_{Dboot} - V_{Cboot}}{R_{boot}} = \frac{10 - 0.6 - 0}{4.6} \approx 2 A \quad (\text{eq. 8})$$

$$P_{Rboot} = (C_{Vcc} - V_{Dboot} - V_{Cboot}) \cdot I_{Rboot} \approx (10 - 0.6 - 0) \cdot 2 \approx 18.8 W \quad (\text{eq. 9})$$

The Boot strap resistor must be designed to accept the current from eq. 8 and power loss from eq. 9 for a while.

### VCC Capacitor Selection

$V_{CC}$  capacitor value should be selected at least ten times the value of  $C_{boot}$ . In this case thus  $C_{Vcc} > 10 \mu F$ .

### IN Pin Input Filter

For PWM connection on the IN pin of the NCP51313, an RC filter can help to filter out high frequency input noise.

This filter is particularly important in case of NCP51313B where no internal filter is included.

The recommended value for  $R_{IN}$  and  $C_{IN}$  are as below.

$$R_{IN} = 100 \Omega$$

$$C_{IN} = 120 pF$$

### Rgate Selection

The  $R_{gate}$  are selected to limit the peak gate current during charging and discharging of the gate capacitance. This resistance also helps to damp the ringing due to the parasitic inductances, reduce  $dV/dt$  on HB pin to safe level and attenuate EMI radiation. If high  $dV/dt$  (during rise/fall edge and/or ringing after switching) is applied on HB pin, it can cause unexpected behavior of the driver.

On the other hand, too high resistor will increase power loss on MOSFETs, which leads to lower efficiency. It is recommended to start evaluation with a high resistor value and decrease the value if behavior is safe under all conditions. We recommend to have at least a 4.7  $\Omega$  resistor between NCP51313 outputs and MOSFET's gate.

The resistors also help to decrease power dissipation of the driver, because part of the energy from charging and discharging  $C_{gs}$  is radiated on the resistors  $R_{gate}$  (and on  $R_{snk}$  if they are used) outside the driver see Figure 32. The gate resistor selection is tricky task. It depends on application, topology, on used MOSFETs, layout etc.

For example for  $R_{gate}$  value of 4.7  $\Omega$ , the peak source and sink currents would be limited to the following values.

$$I_{HO\_Source} = \frac{V_B}{R_{gate} + R_{OH} + R_g} = \frac{10}{7.7} \approx 1.3 A \quad (\text{eq. 10})$$

$$I_{HO\_Sink} = \frac{V_B}{R_{gate} + R_{OL} + R_g} = \frac{10}{6.7} \cong 1.5 \text{ A} \quad (\text{eq. 11})$$

Where:

$R_{OH}$   $R_{DSon}$  of internal source MOSFET (see parametric table  $R_{OH}$  parameter)

$R_{OL}$   $R_{DSon}$  of internal sink MOSFET (see parametric table  $R_{OL}$  parameter)

$R_g$  internal gate resistance of external MOSFET (see appropriate DS), in this case 1  $\Omega$ .

In some applications it is desired/advantageous to use separated current paths for charging and discharging the gate capacitance. For this purpose external MOSFET gate connection must be extended (see Figure 32). Two components  $R_{snk}$  and  $D_{snk}$  can be added in parallel to  $R_{gate}$  resistor. The charging path is now only through  $R_{gate}$  resistor, while discharging path is through  $R_{snk}$  and  $R_{gate}$  in parallel combination. Consider both resistors are the same value 10  $\Omega$ . The source current is calculated using eq. 10. The current is 769 mA.

$$I_{HO\_Sink} = \frac{V_B}{R_{gate} + (R_{OL} + R_g) \cdot 2} + \frac{V_B - V_{Dsnk}}{R_{snk} + (R_{OL} + R_g) \cdot 2} = \frac{9.4}{12} + \frac{8.8}{12} \cong 1.52 \text{ A} \quad (\text{eq. 12})$$

### Total Power Dissipation

Total power dissipation of NCP51313 is sum of partial dissipations which can be calculated as follows (for more details, please refer to [AND90004/D](#)).

1. Power loss of device (except drivers) while switching at appropriate frequency is calculated from current consumption at given voltage for specific frequency. The current can be estimated from Figure 24, or it could be calculated using these formulas:

$$I_{CCnoload} = -5.72 \cdot 10^{-6} \cdot V \cdot f + 51.4 \cdot 10^{-3} \cdot f + 3.98 \cdot V + 40.96 \quad (\text{eq. 13})$$

$$I_{Bnoload} = 25.8 \cdot 10^{-3} \cdot V \cdot f + 0.866 \cdot f + 5.93 \cdot V + 22.51 \quad (\text{eq. 14})$$

Where:

$f$  is frequency in kHz,

$V$  is voltage in V,

Calculated current will be in  $\mu\text{A}$ .

The power dissipation of device (without drivers) is equal to.

$$P_{logic} = P_{HS} + P_{LS} = (V_{boot} \cdot I_{Bnoload}) + (V_{CC} \cdot I_{CCnoload}) = (9.4 \cdot 189 \cdot 10^{-6}) + (10 \cdot 86 \cdot 10^{-6}) = 2.6 \text{ mW} \quad (\text{eq. 15})$$

2. Power loss of driver

$$P_{driver} = (Q_g \cdot V_B) \cdot f = (49 \cdot 10^{-9} \cdot 9.4) \cdot 100 \cdot 10^3 \cong 46 \text{ mW} \quad (\text{eq. 16})$$

$Q_g$  is total gate charge of the used MOSFET.

3. Level shifter power loss

$$P_{lvshft} = (V_{HV} + V_B) \cdot f \cdot (Q_S + Q_R) = (100 + 9.4) \cdot 100 \cdot 10^3 \cdot (166 + 166) \cdot 10^{-12} \cong 3.6 \text{ mW} \quad (\text{eq. 17})$$

Where:

$V_{HV}$  is DC link voltage, here 100 V,

$V_B$  is boot strap voltage, here 9.6 V,

$f$  is switching frequency, here 100 kHz,

$Q_S, Q_R$  is energy needed to transfer information from LS part to HS part of the driver. The worst case is ZVS mode. In hard switch mode is  $Q_S$  very small, as the set pulse comes when HB pin is on low voltage.

4. HS leakage power loss

$$P_{leak} = I_{HV\_LEAK} \cdot (V_{HV} + V_B) \cdot DC = 2 \cdot 10^{-6} \cdot (100 + 9.4) \cdot 0.5 \cong 0.1 \text{ mW} \quad (\text{eq. 18})$$

Where:

$V_{HV}$  is DC link voltage, here 100 V,

$V_B$  is boot strap voltage, here 9.4 V,

$DC$  is duty cycle, here 50 %.

5. Total Power Loss (Hard Switching)

$$P_{total} = P_{logic} + P_{driver} + P_{lvshft} + P_{leak} = (2.6 + 46 + 3.6 + 0.1) \cdot 10^{-3} \cong 52.3 \text{ mW} \quad (\text{eq. 19})$$

Increasing Junction temperature ( $t_j$ ) compared to Ambient temperature ( $t_a$ ) is

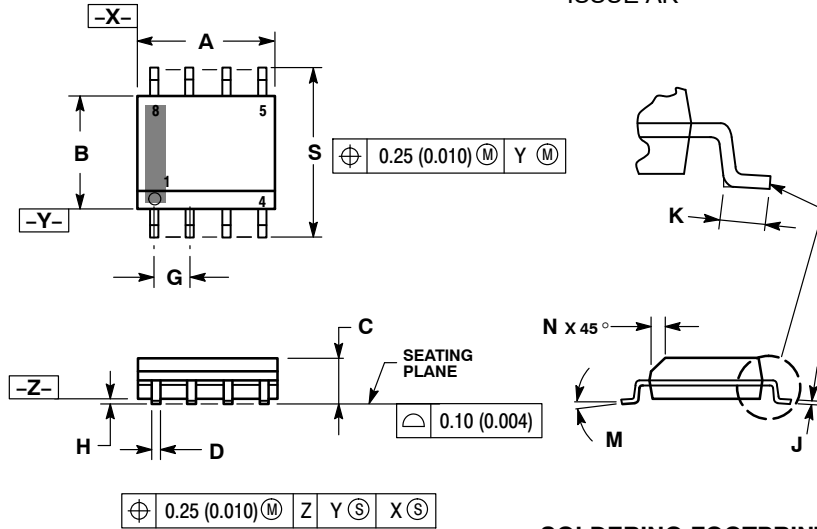
$$t_j = R_{\theta JA} \cdot P_{total} = 130 \cdot 0.052 \cong 6.8 \text{ K} \quad (\text{eq. 20})$$

The temperature calculated in eq. 20 is the value which has to be added to ambient temperature. In case the ambient temperature is 30°C, the junction temperature will be 36.8°C.

# NCP51313

## PACKAGE DIMENSIONS

### SOIC-8 NB CASE 751-07 ISSUE AK

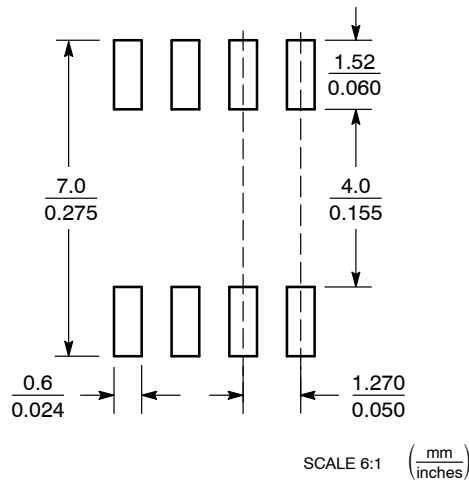


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

#### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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