Single 2.6 A, Low-Side Gate Driver with Over Current Protection

NCP51105

1

TSOP−6
CASE 318G−02

The NCP51105 is a high current low side gate driver designed to drive Power MOSFET and IGBT. The logic input is compatible with CMOS and TTL output. The NCP51105 has OCP pin to provide over current protection with negative voltage detected across switching current sensing resistor and EN pin that be able to report faults status to external controller such as MCU. EN pin must be pulled up to higher voltage than threshold for normal operation while it will be pulled down to disable output in all fault conditions. Internal V_{DD} circuitry provides an under−voltage lockout function by holding the output low until supply voltage is recovered into operating range and fault recovery time can be programmable by time constant set of resistance and capacitance connected to EN pin.

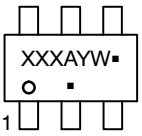
Features

- Wide Operating Voltage Range: up to 25 V
- 2.6 A Peak Sink/Source
- Shorter than 50 ns Propagation Delay Time
- Over Current Protection with Negative Voltage Sensing
- Input Logic Compatible with Wide Voltage Range for TTL & CMOS
- Programmable Fault Clear Time
- Under Voltage Lockout for MOSFET and IGBT
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Typical Applications

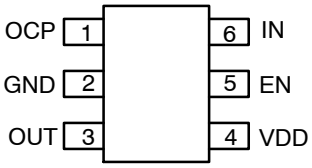
- Switch−Mode Power Supplies
- High−Efficiency MOSFET Switching
- Synchronous Rectifier Circuits
- DC−to−DC Converters
- Motor Control

MARKING DIAGRAM



XXX = Specific Device Code
A =Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Microdot may be in either location.)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP51105ASNT1G	TSOP−6	Tape & Reel 3000

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

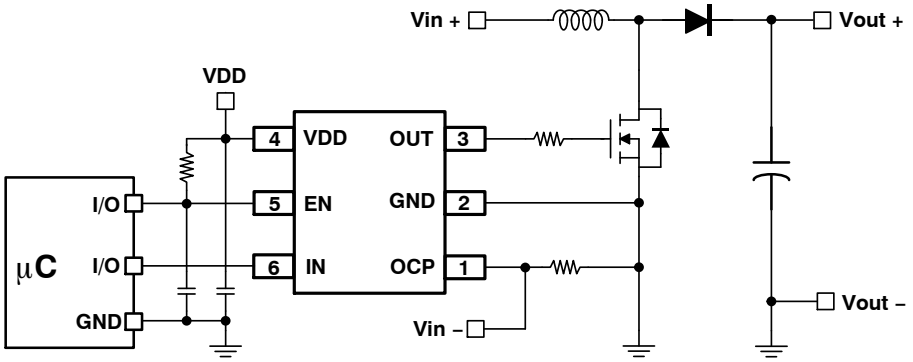


Figure 1. Simplified Application

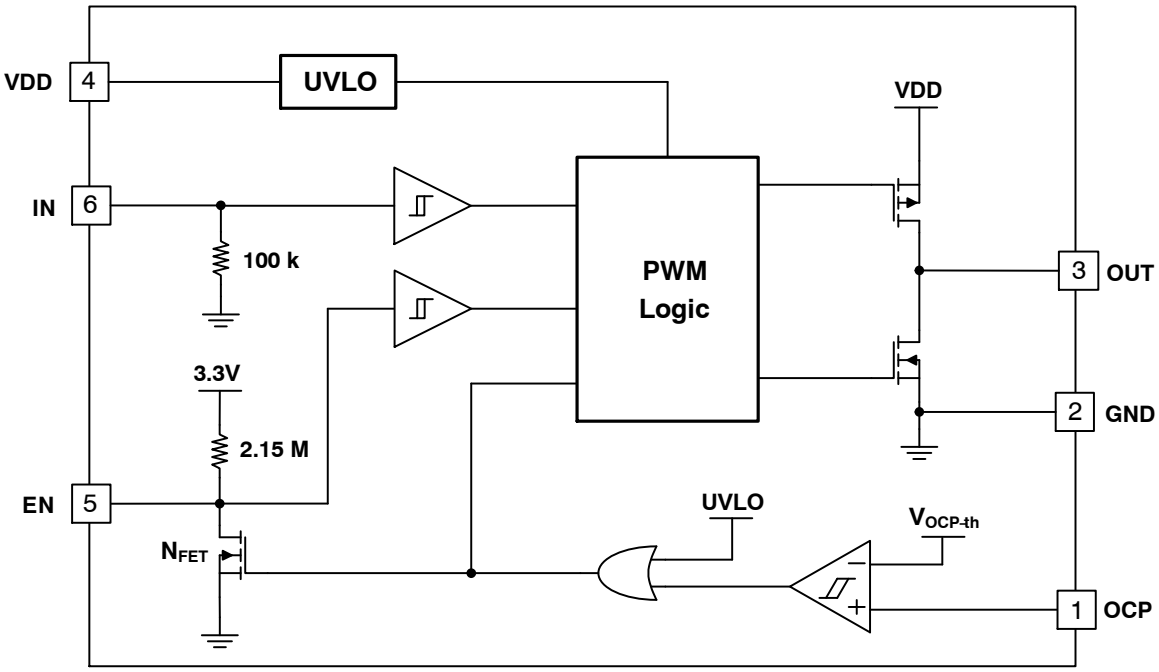


Figure 2. Internal Block Diagram

PIN CONNECTIONS

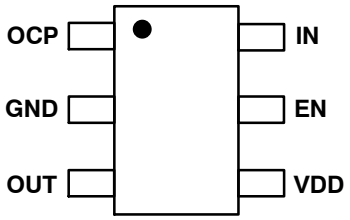


Figure 3. Pin Assignments – TSOP−6 (Top View)

PIN FUNCTION DESCRIPTION

Pin Name	Pin No.	Description
OCP	1	Current sense input with negative voltage
GND	2	Ground that all signals are referenced
OUT	3	Sourcing and sinking current output of driver
VDD	4	Bias supply input
EN	5	Enable I/O for three functions, 1. Logic input to enable output at higher V_{ENH} and to disable output at lower V_{ENL} 2. Reporting fault conditions such as over current and under voltage lockout 3. Programming fault clear time with external RC time constant
IN	6	Logic Input for gate driver output

IN / OUTPUT LOGIC TABLE

IN	UVLO (1)	OCP (2)	EN (3)	OUT	Description
L	H	L	H	L	OUT = Low by IN = L
H	H	L	H	H	OUT = High
H	H	H	L	L	OUT = Low by EN = L
H	L	X	L	L	OUT = Low by EN = L and UVLO = L
X	H	X	H	L	OUT = Low by IN = L (Pulled down by internal resistance)

1. UVLO = L is under−voltage lockout protection.
2. OCP = H is over−current protection.
3. EN = L is pulled down by internal N_{FET} turned on.

MAXIMUM RATINGS (Note 6)

Symbol	Parameter		Min	Max	Unit
V_{DD}	Supply voltage range		−0.3	25	V
V_O	Gate output voltage range		−0.3	V_{DD} + 0.3	V
V_{OCP}	Voltage range at current sense pin		−5	V_{DD} + 0.3	V
V_{EN}	Voltage range at enable pin		−0.3	V_{DD} + 0.3	V
V_{IN}	Logic input voltage range		−5	V_{DD} + 0.3	V
T_{STG}	Storage temperature		−65	150	°C
T_J	Junction temperature		−40	150	°C
T_L	Lead temperature (soldering, 10 seconds)		−	260	°C
ESD_{HBM}	Electrostatic Discharge Capability (Note 5)	Human Body Model	−	3.5	kV
ESD_{CDM}		Charge Device Model	−	1.0	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
5. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JESD22−A114
   ESD Charged Device Model tested per JESD22−C101
   Latch up Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78F
6. All voltage values are given with respect to GND pin.

THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
$R_{\theta JA}$	Junction−to−Ambient Thermal Impedance	250	°C/W
P_D	Power Dissipation	0.5	W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage Range	12.7	25	V
V_O	Gate output voltage range	GND	V_{DD}	V
V_{OCP}	Voltage range at current sense pin	−5	V_{DD}	V
V_{EN}	Voltage range at enable pin	0	V_{DD}	V
V_{IN}	Logic input voltage range	−5	V_{DD}	V
T_A	Ambient temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = 15 V, for typical values T_A = 25°C, unless otherwise specified. All voltage and current parameters are given with respect to GND pin.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
STATIC CHARACTERISTICS						
V_{DDUV+}	VDD UV start−up voltage threshold		11.2	11.9	12.7	V
V_{DDUV-}	VDD UV shut−down voltage threshold		10.3	11.0	11.8	V
V_{DDUVH}	VDD under voltage lockout voltage hysteresis		—	0.9	—	V
V_{INL}	Low level input voltage threshold		0.8	1.0	1.2	V
V_{INH}	High level input voltage threshold		1.9	2.1	2.3	V
V_{ENL}	Enable signal low threshold		0.8	1.0	1.2	V
V_{ENH}	Enable signal high threshold		1.9	2.1	2.3	V
V_{OH}	High level output voltage	I_O = 2 mA	—	0.02	0.1	V
V_{OL}	Low level output voltage		—	0.02	0.1	V
V_{OCP-th}	Threshold voltage for over current protection		−259	−246	−233	mV
I_{IN+}	Logic “1” input bias current	V_{IN} = 5 V	35	50	70	μA
I_{IN-}	Logic “0” input bias current	V_{IN} = 0 V	−1	0		μA
I_{QCC}	Quiescent VDD supply current	V_{IN} = 0 V or 5 V	—	700	1200	μA
I_{O+}	Output sourcing short circuit pulsed current (7)	V_O = 0 V, PW ≤ 2 μs	2	2.6	—	A
I_{O-}	Output sinking short circuit pulsed current (7)	V_O = 15 V, PW ≤ 2 μs	2	2.6	—	A
I_{FLT}	EN pull down sinking current	V_{EN} = 0.4 V	18	—	—	mA
V_{ACTSD}	Active shut down voltage	V_{DD} = open, I_{O+} / I_{O-} = 0.1	—	2	2.3	V
DYNAMIC CHARACTERISTICS						
t_{on}	Turn−on propagation delay	V_{IN} pulse = 5 V, Cload = 1 nF, Figure 24	—	25	45	ns
t_{off}	Turn−off propagation delay		—	25	45	ns
t_r	Turn−on rise time		—	5	—	ns
t_f	Turn−off fall time		—	5	—	ns
t_{DISA}	Disable propagation delay			25	45	ns
t_{OCPDEL}	Over current protection propagation delay	R_{FLTC} = 10 kΩ to V_{DD}, V_{OCP} Pulse = −0.5 V, Cload = 1 nF, Figure 23	—	230	350	ns
t_{OCPFLT}	OCP to low level EN signal delay	R_{FLTC} = 10 kΩ to V_{DD}, V_{OCP} pulse = −0.5 V, Figure 23	—	200	320	ns
t_{FLTC}	FAULT clear time	V_{DD} = 3.3 V, R_{FLTC} = 1 MΩ to V_{DD}, C_{FLTC} = 150 pF to GND, Figures 22, 23	80	103	130	μs
t_{BLK}	Over current protection blanking time (7)	R_{FLT} = 0 Ω, C_{FLT} = NC, V_{OCP} pulse = −0.5 V, Figures 22, 23	100	180	250	ns
t_{VDDUV}	VDD supply UVLO filter time (7)		—	2	—	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. This parameter, although guaranteed by design, is not tested in production.

TYPICAL CHARACTERISTICS

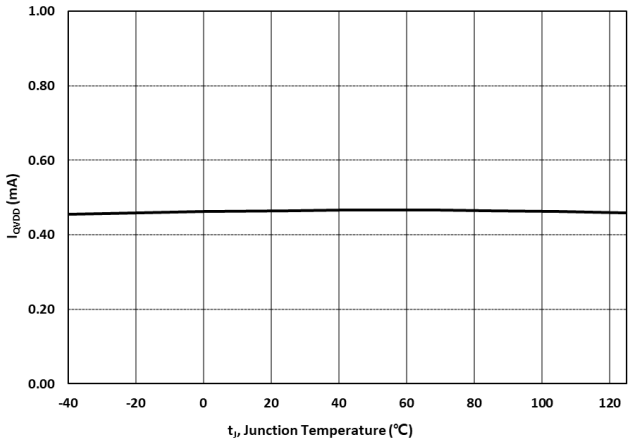


Figure 4. I_{QVDD} vs. Temperature

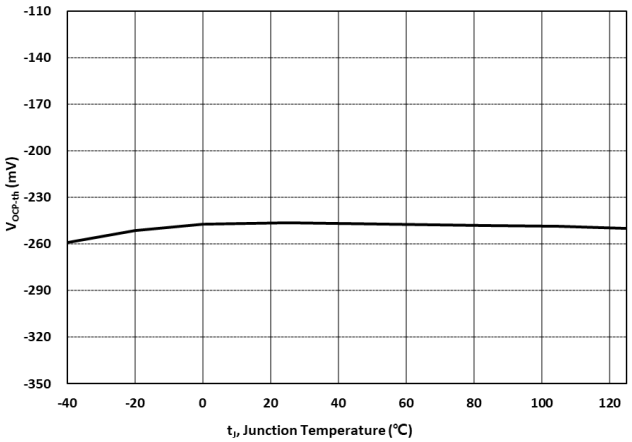


Figure 5. V_{OCP-th} vs. Temperature

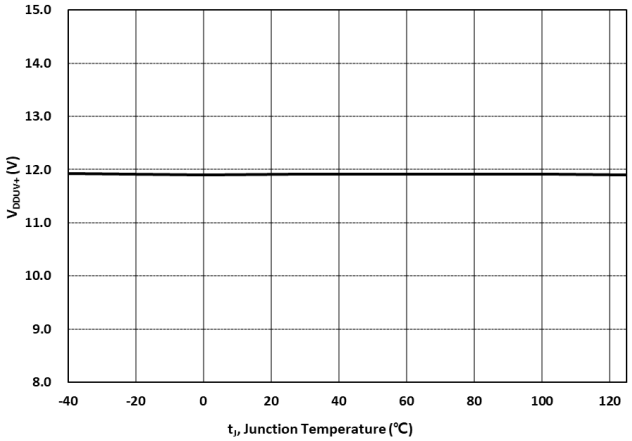


Figure 6. V_{DDUV+} vs. Temperature

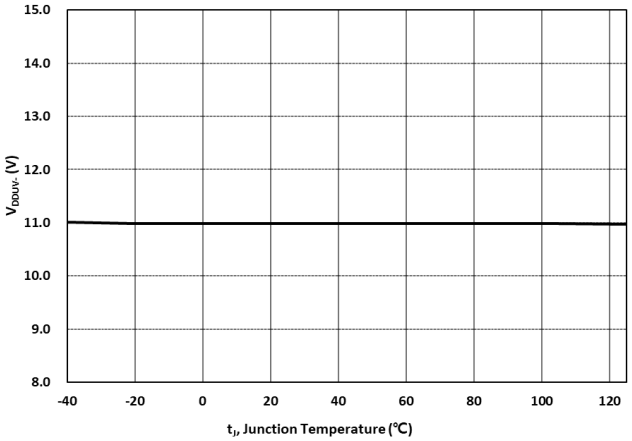


Figure 7. V_{DDUV-} vs. Temperature

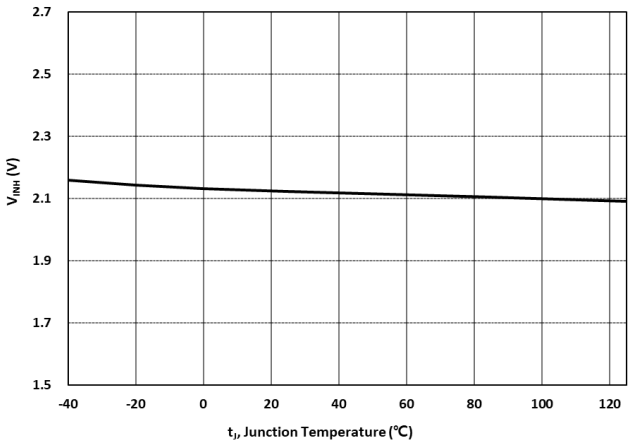


Figure 8. V_{INH} vs. Temperature

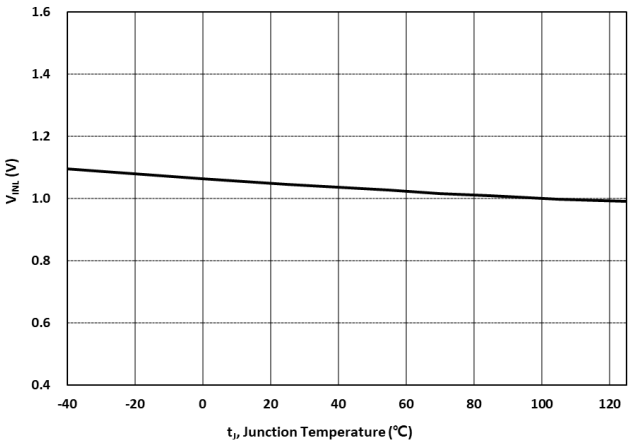


Figure 9. V_{INL} vs. Temperature

TYPICAL CHARACTERISTICS (continued)

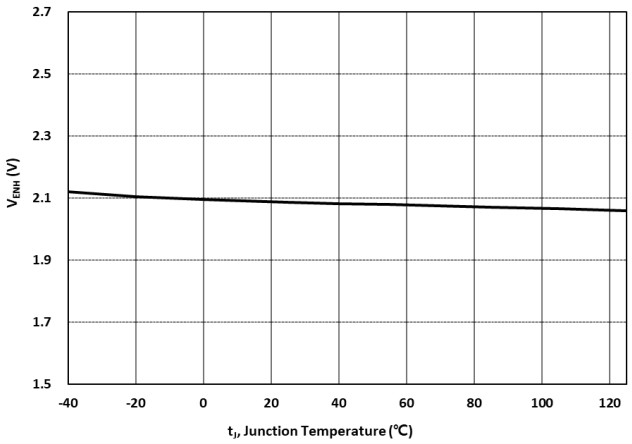


Figure 10. V_{ENH} vs. Temperature

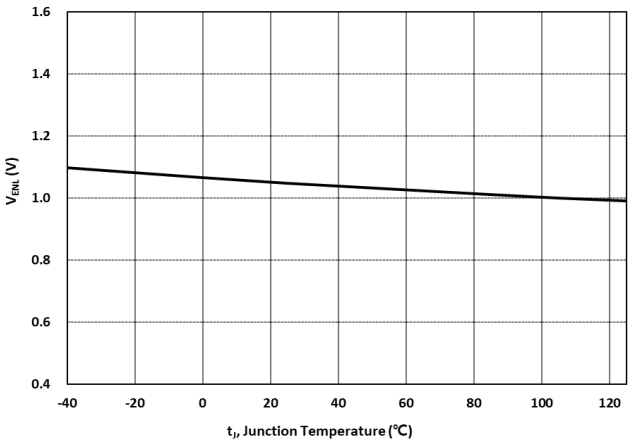


Figure 11. V_{ENL} vs. Temperature

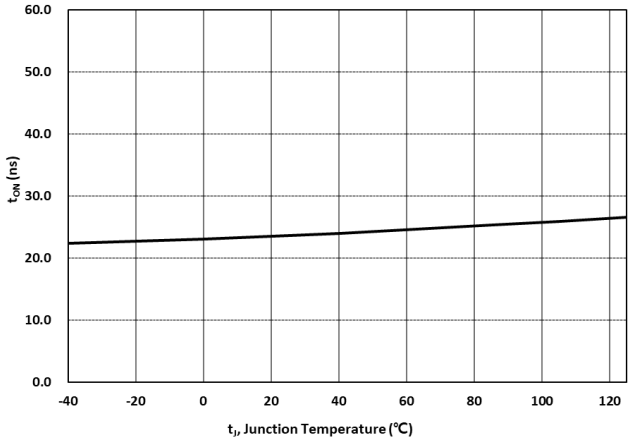


Figure 12. t_{ON} vs. Temperature

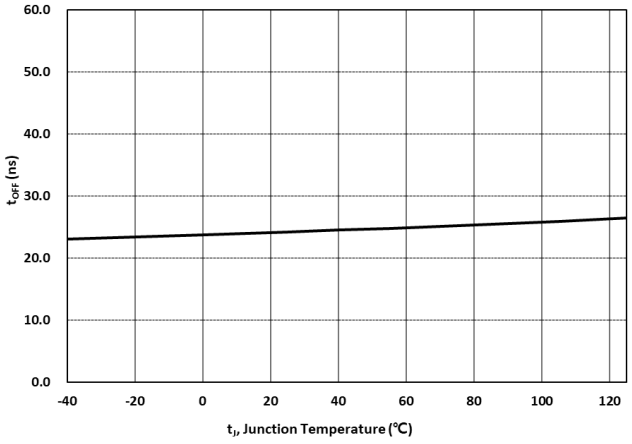


Figure 13. t_{OFF} vs. Temperature

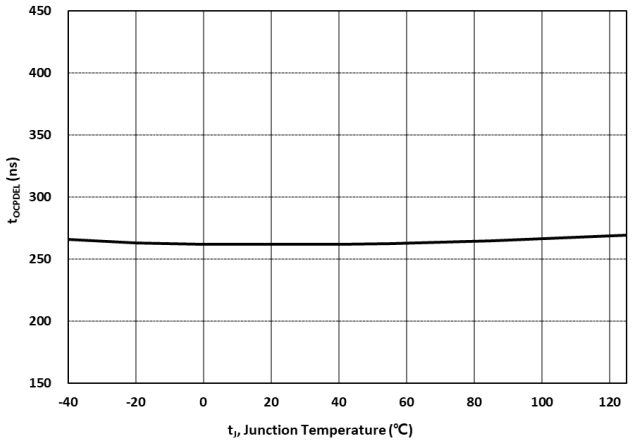


Figure 14. t_{OCPDEL} vs. Temperature

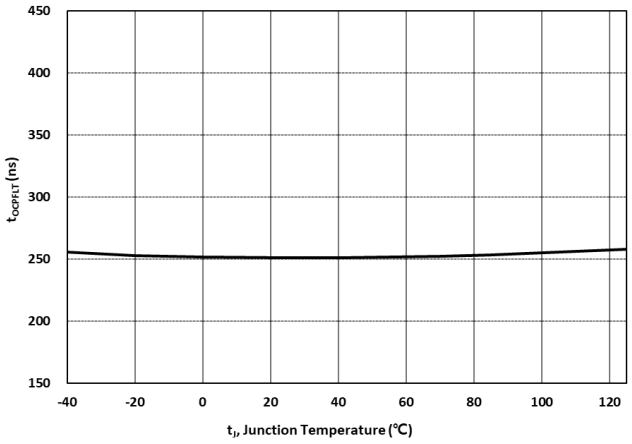


Figure 15. t_{OCPFLT} vs. Temperature

TYPICAL CHARACTERISTICS (continued)

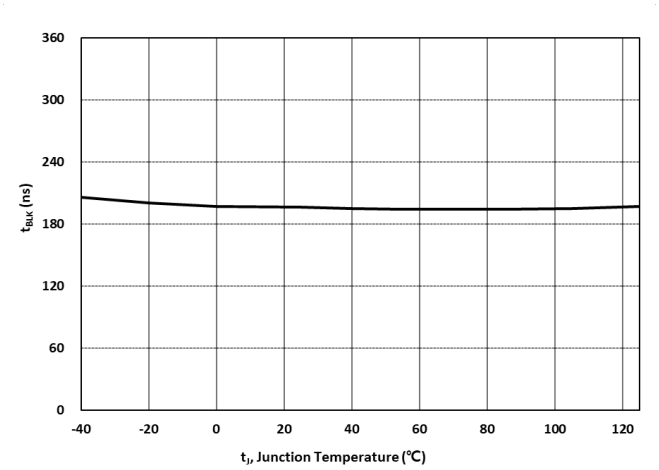


Figure 16. t_{BLK} vs. Temperature

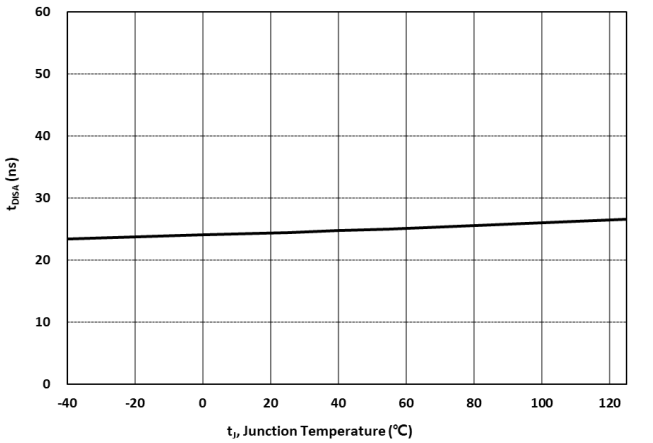


Figure 17. t_{DISA} vs. Temperature

General Description

NCP51105 is the single channel low side gate driver designed to drive Power MOSFET and IGBT with 2.6 A source and sink peak current capability. The logic threshold is compatible with both TTL and CMOS output and has about 1 V hysteresis for strong noise immunity. The over current of power devices can be detected through OCP pin by sensing negative voltage and the information for abnormal operation conditions can be provided by changing EN pin voltage level. When over current or UVLO conditions are detected, EN pin voltage is pulled down by turning on internal N_{FET} while the voltage is recovered to certain voltage levels via resistor connected with the internal or external voltage sources as long as fault conditions are disappeared. Internal circuitries provide an under−voltage lockout function holding the output low and allow the fault clear time to be programmable with external component values.

VDD Under Voltage Lock Out

NCP51105 has internal UVLO protection circuit which monitors the VDD supply voltage. The function of the UVLO circuits is to ensure so that the gate of external power devices is driven at an optimum voltage. The UVLO circuits have hysteresis that helps to avoid VDD chattering when the noise is influenced by switching power supply and when VDD bias voltage is dropped by IDD increased suddenly once switching operation begins. If the VDD is below the V_{DDUV-} (typical 11.0 V for A−Ver and 7.3 V for B−Ver) for more than filtering time, t_{VDDUV}, driver output is kept low regardless of the IN input status and EN pin is pulled down to GND by turning on internal N_{FET}. EN pin is charged by external voltage supply as long as VDD is higher than V_{DDUV+} for more than fault clear time, t_{FLTC}, that is determined by capacitance and resistance connected externally at VDD and EN pins. Driver out is also generated when IN high signal is applied after EN voltage is higher than V_{ENH}. However, for initial power up, EN pin voltage can't be charged until the internal logic configuration is ended completely after VDD becomes the voltage level, 6 V that PoR (Power on Reset) circuits are able to operate properly. Initial logic configuration period, t_{SET}, as shown in Figure 18 might be taken for about 13 ~ 15 μs.

As driver IC consumes the current from the VDD pin to bias the internal circuits, VDD circuits should be designed not only to supply safely the power required for driver operation but also to block efficiently noises delivered from external power switching circuits. Therefore, the bypass ceramic capacitor of 100 nF is recommended to be designed together with VDD decoupling capacitor and must be located as close as possible between VDD and GND pins to minimize switching noise influences.

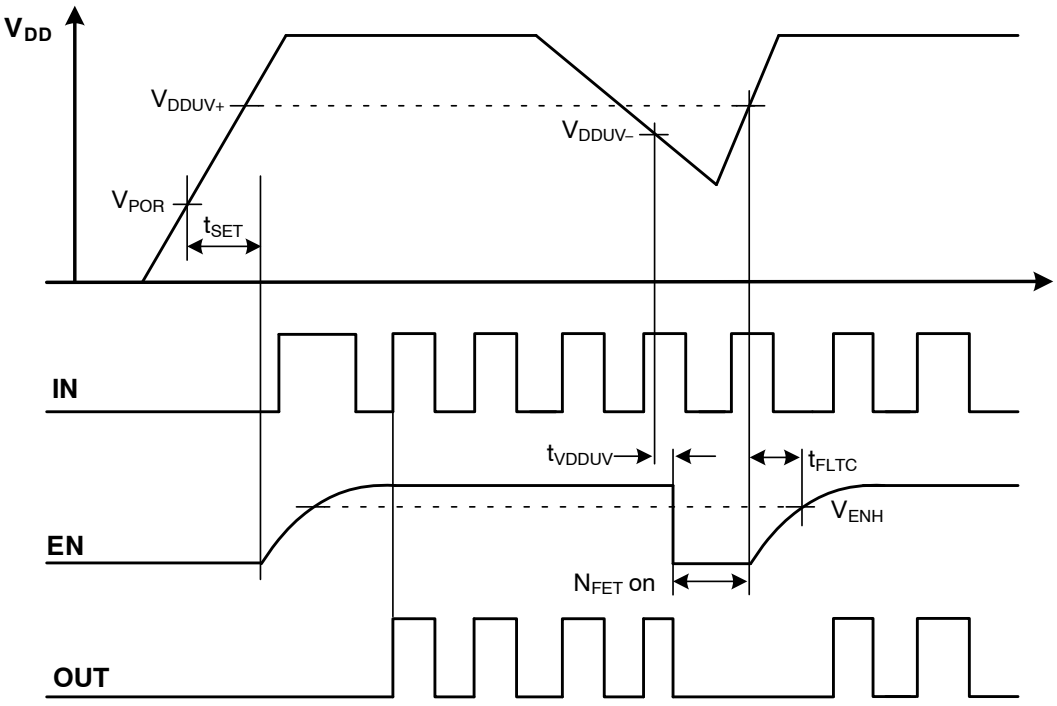


Figure 18. VDD UVLO Protection Timing Diagram

Input Stage

The input pin of NCP51105 is comparable with industry−standard TTL and CMOS logic thresholds regardless VDD supply voltage and has been designed with wider hysteresis voltage, 1.0 V that can provide strong noise immunity. As high input threshold is 2.1 V [Typ] and low threshold is 1 V [Typ], NCP51105 can be comparable with PWM signals delivered from different types of signal generators such as MCU and stand−alone PWM controllers used mainly in switching power supplies. NCP51105 has the feature of input threshold voltage levels with small tolerance across temperature and has the internal pull−down resistor so that the output can be held in the low state whenever the input pin is not connected to PWM controller or floating condition. Input logics for input signals are defined as shown Figure 19.

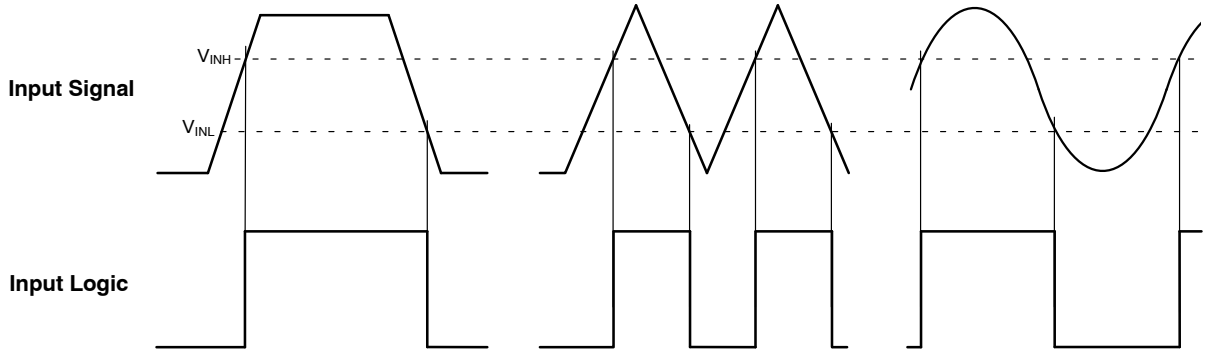


Figure 19. VDD UVLO Protection Timing Diagram

Output Stage

NCP51105 has composed of single driver to deliver typical source and sink current, 2.6 A at VDD = 15 V and can effectively charge and discharge 1 nF load. The bias voltage VDD charges gate capacitance Cgs of external power switch by turning on internal Q_{Source} when logic high signal is received from input stage. Similarly, charged Cgs is discharged by turning on internal Q_{Sink} when low input signal is delivered. The Figure 20 shows the output stage structure and the charging and discharging path of the external power MOSFET. As seen in the Figure 20, the parasitic inductances are presented in charging and discharging path of Cgs, so certain ringing voltage might be occurred in VDD and OUT pins.

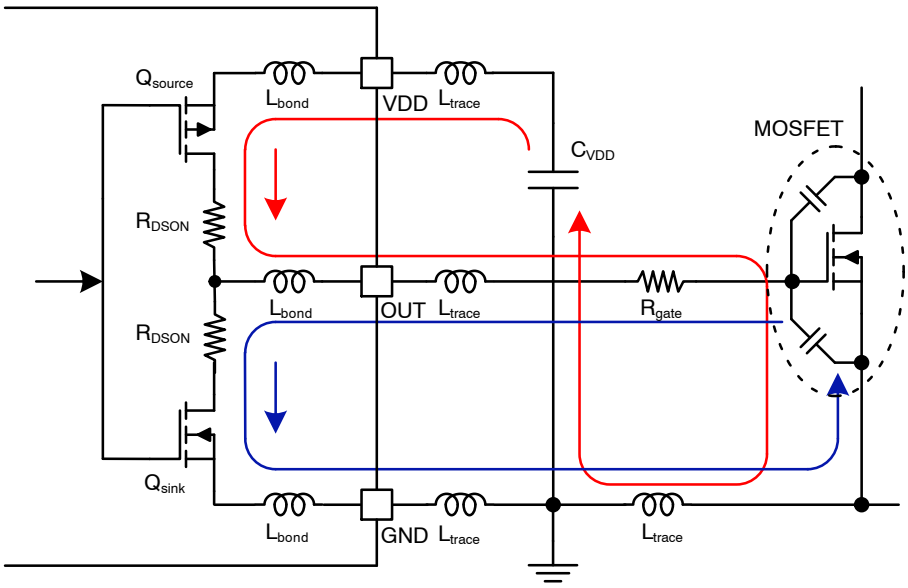


Figure 20. Sourcing and Sinking Current Path

Enable Input

NCP51105 offers enable functions that allow the device to be enable or disable the output. Figure 21 is showing the relationship among IN, OUT and EN signals. If EN pin voltage is higher than the threshold, V_{ENH}, the output will be active while it will be kept low if the voltage is lower than V_{ENL} or pulled down to GND. Internal 2.15 MΩ pull up resister is connected between EN pin to 3.3 V reference voltage and internal pull down N_{FET} is placed between EN pin and GND as shown in Figure 22. Therefore, floating EN pin can enable the output as long as the fault condition is not exiting but EN pin should be not only connected to VDD pin through the external pull−up resistor but also the small capacitor needs to be designed together with the resister to ensure proper operation from the noisy circumstance such as switch mode power supply.

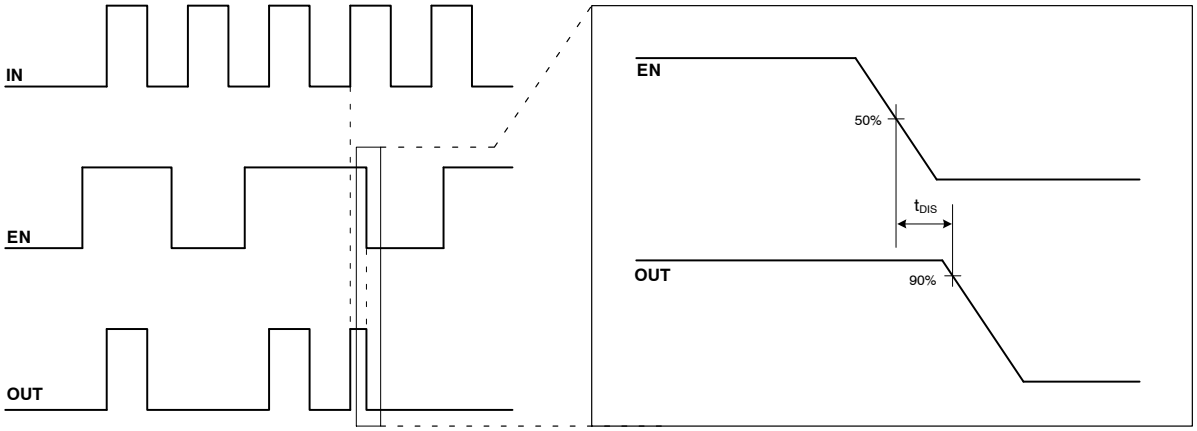


Figure 21. IN, EN, OUT Timing Diagram

Over Current Protection

NCP51105 provides over current protection features by detecting the negative voltage at OCP pin. When the voltage drop across the switching current sensing resister is bigger than threshold voltage, V_{OCP-th}, OCP is triggered through protection procedures in the blanking time, t_{BLK}. The purpose of t_{BLK} is to disable the over current detection to avoid triggering OCP by high dv/dt oscillations resulting from the parasitic LC components of the power switches and PCB traces. NCP51105 provide t_{BLK} options (200 ns, 250 and 300 ns) but additional filter composed of C_{FLT} and R_{FLT} as seen in Figure 22 might be essential in case an excessive oscillation is longer than t_{BLK} and can't ensure normal operation in severe noisy systems.

Once the negative voltage for triggering OCP is detected, the fault signal is generated initially and delivered to force internal N_{FET} to turn on and then EN pin is discharged fully to GND. As soon as EN pin voltage is lower than V_{ENL}, gate output is terminated immediately as seen in Figure 23. The time period for whole over current protection is completed within over current protection propagation delay, t_{OCPDEL} that includes the time delay, t_{OCPFLT} until EN signal is kept to low since OCP pin voltage had crossed threshold for t_{BLK}. Once OCP fault condition is removed, the internal N_{FET} is turned off and EN pin is recharged up to VDD. Figure 22 and Figure 23 are simplified OCP block diagram in boost converter and the timing diagram respectively.

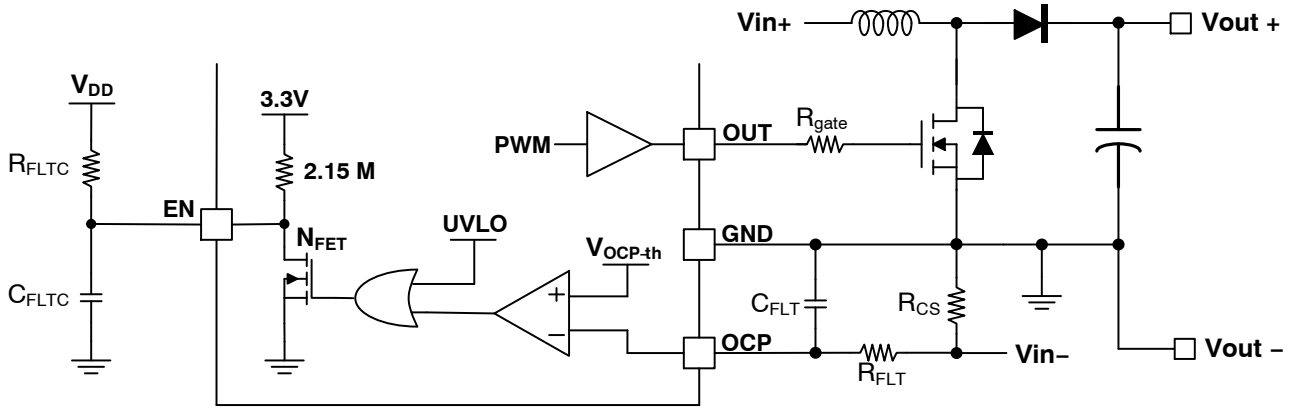


Figure 22. Simplified OCP Block Diagram & Boost Application

Fault Reporting and Clear Time

As NCP51105 have EN pin and it's able to report fault status to external controller with voltage change. Additionally, external RC network connected at both VDD and EN pins can be utilized to adjust fault clear time. EN pin voltage level is changed under fault conditions which OCP and VDD UVLO are triggered. As long as fault conditions are occurred, EN pin voltage is pulled down by turning on internal N_{FET} after the delay associated with fault types and will be remained to lower level than V_{ENL} until fault conditions are cleared. After the fault condition is disappeared, N_{FET} is turned off and capacitor connected at EN pin is recharged via voltage sources linked with internal and external resistors. Therefore, external controller can recognize the status by monitoring EN pin voltage level. The time period of EN pin voltage charged via internal and external voltage sources is programmable by time constant of R_{FLTC} and C_{FLTC} values as shown in Figure 23 and it can be also be changed by VDD level. The fault clear time, t_{FLTC}, can be obtained from following equation.

$$t_{FLTC} = -\left(\frac{R_{FLTC} + 2.15M}{R_{FLTC} \times 2.15M}\right) \times C_{FLTC} \times \ln\left(1 - V_{ENH} \times \frac{R_{FLTC} + 2.15M}{2.15M \times V_{DD} + 3.3\ V \times R_{FLTC}}\right)$$

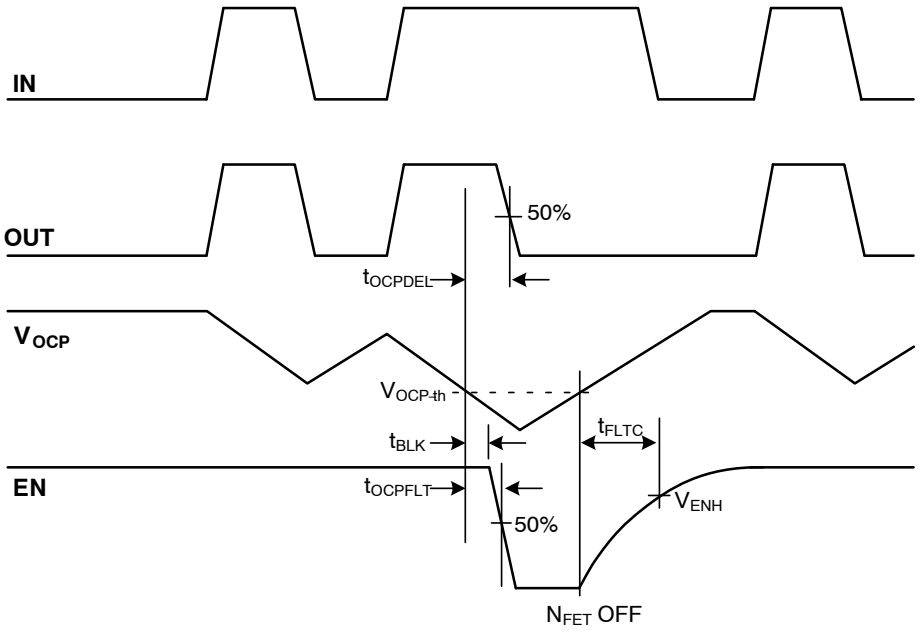


Figure 23. OCP Timing Diagram

Propagation Delay

Propagation delay is defined as the time taking from changing input logic signal to change gate output and is expressed as the delay time of ton and toff from input level of 90 % to output level of 10 % as shown in Figure 24. NCP51105 has short propagation delay, 35 ns (typ) and, allows to operate system with high frequency and to ensure tiny pulse distortions.

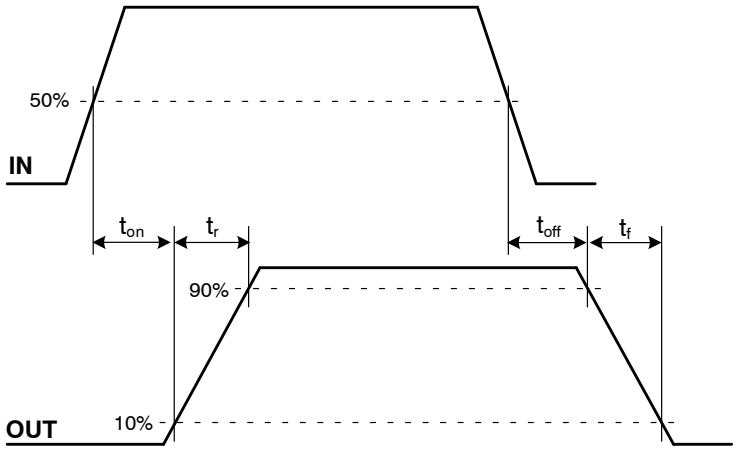


Figure 24. Propagation Delay, Rise and Fall Time

Layout Guidelines

The NCP51105 is a high−speed driver suitable for mid−high power application. To avoid any damage and/or malfunction during switching (and/or during transients, overloads, shorts etc.) proper PCB layout is very important to avoid a high parasitic inductance in high current paths. It is recommended to fulfill some rules in layout. One of possible layouts for the IC is depicted in Figure 25.

- Locate the driver device as close as possible to the power device to minimize the high current traces between output pin and gate of power transistor.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver to ensure noise filtering. For bypass capacitor, the multi−layer ceramic capacitor of low inductance SMD type is recommended.
- Current loop paths between Gate driver, VDD and Power switch should be minimized to keep the parasitic inductance small because high di/dt and severe voltage transient are occurred in these loops during switching operation.
- Separate power traces and signal trances.
- The star connection of ground is popular way to reduce noises induced from one current loop to another. Therefore, GND of the driver should be connected to the other circuit nodes at single point and the connected length should be as small as possible to minimize inductances.
- Do not place low voltage and sensitive traces in the proximity of HV node.

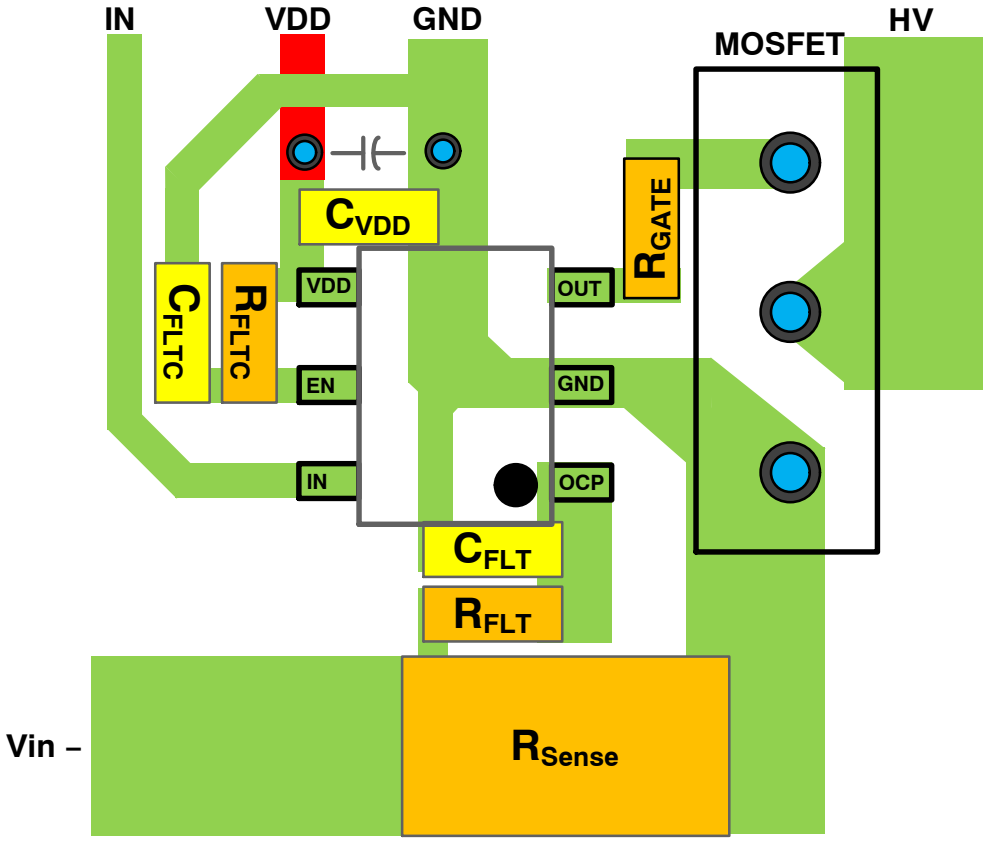
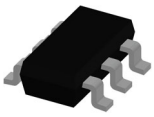


Figure 25. Recommended PCB Layout



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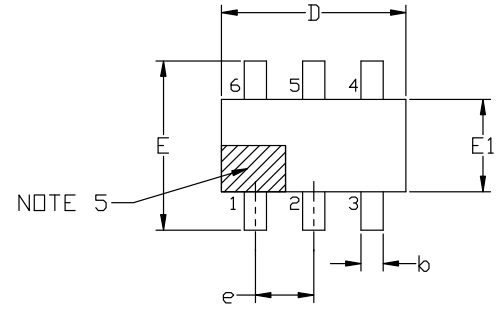
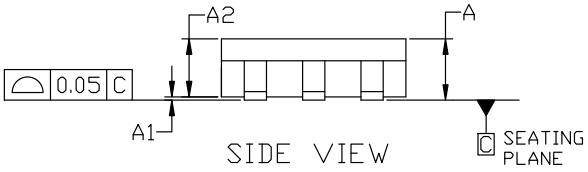
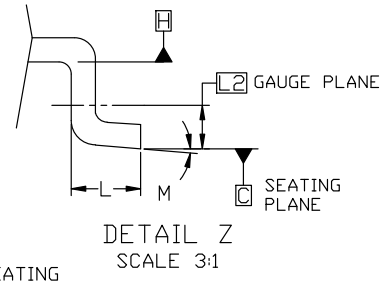
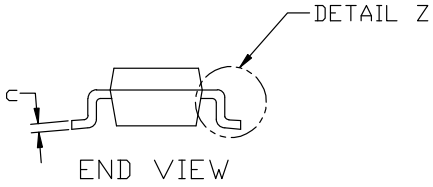


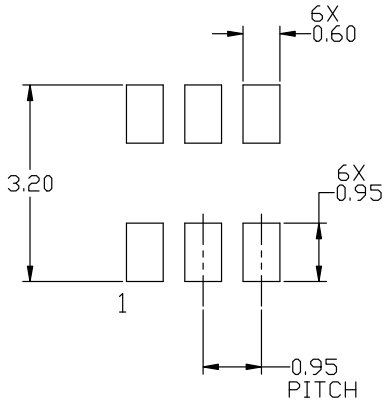






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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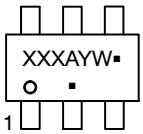
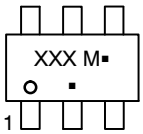
GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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