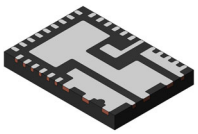
40 A Stackable Synchronous Buck Regulator with PMBus® Interface

NCP3286



WQFN34 5x7, 0.5P
CASE 510CL

MARKING DIAGRAM

NCP3286 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Designator

ORDERING INFORMATION

See detailed ordering and shipping information on page 49 of this data sheet.

The NCP3286, a highly−efficient stackable synchronous buck regulator with PMBus interface, is capable of operating with an input range from 3 V to 18 V and supporting up to 40 A continuous load currents. Higher output currents can be achieved by 2, 3, or 4 parallel NCP3286 devices operating as an interleaved multi−phase buck regulator.

The NCP3286 utilizes fixed−frequency current−mode control to provide accurate voltage regulation and fast transient response. Flexible programming of function and parameters supports multiple applications.

Features

- V_{IN}: 3 − 18 V with Input Feed−Forward
- V_{OUT}: 0.5 − 5.5 V with Remote Output Voltage Sense
- 40 A Continuous Output Current − Stackable to 160 A
- Programmable Fixed Frequency Current Mode Control
- Integrated 5 V LDO or External Supply
- Enable with Programmable VIN UVLO
- Programmable Boot−Up Voltage
- Programmable Soft−Start
- Pre−Bias Start−Up
- Programmable Current Limit
- Power Good Indicator
- Selectable Protection Mode (Latch−off or Hiccup)
- Under−Voltage and Over−Voltage Protection
- Output Discharge in Shutdown
- 150°C Operating Junction Temperature

Typical Applications

- Networking − Routers and Switches
- Telecom Digital Baseband
- Telecom Radio Unit
- Server and Desktop Computers, Notebooks, Gaming
- High Density Power Solutions
- DC/DC Modules
- General Purpose POL Regulator

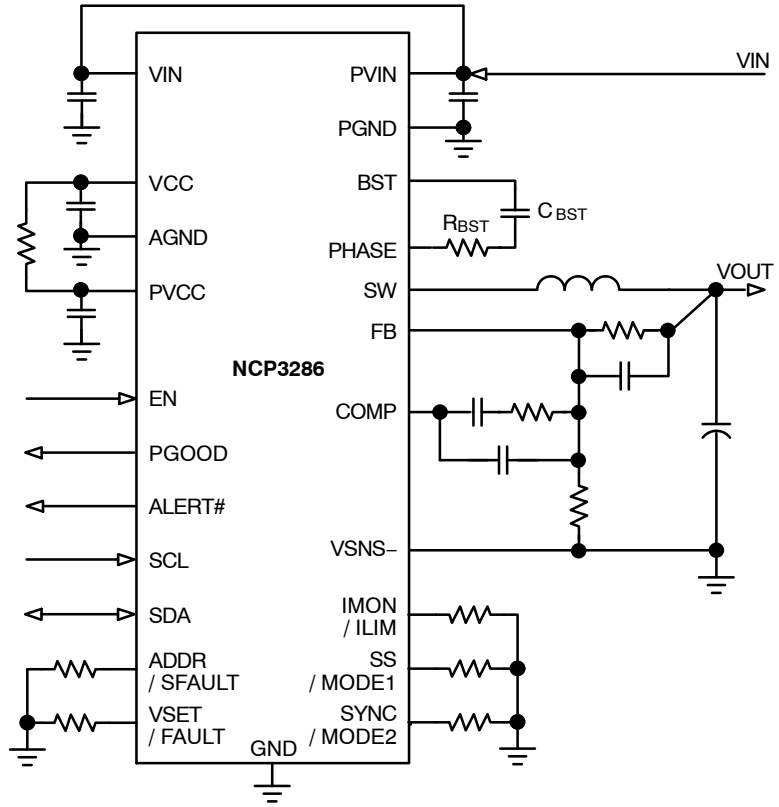


Figure 1. Typical 12 V_{IN}, 40 A Application Circuit for Single Input Supply (LDO Enabled)

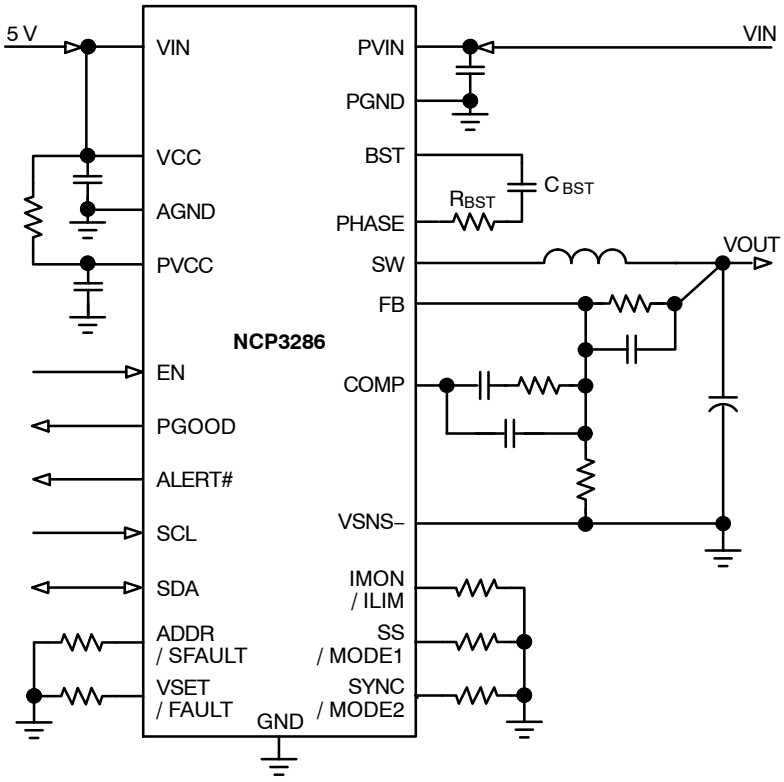


Figure 2. Typical 12 V_{IN}, 40 A Application Circuit with External 5 V VCC Supply (LDO Disabled)

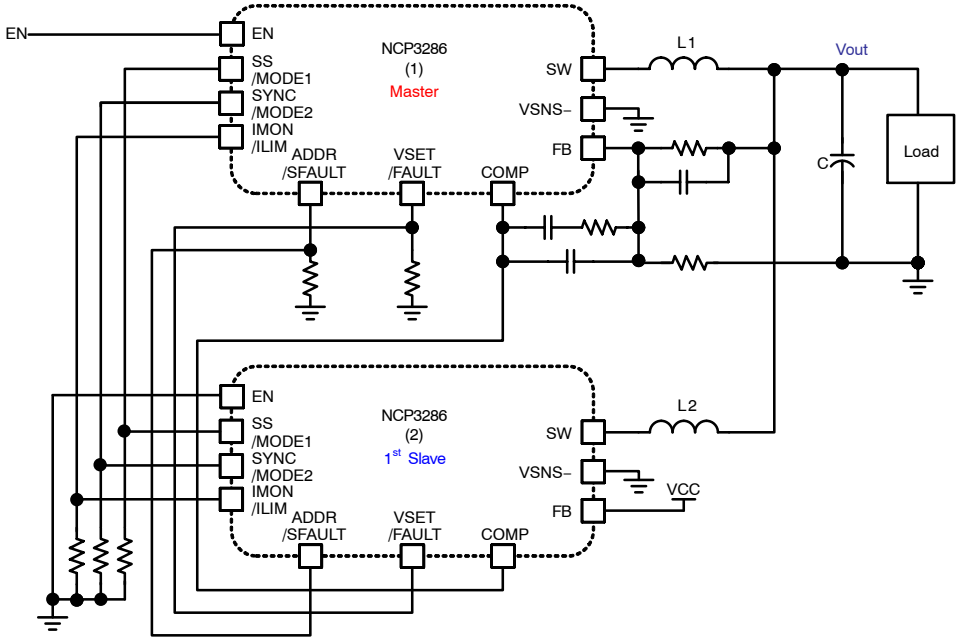


Figure 3. Typical 80 A Application Circuit with 2 Parallel NCP3286

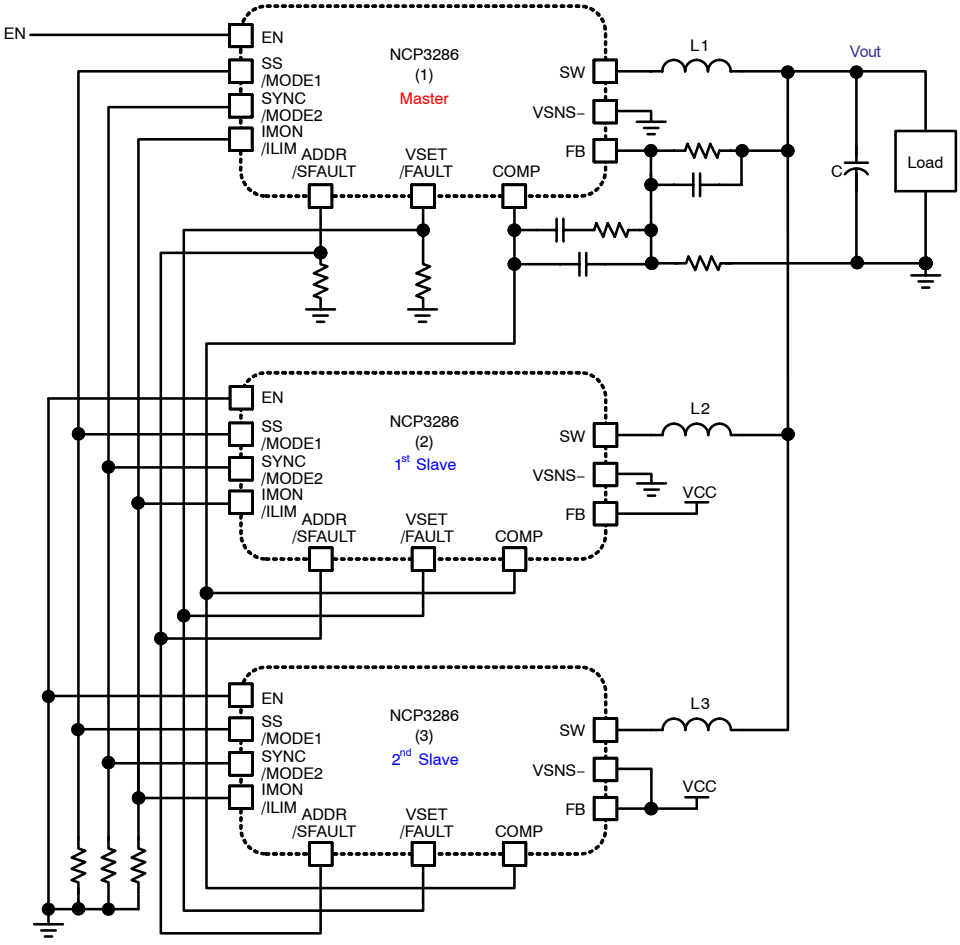


Figure 4. Typical 120 A Application Circuit with 3 Parallel NCP3286

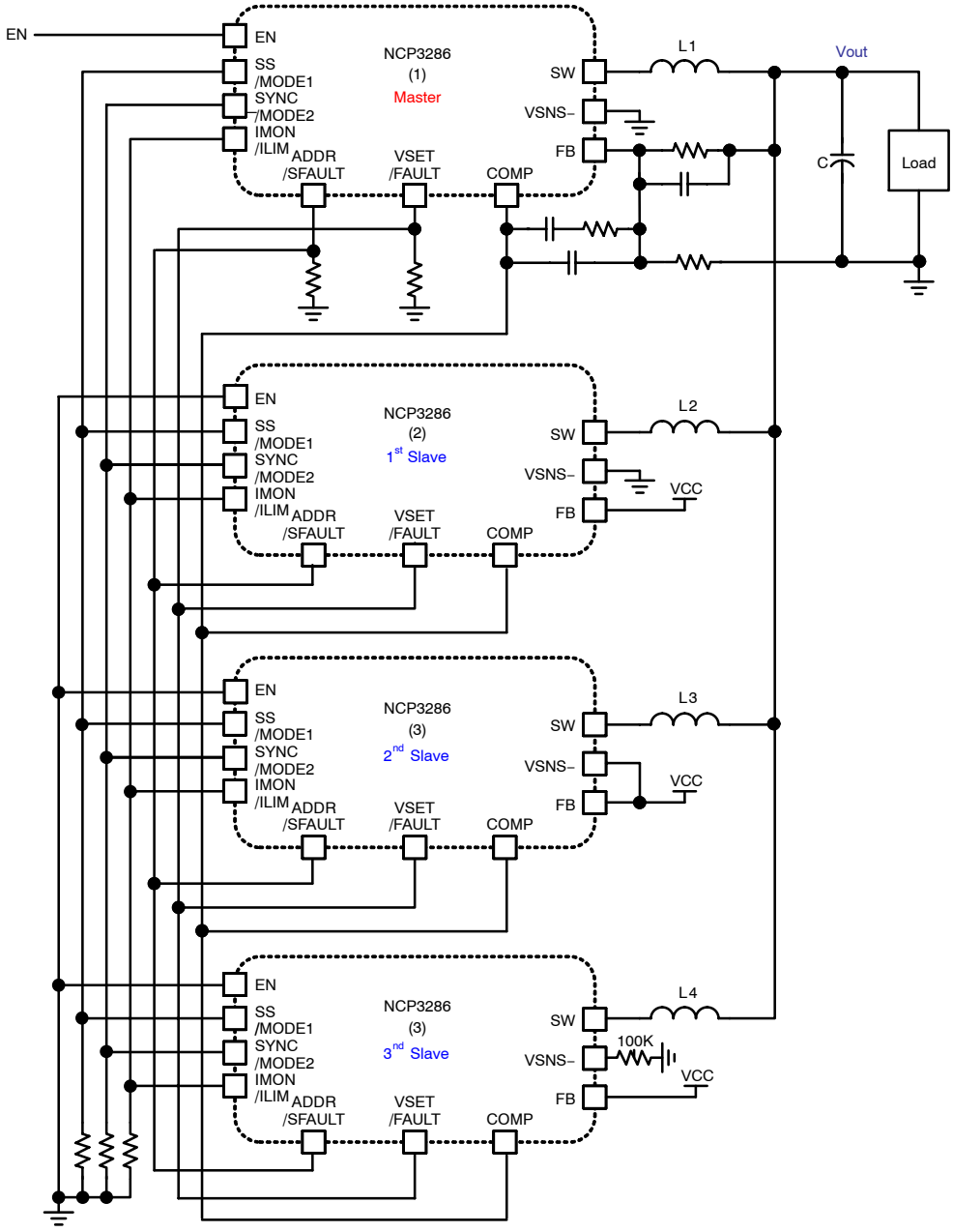


Figure 5. Typical 160 A Application Circuit with 4 Parallel NCP3286

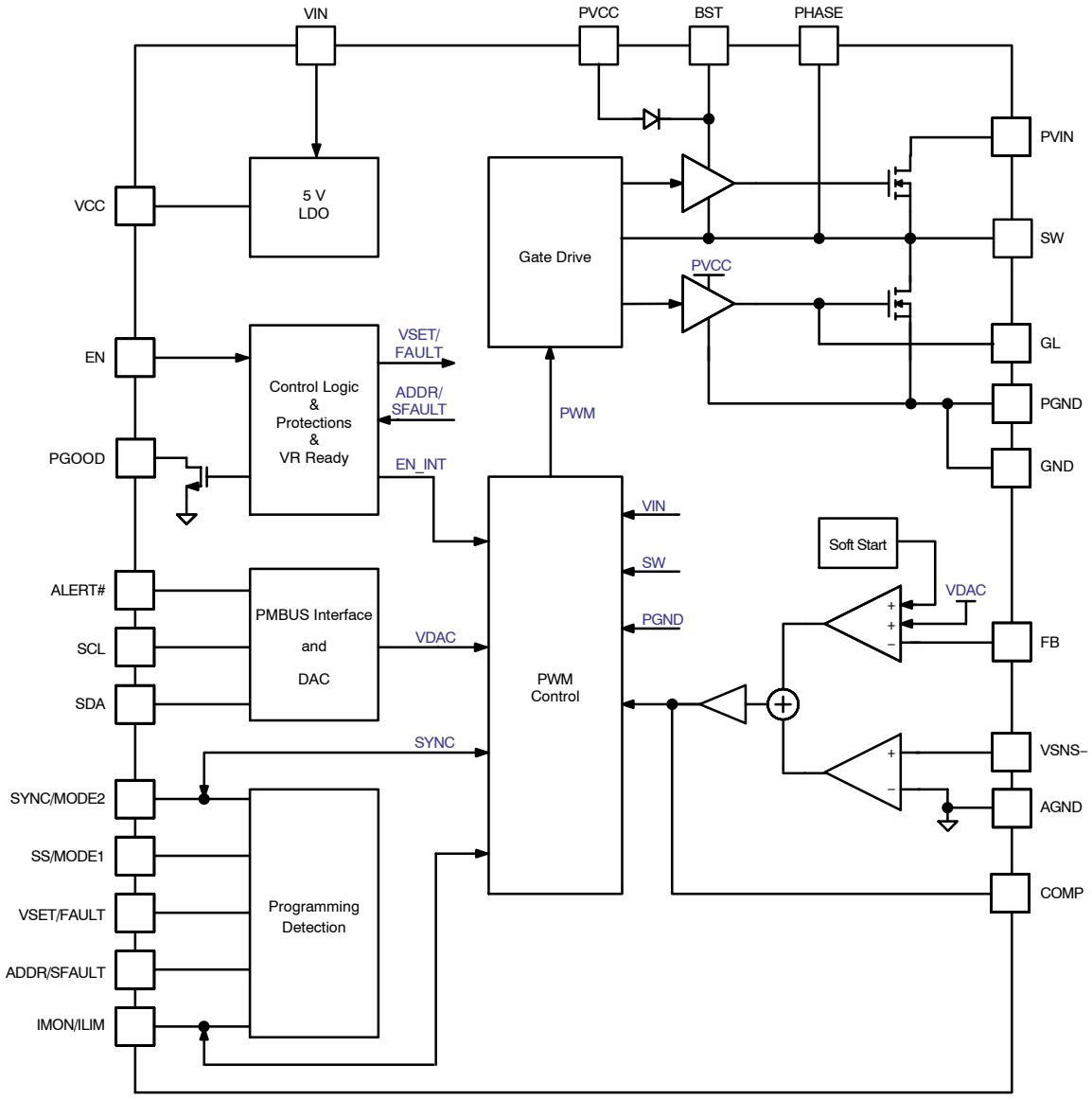


Figure 6. Functional Block Diagram

PIN CONNECTIONS

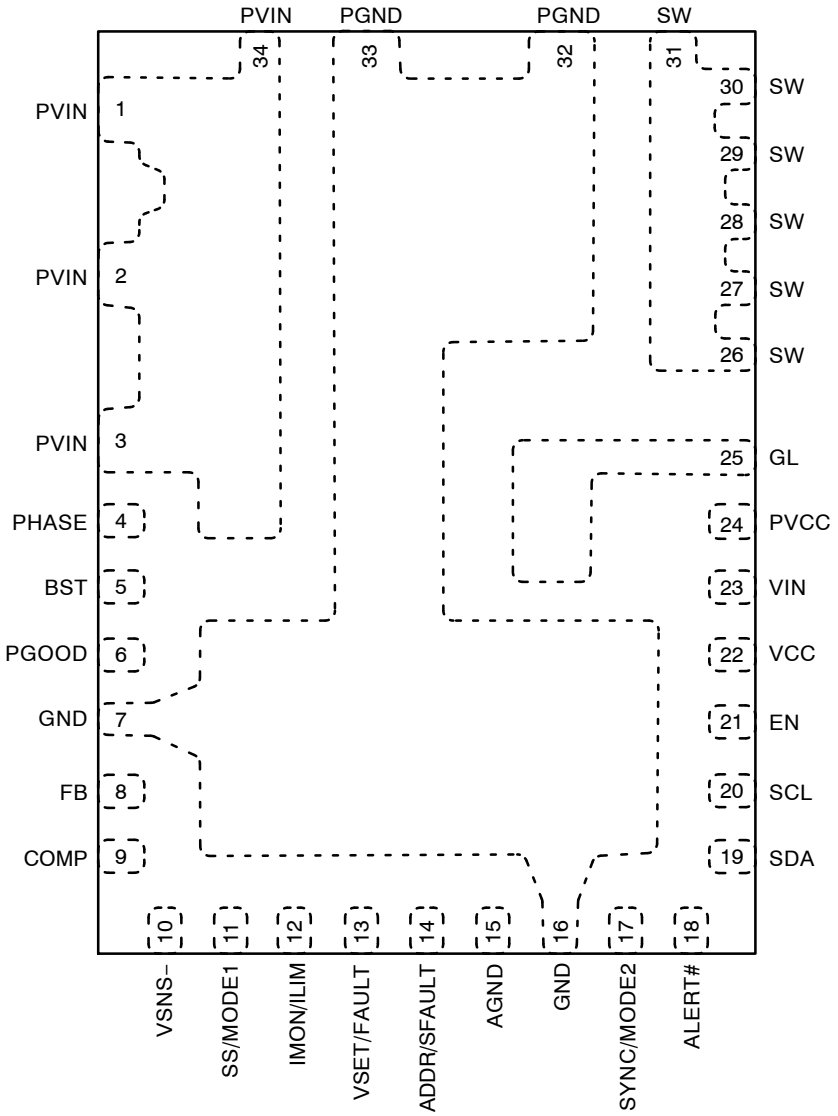


Figure 7. Pin Assignment, Top Transparent View (5 x 7 mm, 0.5 mm Pitch)

PIN DESCRIPTION

Pin	Name	Type	Description
1~3, 34	PVIN	Power	**Power Supply Input**. Power supply input pins of the device, which are connected to the drain of internal high−side power MOSFET. Bypass directly to PGND with ≥22 μF ceramic capacitors using the lowest impedance possible connections to the IC pins.
4	PHASE	Power	**Phase Node**. Provides a return path for integrated high−side gate driver, which is internally connected to the source of the high−side MOSFET.
5	BST	Power	**Bootstrap**. Provides bootstrap voltage for high−side gate driver. A 0.22 μF, 25 V ceramic capacitor is required from this pin to PHASE. A resistor (R_{BST}) in series with capacitor (C_{BST}) is also recommended.
6	PGOOD	Logic Output	**Power GOOD**. Open−drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in the regulation window.
7, 16, 32~33	GND PGND	Power Ground	**Power Ground**. Power supply ground pins of the device, which are connected to the source of the internal low−side power MOSFET. Must be connected to the system ground using lowest possible impedance path.
8	FB	Analog Input	**Feedback**. Inverting input to error amplifier. Also used to program the slave phase number.
9	COMP	Analog Output	**Compensation**. Output of error amplifier.
10	VSNS−	Analog Input	**Voltage Sense Negative Input**. Connect this pin to remote voltage negative sense point. Also used to program the slave phase number.
11	SS / MODE1	Analog Input	**Soft Start and Mode 1**. A 1% resistor between this pin and ground sets default soft start time, operation mode, and VOUT_SCALE_LOOP.
12	IMON / ILIM	Analog I/O	**IMON and Current Limit**. IMON voltage output/input pin. A 1% resistor between this pin and ground programs the per−phase valley current limit and protection mode.
13	VSET / FAULT	Analog I/O	**Boot−Up Voltage and FAULT**. A resistor from this pin to ground programs the boot−up voltage. Output pin of fault signal from master.
14	ADDR / SFAULT	Analog I/O	**PMBUS Address and SFAULT**. A resistor from this pin to ground programs the PMBUS address. Output pin of fault signal from slave.
15	AGND	Analog Ground	**Analog Ground**. Ground of controller. Must be connected to the system ground using a low impedance single−point connection to GND/PGND.
17	SYNC / MODE2	Analog I/O	**Synchronization Clock and Mode 2**. Synchronization clock output from master. A resistor between this pin and ground programs frequency and phase number.
18	ALERT#	Logic Output	**ALERT#**. Open−drain output. A logic low alert signal of the PMBUS interface.
19	SDA	Logic I/O	**PMBUS Data IO Port**. Data port of PMBUS interface.
20	SCL	Logic Input	**PMBUS Serial Clock**. Clock input of PMBUS interface.
21	EN	Logic Input	**Enable**. High enables the controller. Input supply UVLO can be programmed at this pin with external resistor divider.
22	VCC	Power	**Output of LDO and Supply Voltage Input of Controller**. Output of LDO and bias supply input of controller. A 2.2 μF or larger ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to the pin.
23	VIN	Power	**Power Supply Input of LDO**. Power supply input of LDO. Use 1.0 μF or more ceramic bypass capacitor to power ground. The capacitors should be placed as close as possible to this pin. For applications using an external VCC source, connect this pin to VCC and the 5 V source.
24	PVCC	Power	**Supply Voltage Input of Gate Drivers**. A 4.7 μF, 25 V or larger ceramic capacitor bypasses this input to PGND. This capacitor should be placed as close as possible to this pin.
25	GL	Analog Output	**Gate of Low−Side MOSFET**. Directly connected with the gate of the low−side power MOSFET. No external connection is necessary.
26~31	SW	Power	**Switch Node**. Connect to the external inductor. These pins are interconnection between internal high−side MOSFET and low−side MOSFET.

MAXIMUM RATINGS (All voltages with respect to GND/PGND, unless otherwise specified.)

Rating (Note 1)		Symbol	Min	Max	Unit
Input Voltage		V_{VIN}, V_{PVIN}	−0.3	22	V
Driver Supply Voltage		V_{PVCC}	−0.3	6.5	V
Analog Supply Voltage to AGND		V_{VCC}	−0.3	6.5	V
SW, PHASE Voltage		V_{SW}, V_{PHASE}	−0.5, −5 (<10 ns)	25, 28 (<10 ns)	V
BST Voltage		V_{BST}	−0.3	30	V
BST to SW/PHASE Voltage		V_{BST-SW}	−0.3	6.5	V
GL Voltage		V_{GL}	−0.3, −2 (<50 ns)	V_{PVCC} + 0.3	V
VSNS− to AGND	Normal Dynamic Operation Range	V_{SNS-}	−0.2	0.2	V
	During Slave Configuration at Start−up		−0.2	V_{VCC} + 0.3	
SCL, SDA, PGOOD, ALERT# Pins			−0.3	6.5	V
Other Pins			−0.3	V_{VCC} + 0.3	V
GND/PGND to AGND (Note 2)		V_{AGND}	−0.3	0.3	V
Operating Junction Temperature		T_J	−40	150	°C
Storage Temperature		TSTG	−55	150	°C
Lead Temperature Soldering Reflow (Note 3)		T_{SLD}	260		°C
ESD, Human Body Model per ANSI/ESDA/JEDEC JS−001		ESD_{HBM}	2	−	kV
ESD, Charge Device Model per ANSI/ESDA/JEDEC JS−002		ESD_{CDM}	1.5	−	kV
Maximum Latch−up Current Rating, 150°C, per JEDEC JESD78		ILU	−100	100	mA
Moisture Sensitivity Level per IPC/JEDEC Standard: J−STD−020A		MSL	1		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. GND and PGND are internally connected. AGND requires PCB connection to GND.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Air (Note 4)	$R_{\theta JA}$	14.6	°C/W
Thermal Resistance, MOSFET Junction−to−PCB	$R_{\theta JB}$	1.5	°C/W

4. Values are based upon **onsemi** Evaluation Board of 2 oz. copper thickness and FR4 PCB substrate.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 5)	V_{VIN}, V_{PVIN}	3	18	V
Output Voltage	V_{OUT}	0.25	5.5	V
Output Current, Continuous	I_{OUT}	0	40	A
SW Voltage, Peak (Note 6)	$V_{SW\ pk}$	−	22	V
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Operation at <4.5V_{IN} requires external 5 V supply be applied to the VIN and VCC pins per Figure 2.
6. Operation above $V_{SW\ pk}$ may result in reduced IMON accuracy ($V_{IMON\ ACY}$).

ELECTRICAL CHARACTERISTICS (VIN = PVIN = 12 V, VOUT = 1.0 V, F_{SW} = 500 kHz, circuit of Figure 1. Typical values: $T_A = T_J$ = 25°C, min/max: −40°C ≤ T_J ≤ 150°C, unless otherwise specified.)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY CURRENT						
Input Shutdown Current	EN = 0, VIN = PVIN, LDO Enabled	I_{PVIN_SD}	–	7	9	mA
	EN = 0, LDO Disabled, VCC = 5.2 V			375	480	μA
Input Quiescent Current	12 V_{IN}, VIN = PVIN, no switching	I_{PVIN_Q}	–	10	17	mA
	18 V_{IN}, VIN = PVIN, no switching		–	10	17	
INTERNAL LINEAR REGULATOR						
LDO Output Voltage	6 V ≤ V_{VIN} ≤ 18 V, EN = 0, I_{VCC} = 0 – 50 mA external	V_{CC}	4.8	5.0	5.3	V
LDO Drop−Out Voltage	V_{VIN} = 5 V, EN = 0, I_{VCC} = 50 mA external	V_{DO}	–	–	250	mV
LDO Current Limit	V_{VIN} = 5.4 V, EN = 0	I_{CC_MAX}	95	–	–	mA
VCC UVLO Threshold	V_{VCC} rising	V_{CC_OK}	–	4.4	4.5	V
	V_{VCC} falling	V_{CC_UV}	4.0	4.2	–	
	Hysteresis	V_{CC_HYS}	–	200	–	mV
ENABLE						
EN On Threshold	EN rising	V_{EN_TH}	1.08	1.20	1.32	V
Hysteresis Resistance		R_{HYS}	–	40	–	kΩ
Hysteresis Current		I_{EN_HYS}	–	5.2	–	μA
EN Input Leakage Current	EN = 1 V	I_{EN_LKG}	–	–	0.5	μA
DEFAULT PROGRAMMING /DETECTION						
Source Current from Pin	SS/MODE1 pin	I_{SS}	9.7	10	10.3	μA
	IMON/ILIM pin	I_{ILIM}	9.7	10	10.3	
	VSET/FAULT pin	I_{VSET}	9.7	10	10.3	
	ADDR/SFAULT pin	I_{ADDR}	9.7	10	10.3	
	SYNC/MODE2 pin	I_{FSW}	9.7	10	10.3	
PWM MODULATOR						
Minimum On−Time (Note 7)		T_{ON_MIN}	–	35	55	ns
Minimum Off−Time (Note 7)		T_{OFF_MIN}	–	275	300	ns
VOLTAGE ERROR AMPLIFIER						
Open Loop DC Gain (Note 7)		AV_{EA}	–	80	–	dB
Unity Gain Bandwidth (Note 7)		GBW_{EA}	–	12	–	MHz
Slew Rate (Note 7)		SR_{COMP}	–	15	–	V/μs
Output Source/Sink Current	V_{COMP} = 1.2 V	I_{COMP}	10	20	–	mA
COMP Voltage Swing	$I_{COMP(SOURCE)}$ = 2 mA	V_{COMP_H}	3.1	3.4	–	V
	$I_{COMP(SINK)}$ = 2 mA	V_{COMP_L}	–	0.55	0.78	V
FB Bias Current	V_{FB} = 1.00 V	I_{FB}	−150	–	150	nA
CURRENT SENSE AMPLIFIER						
Closed Loop DC Gain		AV_{CA}	–	−10	–	mV/A
−3dB Gain Bandwidth (Note 7)		BW_{CA}	–	7	–	MHz
REFERENCE VOLTAGE						
Reference Voltage (Note 7)	Programmable Range	V_{FB}	0.25	–	1.99	V
	Resolution		–	3.90625	–	mV
	Default Value		Determined by $R_{VSET/FAULT}$			V

ELECTRICAL CHARACTERISTICS (VIN = PVIN = 12 V, VOUT = 1.0 V, F_{SW} = 500 kHz, circuit of Figure 1. Typical values: $T_A = T_J$ = 25°C, min/max: −40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (continued)

Parameter	Conditions		Symbol	Min	Typ	Max	Unit
REFERENCE VOLTAGE							
Reference Voltage Accuracy	0°C ≤ T_J ≤ 125°C	R_{VSET} = 10.0 kΩ	V_{FB_ACCY}	494	500	506	mV
		R_{VSET} = 82.5 kΩ		994	1000	1006	
		R_{VSET} = 221 kΩ		1243	1250	1257	
	−40°C ≤ T_J ≤ 150°C	R_{VSET} = 10.0 kΩ		492	500	508	
		R_{VSET} = 82.5 kΩ		992	1000	1008	
		R_{VSET} = 221 kΩ		1241	1250	1259	
CYCLE−BY−CYCLE CURRENT LIMIT							
Valley Current Limit (Note 7)	Programmable Threshold Range		I_{VLY}	8	–	70	A
	Resolution			–	2	–	
	Default Setting			Determined by $R_{IMON/ILIM}$			
	Accuracy, I_{VLY} ≥ 20 A, 0°C < T_J < 125°C			−5	–	10	%
	Accuracy, I_{VLY} ≥ 20 A, −40°C < T_J < 150°C			−10	–	15	
Over−Current Protection De−Bounce Time (Note 7)	Consecutive cycles before fault state entry		T_{D_VLY}	–	32 / F_{SW}	–	s
Negative Current Limit Threshold (Note 7)	Low−Side FET		I_{LIM_NEG}	–	45	–	A
AVERAGE OUTPUT CURRENT							
Output Current Warn Limit	Programmable Threshold Range		I_{LIM}	0	–	64	A
	Resolution			–	125	–	mA
	Default Setting			Determined by $R_{IMON/ILIM}$, less 4 A (I_{VLY} − 4)			A
	Accuracy, I_{VLY} ≥ 20 A, −40°C < T_J < 150°C			−10	–	15	%
SWITCHING FREQUENCY							
Switching Frequency, 1 Phase	Programmable Range		F_{SW}	200	–	2000	kHz
	Resolution	200 ≤ F_{SW} < 400 kHz		–	50	–	
		400 ≤ F_{SW} < 1,000 kHz		–	100	–	
		1,000 ≤ F_{SW} ≤ 2,000 kHz		–	200	–	
	Default Setting			Determined by $R_{SYNC/MODE2}$			
	Accuracy			−10	–	10	%
SYNCHRONIZATION (SYNC/MODE2 PIN)							
Logic High Output Voltage, Master	I_{SYNC} = 4 mA (sourcing)		V_{OH_SYNC}	VCC − 0.3	–	–	V
Logic Low Output Voltage, Master	I_{SYNC} = −4 mA (sinking)		V_{OL_SYNC}		–	0.3	V
Logic High Input Voltage, Slave			V_{IH_SYNC}	VCC − 1.0	–	–	V
Logic Low Input Voltage, Slave			V_{IL_SYNC}	–	–	1.0	V
Hysteresis (Slave)				–	1.3	–	V
Input Current Bias, Slave			I_{IN_SYNC}	−0.5	–	0.5	μA
Input Capacitance, Slave (Note 7)				–	5.0	–	pF
MASTER/SLAVE FAULTS (FAULT, SFAULT PINS)							
Tri−State Voltage	I_{FAULT} = I_{SFAULT} = 0		V_{FLT_3ST}	1.7	2.0	2.3	V
Tri−State Source Current	V_{FAULT} = V_{SFAULT} = 1.6 V		I_{3ST_UP}	230	300	370	μA
Tri−State Sink Current	V_{FAULT} = V_{SFAULT} = 2.4 V		I_{3ST_DN}	80	100	120	μA
Output Pull−Up Impedance	I_{FAULT} = I_{SFAULT} = 2 mA (sourcing)		R_{FLT_HI}	25	36	60	Ω
Output Pull−Down Impedance	I_{FAULT} = I_{SFAULT} = −2 mA (sinking)		R_{FLT_LO}	240	270	290	Ω

ELECTRICAL CHARACTERISTICS (VIN = PVIN = 12 V, VOUT = 1.0 V, F_{SW} = 500 kHz, circuit of Figure 1. Typical values: $T_A = T_J = 25°C$, min/max: $-40°C \le T_J \le 150°C$, unless otherwise specified.) (continued)

Parameter	Conditions		Symbol	Min	Typ	Max	Unit
MASTER/SLAVE FAULTS (FAULT, SFAULT PINS)							
Input Logic Low Threshold			V_{FLT_IL}	–	–	0.4	V
Input Logic High Threshold			V_{FLT_IH}	VCC – 1.5	–	–	V
SOFT START							
Soft Start Delay Time	Programmable Range		T_{ON_DLY}	1	–	10	ms
	Resolution			–	1	–	
	Default Setting			–	1	–	
	Accuracy			–0.8	–	1.4	
Soft Start Time (0–V_{FB})	Programmable Range		T_{SS}	1	–	20	ms
	Resolution			–	1	–	
	Default Setting			Determined by $R_{SS/MODE1}$			
	Accuracy	Valid R_{VSET} values ≥ 1.00 V_{OUT}		–20	–	20	%
		Valid R_{VSET} values < 1.00 V_{OUT}		–25	–	25	
DISABLE / SHUTDOWN							
Shutdown Delay Time	Programmable Range		T_{OFF_DLY}	0	–	10	ms
	Resolution			–	1	–	
	Default Setting			–	0	–	
	Accuracy			–0.8	–	1.4	
Output Fall Time, (V_{FB}–0)	Programmable Range		T_{OFF}	1	–	20	ms
	Resolution			–	1	–	
	Default Setting			–	5	–	
	Accuracy (for valid $R_{VSET/FAULT}$ values)			–20	–	20	%
Output Discharge Load	SW to GND		R_{SW_D}	–	5	–	kΩ
INPUT VOLTAGE PROTECTION							
Input Over–Voltage Protection, Rising	Programmable Threshold Range		V_{PVIN_OVP}	5	–	20	V
	Resolution			–	1	–	
	Default Setting			–	18	–	
	Accuracy			–5	–	5	%
	Hysteresis			–	200	–	mV
	De–Bounce Time		T_{D_PVOVP}	–	1	–	μs
Input UVLO Threshold, Rising	Programmable Threshold Range		V_{PVIN_ON}	3	–	10.5	V
	Resolution			–	0.5	–	
	Default Setting			–	6.0	–	
	Accuracy			–6	–	5	%
Input UVLO Threshold, Falling	Programmable Threshold Range		V_{PVIN_OFF}	2.5	–	10	V
	Resolution			–	0.5	–	
	Default Setting			–	5.5	–	
	Accuracy			–6	–	5	%

ELECTRICAL CHARACTERISTICS (VIN = PVIN = 12 V, VOUT = 1.0 V, F_{SW} = 500 kHz, circuit of Figure 1. Typical values: $T_A = T_J = 25°C$, min/max: $-40°C \le T_J \le 150°C$, unless otherwise specified.) (continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
OUTPUT VOLTAGE PROTECTION						
Output Over−Voltage Fault Threshold (FB to VSNS−, Rising FB)	Programmable Threshold Range	V_{OVP_TH}	105	−	135	% V_{FB}
	Resolution		−	2	−	
	Default Setting		−	121	−	
	Accuracy		−2	−	2	
	Hysteresis		−	25	−	mV
	De−Bounce Time	T_{D_OVP}	−	1	−	μs
Output Over−Voltage Warn Limit (FB to VSNS−, Rising FB)	Programmable Threshold Range	V_{OVW_TH}	103	−	118	% V_{FB}
	Resolution		−	1	−	
	Default Setting		−	108	−	
	Accuracy		−2	−	2	
Output Under−Voltage Fault Threshold (FB to VSNS−, Falling FB)	Programmable Threshold Range	V_{UVP_TH}	20	−	95	% V_{FB}
	Resolution		−	5	−	
	Default Setting		−	20	−	
	Accuracy		−3.5	−	2	
	Hysteresis		−	1	−	
	De−Bounce Time	T_{D_UVP}	−	1	−	μs
Output Under−Voltage Warn Limit (FB to VSNS−, Falling FB)	Programmable Threshold Range	V_{UVW_TH}	82	−	97	% V_{FB}
	Resolution		−	1	−	
	Default Setting		−	90	−	
	Accuracy		−3.5	−	2	
Absolute Over−Voltage Threshold during Soft Start (FB to VSNS−)	Threshold, rising	V_{OV_A}	2.02	2.20	2.38	V
	Hysteresis	V_{OV_HYS}	−	25	−	mV
THERMAL PROTECTION						
Over−Temperature Fault Limit (Note 7)	Programmable Threshold Range	T_{OT_F}	80	−	160	°C
	Resolution		−	0.5	−	
	Default Setting		−	150	−	
Over−Temperature Warn Limit (Note 7)	Programmable Threshold Range	T_{OT_W}	70	−	150	°C
	Resolution		−	0.5	−	
	Default Setting		−	130	−	
Thermal Shutdown Threshold (Note 7)	T_J rising	T_{SD}	160	170	−	°C
Restart Temperature Threshold (Note 7)	T_J falling	T_{RST}	−	155	−	°C
IMON						
Output Offset Voltage	I_{OUT} = 0 A	V_{IMON_0}	−	1.00	−	V
Output Voltage Gain	$V_{IMON} = [1.00 + (0.015625 * I_{OUT})]$ V	V_{IMON_I}	−	15.625	−	mV/A
Output Accuracy (Note 7)	I_{OUT} = 40 A	V_{IMON_ACY}	−	±6	−	%
	I_{OUT} = 25 A		−	±8	−	
	I_{OUT} = 10 A		−	±12	−	
CURRENT SHARING						
Current Sense Offset	Programmable Threshold Range	I_{IDC0}	−2.000	−	2.000	A
	Resolution		−	125	−	mA
	Default Setting		−	0	−	A

ELECTRICAL CHARACTERISTICS (VIN = PVIN = 12 V, VOUT = 1.0 V, F_{SW} = 500 kHz, circuit of Figure 1. Typical values: $T_A = T_J = 25°C$, min/max: $-40°C \le T_J \le 150°C$, unless otherwise specified.) (continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
CURRENT SHARING						
Current Balance Offset	Programmable Threshold Range	I_{ICB0}	−3.875	–	3.875	A
	Resolution		–	125	–	mA
	Default Setting		–	0	–	A
POWER GOOD (as a percentage of V_{OUT})						
PGOOD Assertion (V_{OUT} Rising)	Programmable Threshold Range	V_{PG_ON}	84	–	98	$\%V_{FB}$
	Resolution		–	2	–	
	Default Setting		–	90	–	
	Accuracy		−2	–	2	
PGOOD Leakage Current	V_{PGOOD} = 5 V	I_{IOH_PG}	–	–	1.0	μA
PGOOD Startup Delay	From end of soft−start (V_{OUT} ramping) until PGOOD asserts	T_{DH_PD}	–	560	720	μs
PGOOD De−Assert (V_{OUT} Falling)	Programmable Threshold Range	V_{PG_OFF}	82	–	96	$\%V_{FB}$
	Resolution		–	2	–	
	Default Setting		–	84	–	
	Accuracy		−2	–	2	
PGOOD Low Voltage	I_{PGOOD} = −4 mA (sinking)	V_{OL_PG}	–	–	0.3	V
PGOOD Shutdown Delay	Falling EN or V_{FB} < POWER_GOOD_OFF until PGOOD de−asserts	T_{DL_PD}	–	2	5	μs
ALERT#						
Leakage Current	ALERT# = 3.3 V	I_{ALT_HI}	–	–	1	μA
Output Low	I_{ALERT} = 20 mA (sinking)	V_{ALT_LO}	–	–	0.3	V
AUTO RESTART						
Automatic−Restart (Hiccup) Delay Time	Programmable Range	T_{HCP}	32	–	256	ms
	Resolution		–	32	–	
	Default Setting		–	32	–	
	Accuracy		−15	–	20	%
TELEMETRY						
Telemetry Refresh Interval	Round Robin (5 channels)	T_{TLMR}	–	100	–	μs
Input Voltage Reporting	Range	V_{PVIN_MON}	0	–	32	V
	Resolution		–	31.25	–	mV
	Accuracy		−5	–	5	%
Output Voltage Reporting, Master Only	Range	V_{VFB_MON}	0	–	5.5	V
	Resolution		–	3.90625	–	mV
	Accuracy (FB to VSNS−) 250 mV ≤ V_{OUT} < 400 mV		−7	–	7	%
	Accuracy (FB to VSNS−) 400 mV ≤ V_{OUT} < 600 mV		−4	–	4	
	Accuracy (FB to VSNS−) 600 mV ≤ V_{OUT} < 900 mV		−3	–	3	
	Accuracy (FB to VSNS−) 900 mV ≤ V_{OUT} < 2.0 V		−2	–	2	
Output Current Reporting	Range	I_{OUT_MON}	−64	–	64	A
	Resolution (1 LSB)		–	125	–	mA
	Accuracy, relative to V_{IMON}		−4	±2	4	LSB
Internal Temperature Reporting (Note 7)	Range	I_{TJ_MON}	−256	–	256	°C
	Resolution		–	0.5	–	
	Accuracy		−6	–	6	

ELECTRICAL CHARACTERISTICS (VIN = PVIN = 12 V, VOUT = 1.0 V, F_{SW} = 500 kHz, circuit of Figure 1. Typical values: $T_A = T_J = 25°C$, min/max: $-40°C \le T_J \le 150°C$, unless otherwise specified.) (continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
POWER STAGE						
High−Side MOSFET On Resistance	$V_{BST} - V_{PHASE}$ = 5 V	R_{DS_HI}	–	1.8	–	mΩ
Low−Side MOSFET On Resistance	V_{PVCC} = 5 V	R_{DS_LO}	–	0.8	–	mΩ
High−Gate Pull−Up Resistance (Note 7)	$V_{BST} - V_{PHASE}$ = 5 V, I_{HG} = 2 mA (source)	R_{HG_UP}	–	1.5	–	Ω
High−Gate Pull−Down Resistance (Note 7)	$V_{BST} - V_{PHASE}$ = 5 V, I_{HG} = 2 mA (sink)	R_{HG_DN}	–	0.6	–	Ω
Leading Edge Dead Time (Note 7)	SW/PHASE rising, $V_{BST} - V_{PHASE}$ = 5 V	T_{SWD_UP}	–	14	–	ns
Low−Gate Pull−Up Resistance (Note 7)	V_{PVCC} = 5 V, I_{LG} = 2 mA (source)	R_{LG_UP}	–	0.8	–	Ω
Low−Gate Pull−Down Resistance (Note 7)	V_{PVCC} = 5 V, I_{LG} = 2mA (sink)	R_{LG_DN}	–	0.4	–	Ω
Trailing Edge Dead Time (Note 7)	SW/PHASE falling, V_{PVCC} = 5 V	T_{SWD_DN}	–	9	–	ns
BST Rectifier On Resistance	V_{PVCC} = 5 V, I_F = 2 mA	R_{BST_ON}	–	50	–	Ω
BST Rectifier Reverse Leakage Current	V_{PVCC} = 5 V, V_{PHASE} = 25 V	R_{BST_LKG}	–	–	3	μA
PMBUS INTERFACE (SCL, SDA PINS)						
PMBUS Operating Frequency Range			10	–	400	kHz
Logic High Input Threshold			1.35	–	–	V
Logic Low Input Threshold			–	–	0.8	V
Logic Input Hysteresis (Note 7)			80	150	–	mV
Logic Input Bias Current			−1	–	1	μA
SDA Logic Output Low	I_{SDA} = 6 mA (sinking)		–	–	0.4	V
Pin Capacitance (Note 7)			–	–	10	pF
Rise / Fall Time (Note 7)			120	–	–	ns
Data Set−Up Time (Note 7)			100	–	–	ns
Data Hold Time (Note 7)	Receive/transmit modes		0	–	–	ns
Clock High Time (Note 7)			0.6	–	50	μs
Clock Low Time (Note 7)			1.3	–	–	μs
Clock Low Timeout Detect (Note 7)			25	–	35	ms
Bus Free Time START to STOP (Note 7)			1.3	–	–	μs
Repeated START Set−Up Time (Note 7)			0.6	–	–	μs
Hold Time after Repeated START (Note 7)			0.6	–	–	μs
Master Extend Time (Note 7)	Cumulative Clock Low		–	–	10	ms
Slave Extend Time (Note 7)	Cumulative Clock Low		–	–	25	ms
Noise Spike Suppression Time (Note 7)			0	–	50	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance over the indicated operating temperature range by design and/or characterization and may not be production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

(RESULTS USE FIGURE 1 CIRCUIT, V_{IN} = 12 V, V_{OUT} = 1.0 V, F_{SW} = 500 KHZ, R_{BST} = 3.3 Ω, T_A = 25°C, UNLESS OTHERWISE SPECIFIED. L AND C_{OUT} VALUES (NOTE 8).)

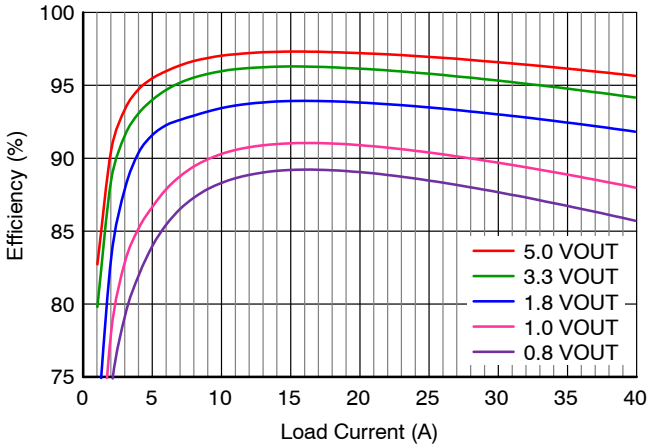


Figure 8. Efficiency vs. Load

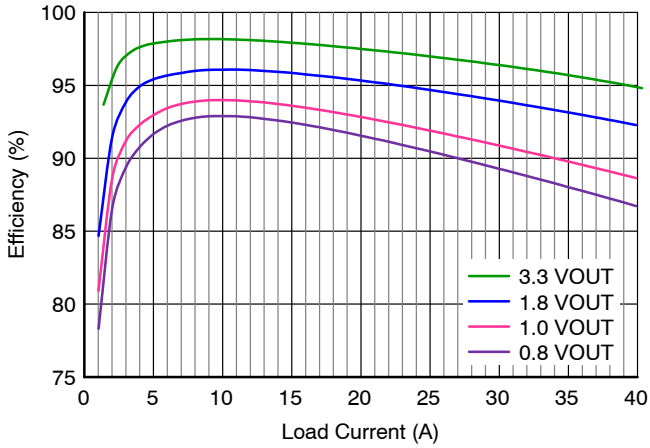


Figure 9. Efficiency vs. Load, 5 V_{IN}, R_{BST} = 0 Ω

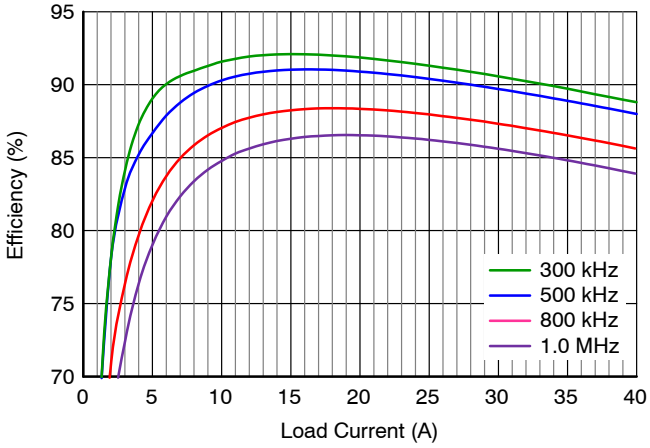


Figure 10. Efficiency vs. Frequency

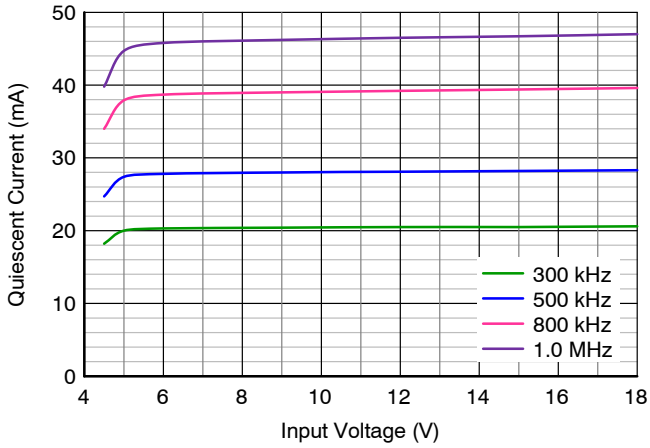


Figure 11. Device Quiescent Current vs. V_{IN} and Frequency

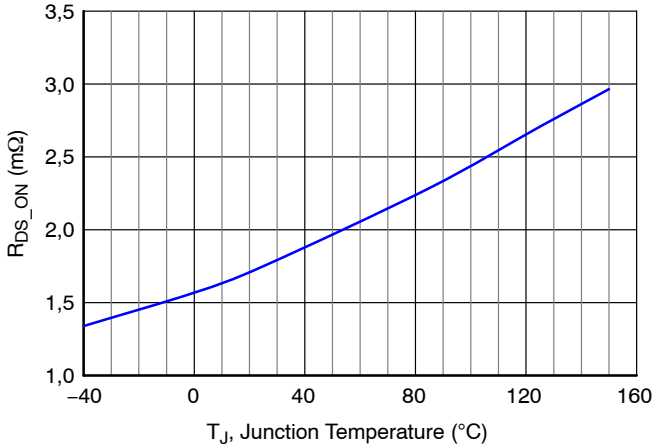


Figure 12. High−Side R_{DS_ON} vs. Temperature, 5 V_{GS}

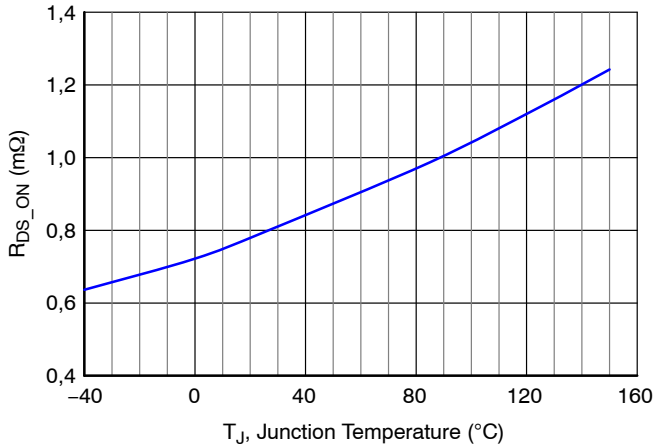


Figure 13. Low−Side R_{DS_ON} vs. Temperature, 5 V_{GS}

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

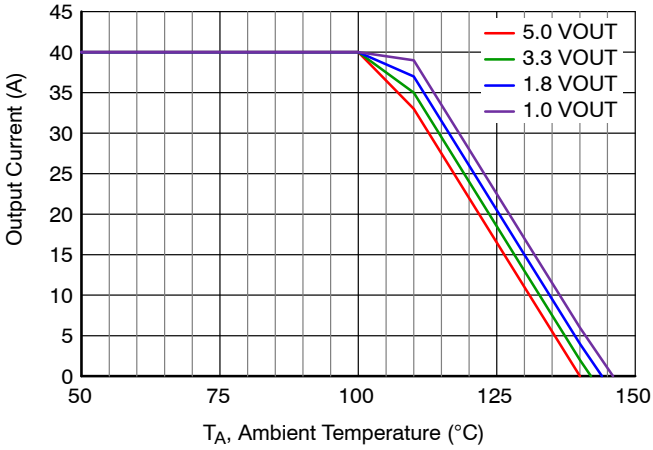


Figure 14. Thermal Safe Operating Area, No Airflow

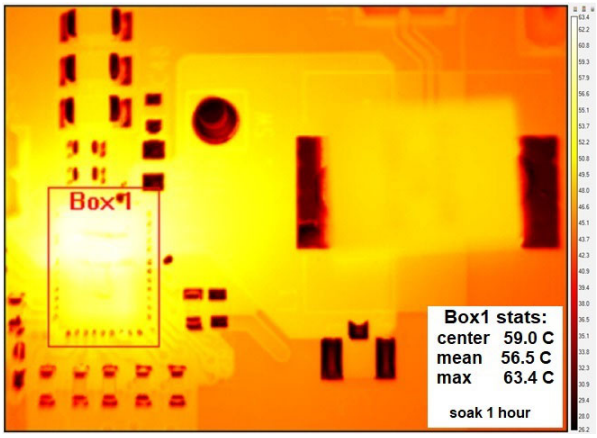


Figure 15. Thermal Image, No Airflow, I_{OUT} = 40 A

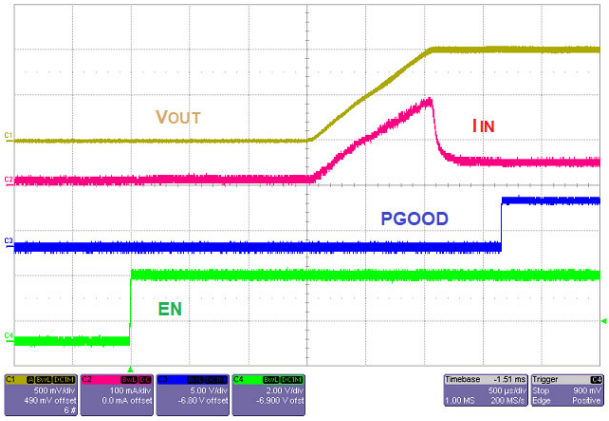


Figure 16. Start−Up, No Load, $R_{SS/MODE1}$ = 10 kΩ

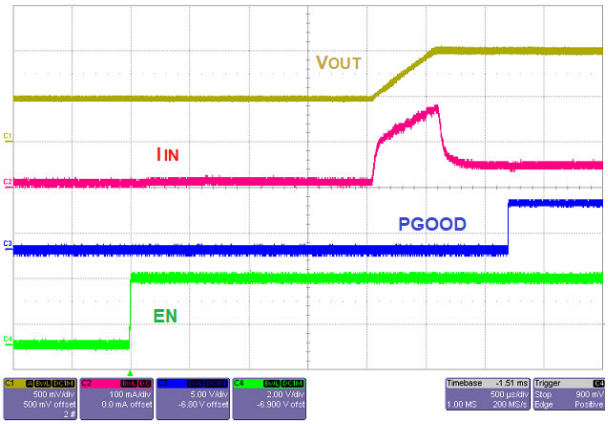


Figure 17. Pre−Bias Start−Up, No Load, $R_{SS/MODE1}$ = 10 kΩ

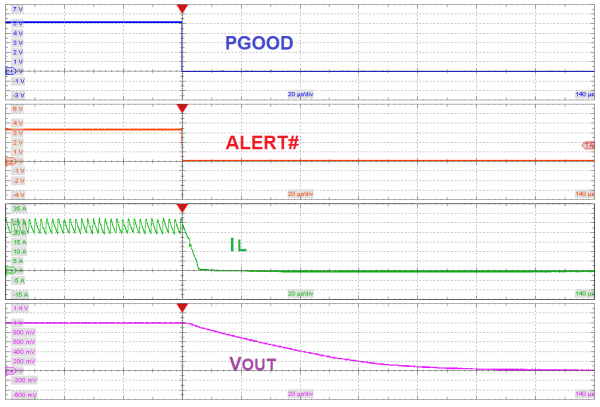


Figure 18. Over−Current Protection Response, Latch−Off, I_{VLY} = 20 A

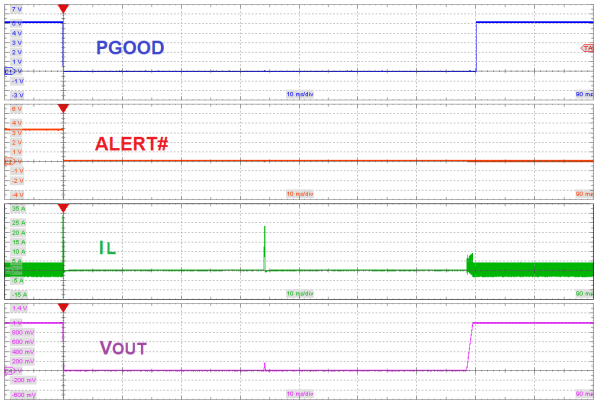


Figure 19. Over−Current Protection Response and Auto−Restart, Hiccup, I_{VLY} = 20 A

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

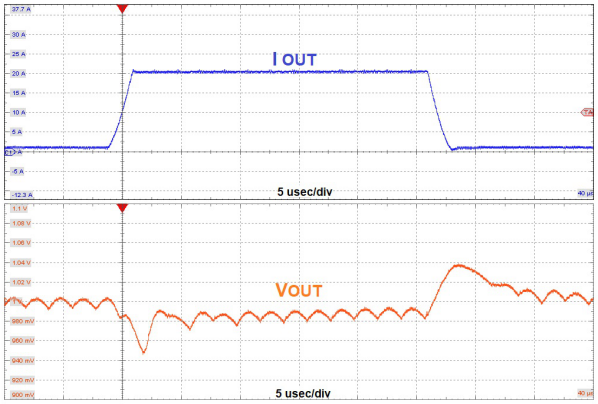


Figure 20. Load Transient Response, 1 – 21 A, 10 A/μs

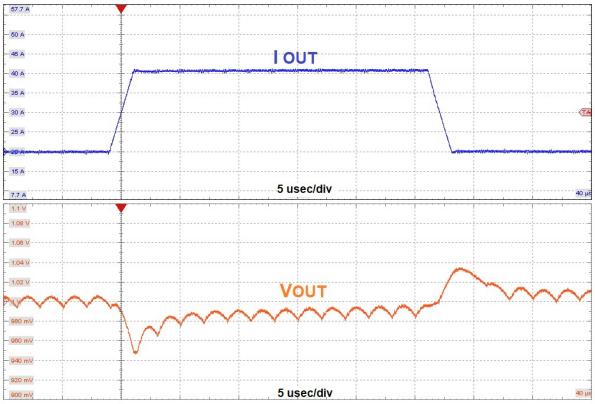


Figure 21. Load Transient Response, 20 – 40 A, 10 A/μs

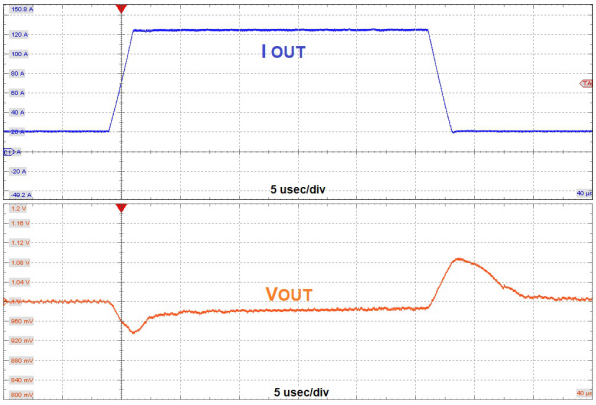


Figure 22. 4−Phase Load Transient Response, 20 – 125 A, 50 A/μs

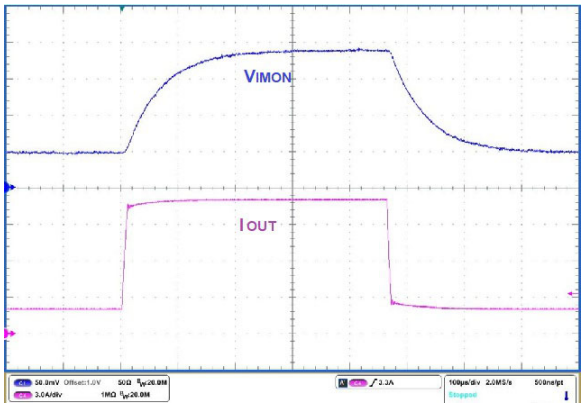


Figure 23. Dynamic IMON Tracking, 3 – 11 A, 1 A/μs

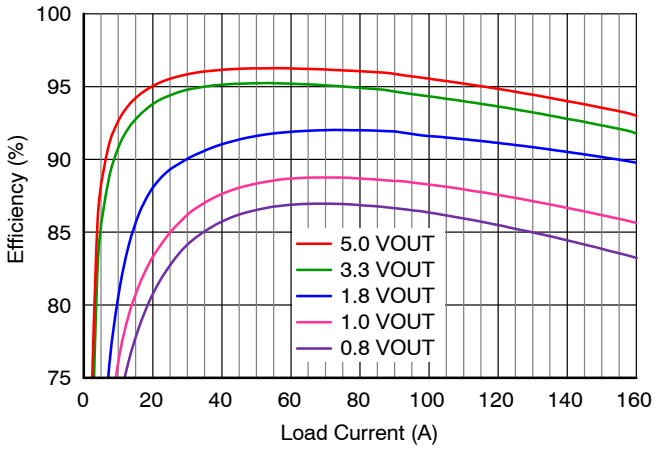


Figure 24. Efficiency vs. Load, 4−Phase

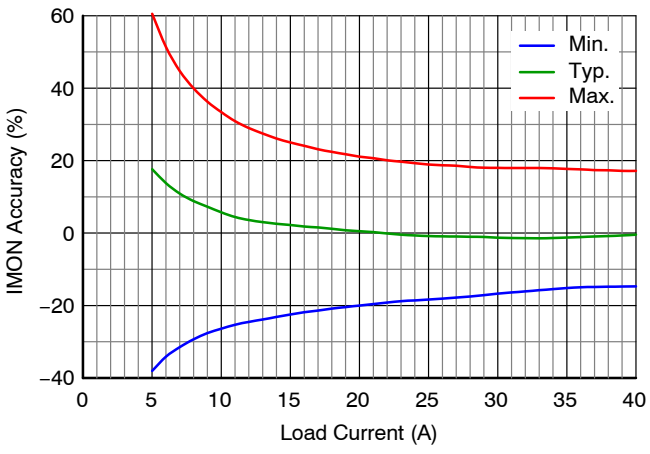


Figure 25. IMON Accuracy vs. Load

NOTE:

8. C_{OUT} used for testing:

Phases	Capacitance
1	20||22 μF ceramic + 2||470 μF poscap
4	20||22 μF ceramic + 6||470 μF poscap

L used:

V_{OUT}	L (nH)	DCR (μΩ)	Supplier
<1.5	210	290	Eaton FP1108R1−R21−R
1.8	330	155	Wurth 744305033
3.3	560	1,400	Wurth 744373770056
5.0	1,000	2,300	Pulse PA4343.102NLT

APPLICATION INFORMATION

General

The NCP3286, a highly efficient stackable synchronous buck regulator with a PMBUS interface, is capable of operating over an input voltage range of 3.0 V to 18 V, supporting load currents up to 40 A. Higher output currents can be achieved by paralleling up to four NCP3286 devices.

The NCP3286 employs a fixed frequency current mode control scheme to provide accurate voltage regulation and fast transient response. Flexible programmability of function and parameters support multiple applications.

Master/Slave Configuration

The NCP3286 can be configured as either a master or slave in an interleaved, multi−phase POL system, by its FB and VSNS− pin configuration, as shown in Table 1.

Table 1. MASTER/SLAVE CONFIGURATION

	FB	VSNS−	Application
Master	V_{OUT}	GND	1, 2, 3, 4 phase
1st Slave	VCC	GND	2, 3, 4 phase
2nd Slave	VCC	VCC	3, 4 phase
3rd Slave	VCC	100 kΩ – GND	4 phase

PMBUS Address Selection

The offset portion of the full PMBUS address is set by connecting a 1% resistor (R_{ADDR}) between the ADDR pin and GND per Table 2.

The base portion of the PMBUS address is manufacturer specific and set by Register C5h.

Table 2. PMBUS ADDRESS SELECTION

R_{ADDR} (kΩ)	PMBUS Address			
	Master	1st Slave	2nd Slave	3rd Slave
10.0	base+00h	base+01h	base+02h	base+03h
15.0	base+01h	base+02h	base+03h	base+04h
18.2	base+02h	base+03h	base+04h	base+05h
22.1	base+03h	base+04h	base+05h	base+06h
27.4	base+04h	base+05h	base+06h	base+07h
33.2	base+05h	base+06h	base+07h	base+08h
39.2	base+06h	base+07h	base+08h	base+09h
47.5	base+07h	base+08h	base+09h	base+0Ah
56.2	base+08h	base+09h	base+0Ah	base+0Bh
68.1	base+09h	base+0Ah	base+0Bh	base+0Ch
82.5	base+0Ah	base+0Bh	base+0Ch	base+0Dh
100	base+0Bh	base+0Ch	base+0Dh	base+0Eh
121	base+0Ch	base+0Dh	base+0Eh	base+0Fh
150	base+0Dh	base+0Eh	base+0Fh	base+10h
182	base+0Eh	base+0Fh	base+10h	base+11h
221	0Fh	0Fh	0Fh	0Fh

If base+offset exceeds 7Fh, fixed slave address 0Fh is used.

V_{OUT} Scale Loop Setting

From the table below, choose the lowest ratio V_{OUT} Scale setting for the desired output voltage (V_{OUT}).

Table 3. V_{OUT} SCALE LOOP SETTING

V_{OUT} Range (V)	V_{OUT} Scale (N)
0.25 – 1.99	1
0.50 – 3.99	$^1/_2$
1.00 – 5.50	$^1/_4$

For instance: 1.2 V_{OUT}, use V_{OUT} Scale = 1.

For V_{OUT} Scale other than 1, a resistor divider of equivalent ratio is required from V_{OUT} to FB to VSNS−.

Using Table 4, select the value (R_{PIN}) for $R_{SS/MODE1}$ corresponding to the required V_{OUT} Scale level and desired soft−start time (T_{SS}).

At initial power−up, or after input power cycling, the following registers automatically load the default levels established by $R_{SS/MODE1}$.

- VOUT_MAX (24h)
- VOUT_SCALE_LOOP (29h)
- VOUT_MIN (2Bh)
- TON_RISE (61h)

The PMBUS may be used to overwrite these values.

V_{BOOT} Setting

Use Table 4 to select the value (R_{PIN}) for $R_{VSET/FAULT}$ corresponding to the target start−up V_{OUT} level (V_{BOOT}) for the already established V_{OUT} Scale setting.

At initial power−up, the VOUT_COMMAND register (21h) will automatically be loaded with the V_{OUT} level established by $R_{VSET/FAULT}$. PMBUS can be used to overwrite this value.

Setting Frequency

Use Table 4 to select the value (R_{PIN}) for $R_{SYNC/MODE2}$ associated with the desired switching frequency per phase and the total number of phases to be implemented.

At initial power−up, the FREQUENCY_SWITCH (33h) and INTERLEAVE (37h) registers will load with the default value according to the selected $R_{SYNC/MODE2}$ value. PMBUS may be used to overwrite the value.

Current Limit Setting

The per phase valley current limit setting (I_{VLY}) and protection mode (hiccup/latch−off) are established by $R_{IMON/ILIM}$, according to the R_{PIN} value shown in Table 4.

At initial power−up, or after input power cycling, the following registers automatically load the default levels established by $R_{IMON/ILIM}$.

- VOUT_OV_FAULT_RESPONSE (41h)
- VOUT_UV_FAULT_RESPONSE (45h)
- IOUT_OC_FAULT_LIMIT (46h)
- IOUT_OC_FAULT_RESPONSE (47h)
- IOUT_OC_WARN_LIMIT (4Ah)

The PMBUS may be used to overwrite these values.

Operation Modes

The device's operating mode can be configured with 1% resistors, which allows start−up, operation, and full protection features without PMBUS instructions, as shown in Table 4.

Table 4. OPERATING MODE SELECTION

	$R_{VSET/FAULT}$ Pin			$R_{IMON/ILIM}$ Pin		$R_{SYNC/MODE2}$ Pin		$R_{SS/MODE1}$ Pin	
	Sets Start−Up V_{OUT} Level (V_{BOOT})			Sets Current Limit (I_{VLY}) per Phase and Protection Mode		Sets Frequency (F_{SW}) per Phase and Phase Count		Sets V_{OUT} Scale and Soft−Start Time (T_{SS})	
R_{PIN} (kΩ)	1 Scale (V)	$^1/_2$ Scale (V)	$^1/_4$ Scale (V)	I_{VLY} (A)	Mode	F_{SW} (kHz)	Phases (N)	T_{SS} (ms)	V_{OUT}−Scale (N)
10.0	0.50	1.30	2.40	14	Hiccup	500	1 phase	1	1
15.0	0.55	1.35	2.50	18		600		3	
18.2	0.60	1.40	2.60	24		700		5	
22.1	0.65	1.45	2.70	30		800		10	
27.4	0.70	1.50	2.80	36		500	2 phase	15	
33.2	0.75	1.55	2.90	42		600		1	$^1/_2$
39.2	0.80	1.60	3.00	50		700		3	
47.5	0.85	1.65	3.10	60		800		5	
56.2	0.90	1.70	3.20	14	Latch−Off	300	3 phase	10	
68.1	0.95	1.75	3.30	18		400		15	
82.5	1.00	1.80	3.40	24		500		1	$^1/_4$
100	1.05	1.90	3.50	30		600		3	
121	1.10	2.00	4.00	36		350	4 phase	5	
150	1.15	2.10	4.50	42		400		10	
182	1.20	2.20	5.00	50		450		15	
221	1.25	2.30	5.50	60		500		20	

The use of resistor values other than shown in the table above is not recommended.

Soft Start

The NCP3286 soft−start function allows starting into a pre−biased output. When the device is enabled, the soft−start ramp time (T_{SS} or TON_RISE) begins after a programmable delay (TON_DELAY).

During the soft−start ramp, switching is prevented when pre−biased V_{FB} exceeds the target reference voltage. At the end of soft−start, if V_{FB} continues to be greater than the programmed reference level, switching will commence to bring the output into compliance.

When the device is disabled, or at falling UVLO, the device shuts down immediately and the power MOSFETs are forced off, by default. Shutdown behavior can be altered via PMBUS using the OPERATION command.

Enable

Depending on ON_OFF_CONFIG (02h) settings, the NCP3286 is enabled when the rising EN voltage (V_{EN_H}) exceeds V_{EN_TH}, as illustrated below:

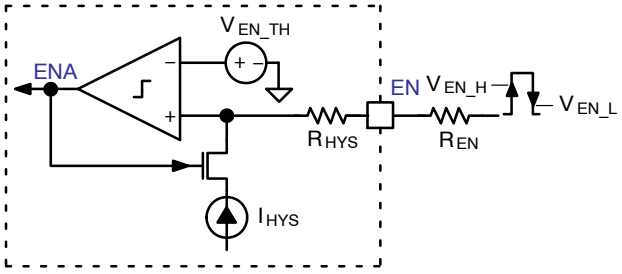


Figure 26. Enable Thresholds and Hysteresis

Optional R_{EN} can be added externally to increase the amount of hysteresis to reach the falling threshold. The falling threshold can be calculated by:

$$V_{EN\_L} = V_{EN\_TH} - I_{HYS} \cdot (R_{HYS} + R_{EN}) \quad \text{(eq. 1)}$$

The EN pin can also be used to implement an input supply UVLO function using the circuit below:

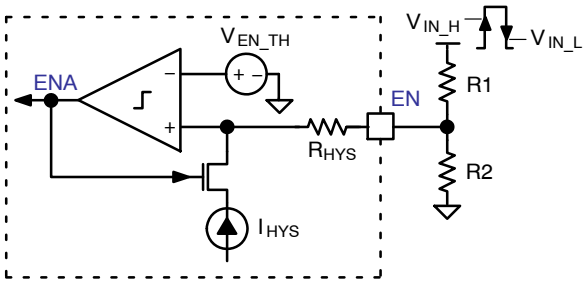


Figure 27. EN Pin Input UVLO Circuit

The associated rising and falling V_{IN} thresholds are:

$$V_{IN\_H} = V_{EN\_TH} \cdot \left(\frac{R1}{R2} + 1\right) \quad \text{(eq. 2)}$$

$$V_{IN\_L} = K + R1 \cdot \left(\frac{K}{R2} - I_{HYS}\right) \quad \text{(eq. 3)}$$

where:

$$K = V_{EN\_TH} - I_{HYS} \cdot R_{HYS} \quad \text{(eq. 4)}$$

To avoid unintended or undefined operation, the EN pin should not be left floating in the application.

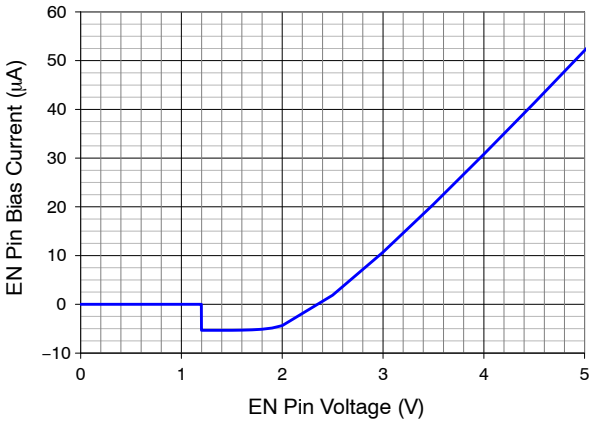


Figure 28. Typical EN Pin Bias Current

Over−Current Protection (OCP)

The NCP3286 employs a cycle−by−cycle valley current limit (I_{VLY}) threshold to protect the regulator. The average current limit (I_{LIM}) value can be calculated from the inductor ripple current and I_{VLY} using:

$$I_{LIM} = I_{VLY} + \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{2 \cdot V_{IN} \cdot L \cdot F_{SW}} \quad \text{(eq. 5)}$$

OCP detection starts at the beginning of the soft−start ramp (T_{SS}) and extends until shutdown. Inductor current is monitored between SW and PGND. If the OCP event lasts for more than 32 consecutive switching cycles, the device enters fault state (hiccup or latch−off). If V_{OUT} is falling rapidly, the device may trip under−voltage protection before the 32 current limit cycles accumulate.

To restart the device from an OCP latch−off condition, the system needs to toggle VCC or EN off, then back on.

Output Under−Voltage Protection (UVP)

UVP detection is active from when PGOOD asserts at the end of soft−start, until shutdown. The NCP3286 will force PGOOD low and turn off both power MOSFETs once the FB pin voltage falls below V_{UVP_TH}, established by the VOUT_UV_FAULT_LIMIT register (44h) setting, for more than T_{D_UVP}.

To restart the device after a UVP latch−off, the system needs to toggle VCC or EN off, and then back on.

Output Over−Voltage Protection (OVP)

The NCP3286 offers output over−voltage protection to protect the regulator and prevent possible destruction of the downstream load. OVP is active from the beginning of soft−start until shutdown, latch−off, or during hiccup idle time.

During operation, if the FB pin voltage exceeds the V_{OVP_TH} threshold set by the VOUT_OV_FAULT_LIMIT register (40h) value, for longer than T_{D_OVP}, OVP is triggered and PGOOD is forced low.

Once OVP triggers, FCCM operation is maintained while the DAC voltage ramps down according to TOFF_FALL (65h), preventing large negative voltage spikes from occurring at the output. Once the DAC reaches 0, the high−side FET is turned off, while the low−side FET remains on.

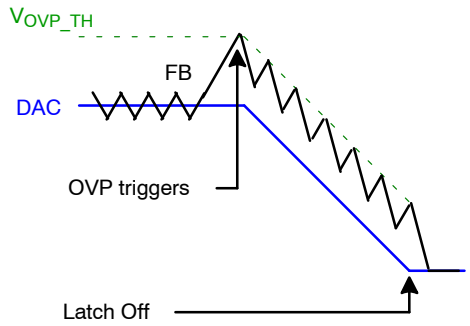


Figure 29. OVP Behavior during Normal Operation

During soft−start, the OVP threshold is set to a fixed absolute value of V_{OV_A}.

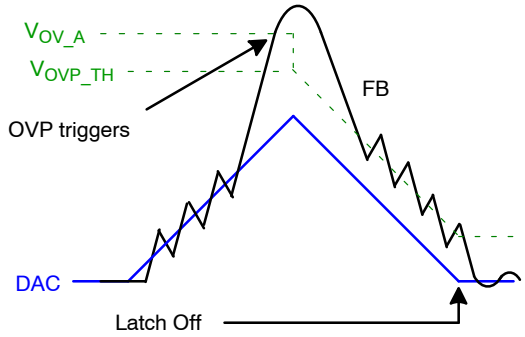


Figure 30. OVP Behavior during Start−Up

To restart the device after an OVP latch−off, the system needs to toggle VCC or EN off, and then back on.

Thermal Shutdown (T_{SD})

Severe overheating is prevented by forcing the entire device into shutdown when die temperature (T_J) reaches the thermal shutdown threshold (T_{SD}). T_{SD} detection activates when VCC and EN are valid. Once the thermal protection is triggered, the entire chip remains off until T_J cools to T_{RST}, where an automatic recovery and soft−start sequence commence.

Hiccup / Latch−Off Mode

The selected resistor value at the IMON/ILIM pin ($R_{IMON/ILIM}$) determines whether hiccup or latch−off protection mode is applied under V_{OUT} OVP, V_{OUT} UVP, or OCP conditions.

To restart a device in latch−off mode, EN or VCC need to be toggled. In hiccup mode, the idle time counter (T_{HCP}) begins counting when the device shuts down for OCP, UVP, or the end of OVP DAC ramp down. A normal start−up sequence automatically occurs once T_{HCP} expires.

PGOOD Pin

The PGOOD signal is held low during soft−start and in shutdown state.

PGOOD is high while V_{FB} remains within the adjustable regulation envelope set by POWER_GOOD_ON (5Eh) and POWER_GOOD_OFF (5Fh).

During thermal shutdown (T_{SD}), PGOOD is low until the device sufficiently cools. PGOOD will be low during all fault conditions, but will remain high during warn conditions.

Multi−Phase Frequency and Synchronization

Per phase switching frequency (F_{SW}) and phase count (N) are programmed by $R_{SYNC/MODE2}$ resistor value selection per Table 4. The sequential interleave order of the slave phases is determined by FB and VSNS− pin connections shown in Table 1.

In a multi−phase system, the master outputs a SYNC signal to the parallel slaves' SYNC pins to establish a common switching frequency and evenly space the interleaved phases, as shown in the subsequent figure:

The falling edge of the SYNC pulse resets the ramp, beginning the interleaved PWM on cycles after a narrow propagation delay. The vertical dotted lines signify the modulated PWM edge (duty cycle).

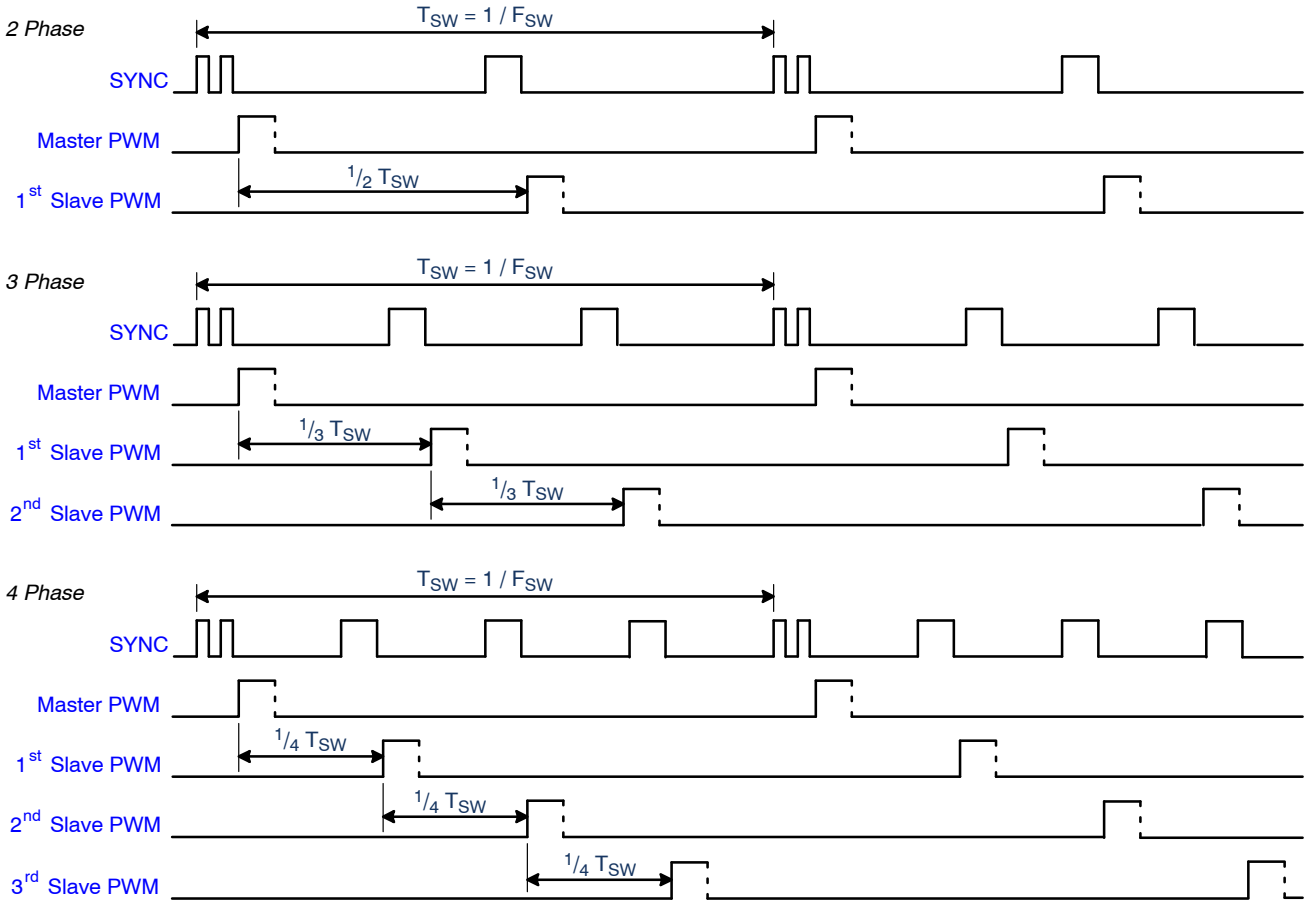


Figure 31. Multi−Phase Synchronization Timing

FAULT and SFAULT Operation

In a multi−phase application, communication between the master and slaves is accomplished via signaling over the VSET/FAULT and ADDR/SFAULT pins.

The following table is a summary of NCP3286 actions in response to the main fault conditions:

Table 5. MASTER / SLAVE ACTIONS BY PROTECTION TYPE

Master / Standalone		Protection Type	Slave	
Detection	**Action**		**Detection**	**Action**
V_{CC}	Auto recoverable Both power MOSFETS off FAULT pulled high SFAULT pulled low	UVLO	V_{CC}	Auto recoverable Both power MOSFETS off FAULT pulled high SFAULT pulled low
T_J	Auto recoverable Both power MOSFETS off FAULT pulled low	TSD	T_J	Auto recoverable Both power MOSFETS off SFAULT pulled low
I_{DRAIN}	Cycle−by−cycle current limit Both power MOSFETS off FAULT pulled low	OCP	I_{DRAIN}	Cycle−by−cycle current limit Both power MOSFETS off SFAULT pulled low
V_{FB}	Both power MOSFETS off FAULT pulled low	UVP	Master V_{FB}	Both power MOSFETS off after Master pulls FAULT low
V_{FB}	Ramp down DAC with FCCM High−side FET turns off Low−side FET remains on SFAULT pulled high	OVP	Master V_{FB}	Once Master pulls SFAULT high: High−side FET turns off Low−side FET remains on

FAULT and SFAULT Signaling

The VSET/FAULT and ADDR/SFAULT pins utilize bi−directional signaling for master/slave communication and fault management. The figures below illustrate circuit operation:

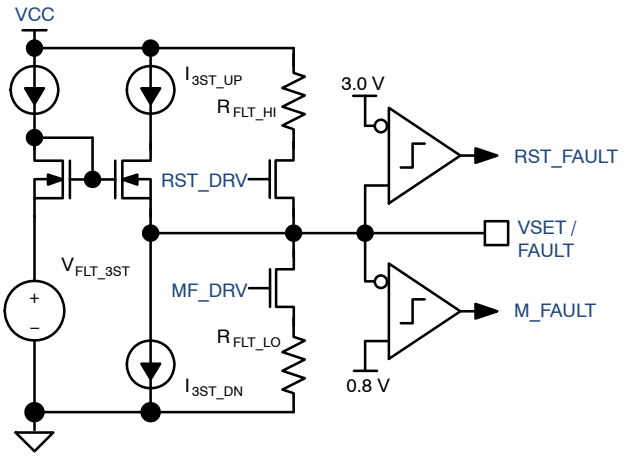


Figure 32. VSET/FAULT Pin Circuit

The internal signal MF_DRV asserts high when a master fault occurs. RST_DRV gets asserted to reset the system. M_FAULT and RST_FAULT are the associated fault signals (active high).

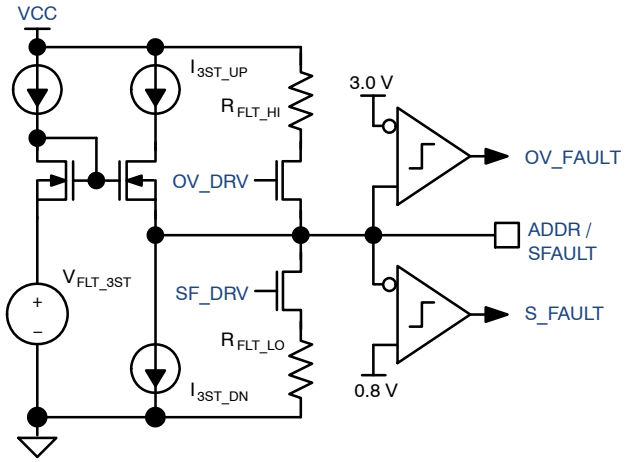


Figure 33. ADDR/SFAULT Pin Circuit

The internal signal OV_DRV asserts when the master detects an output OVP event, which forces the ADDR/SFAULT pin high. SF_DRV asserts when a slave needs to signal a fault condition. OV_FAULT and S_FAULT are the associated fault signals (active high).

When EN=0, the master forces both VSET/FAULT and ADDR/SFAULT low. Switching is prohibited.

The VSET/FAULT and ADDR/SFAULT signals remain tri−stated (2 V) during normal operation.

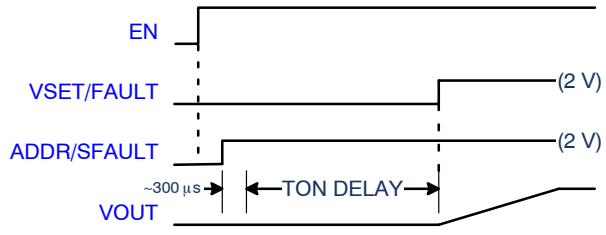


Figure 34. Master/Slave Start−Up Signals

At start−up, once EN is asserted, the master imposes a small housekeeping delay before tri−stating the ADDR/SFAULT pin, which awakens the slaves. While VSET/FAULT is low, all the master and slave FETs remain off.

After the TON_DELAY period expires, the master tri−states the VSET/FAULT pin and the soft−start cycle begins.

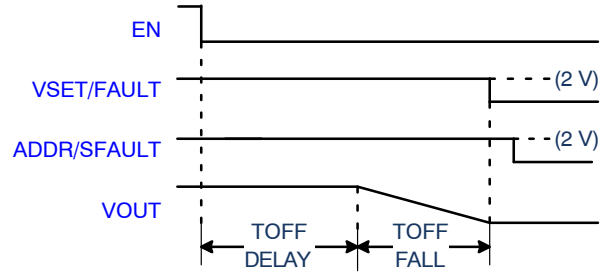


Figure 35. Master/Slave Power−Off Signals

When EN goes low, the VSET/FAULT and ADDR/SFAULT pins remain tri−stated until the TOFF_DELAY and TOFF_FALL intervals, set by their respective registers, expire. Then, the master lowers the VSET/FAULT pin which halts switching and all FETs are turned off. Later, the master lowers the ADDR/SFAULT pin, returning the slaves to their stand−by (inactive) state.

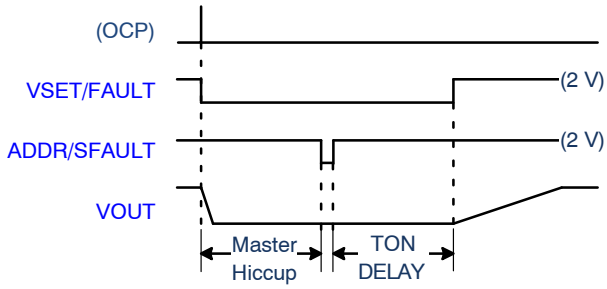


Figure 36. Master/Slave Signals, Master OCP or UVP

When the master encounters an over−current fault situation, indicated here by internal logic signal (OCP) high, it lowers the VSET/FAULT pin to instruct slaves to stop switching.

Once the master completes its hiccup cycle, it momentarily cycles ADDR/SFAULT low to reset and re−activate slaves.

Upon expiration of the TON_DELAY interval, the master tri−stats the VSET/FAULT pin and a soft−start cycle commences.

The same signaling/sequence is used in response to output under−voltage (UVP) faults.

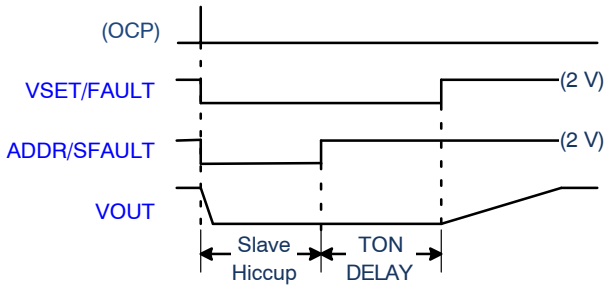


Figure 37. Master/Slave Signals, Slave OCP or OT Fault

When any slave encounters an over−current event, it signals the master by lowering the ADDR/SFAULT pin. As a result, the master forces VSET/FAULT low to halt all switching.

Once the slave hiccup period expires, it releases the ADDR/SFAULT signal. The master holds VSET/FAULT low to prevent all switching until TON_DELAY elapses. When the master releases the VSET/FAULT signal to the tri−state level, the soft−start cycle commences.

The same signaling/sequence is used in response to an over−temperature (OT) fault.

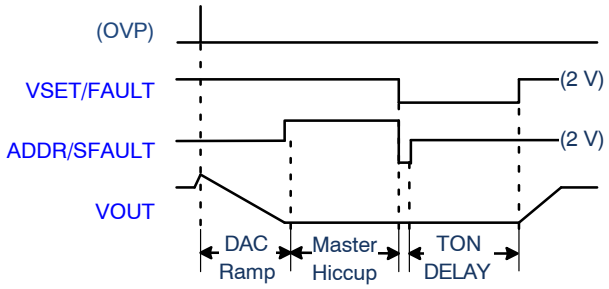


Figure 38. Master/Slave Signals, OVP Fault

In the event of an output over−voltage fault (OVP), the VSET/FAULT and ADDR/SFAULT pins both remain at 2 V until the DAC ramps down the output in a controlled fashion.

During the hiccup interval, the master pulls ADDR/SFAULT high, instructing the slaves to turn off high−side FETs and enhance low−side FETs.

After the hiccup cycle, the master forces both signals low, momentarily, which resets the slaves. Slave re−activate when the master releases the ADDR/SFAULT signal during the TON_DELAY interval. When the master releases the VSET/FAULT signal, the re−start ramp begins.

Operating / Fault States

The table below provides a summary of device and pin states during operating and/or fault conditions:

Table 6. STATE TRUTH TABLE

State / Condition	Action / Function				
	PGOOD Pin	**COMP Pin**	**OCP**	**OVP**	**UVP**
POR V_{CC} < UVLO	N/A	N/A	N/A	N/A	N/A
Disabled, EN low, V_{CC} > UVLO	Low	Low	Disabled	Disabled	Disabled
Start−Up Delay EN low, V_{CC} > UVLO, before SS ramp begins	Low	Low	Disabled	Disabled	Disabled
Soft Start EN high, V_{CC} > UVLO	Low	Active	Active	Active, (threshold = V_{OV_A})	Disabled
Normal Operation	High	Active	Active	Active, (threshold = V_{OVP_TH})	Active
Over−Current (OCP)	Low		Cycle−by−Cycle	Active until shutdown	Active until shutdown
Over−Voltage (OVP)	Low		Disabled		Disabled
Under Voltage (UVP)	Low		Disabled	Disabled	
Thermal Shutdown (T_{SD})	Low	Low	Disabled	Disabled	Disabled
Hiccup Idle Time	Low	Low	Disabled	Disabled	Disabled

PMBUS GENERAL DESCRIPTION

The PMBUS specification can be found at http://pmbus.org. The NCP3286 supports both 100 kHz and 400 kHz bus timing requirements. Communication over the PMBUS interface supports Packet Error Checking (PEC).

If the master/host provides the clock pulses for the PEC byte, PEC is used. If the additional clock pulses are not present before a STOP, the PEC is not used.

PMBUS has several formats. The NCP3286 supported formats are listed below.

PMBUS Send Byte

The Send Byte transaction is used to send a simple command to the device. A send byte transaction transfers a command with no data. The CLEAR_FAULTS command, which clears present fault flags, is a good example.

A start bit followed by the 7bit slave address with a 0 (write) appended comprises the first stage of the transaction. If the slave ACKs the address, then the host sends the 8bit command followed by a stop condition. A format example is shown below:

SEND BYTE

1	7	1	1	8	1	1
S	Slave Address	W	A	Command Code	A	P

PMBUS Read Byte

The Read Byte starts like a typical I^2C write transaction by sending the slave address, plus write bit, followed by a 2^{nd} byte containing the command code. Then a repeated start (S_R) is sent, followed by the slave address with read bit (1), requesting the slave device to return the data for the specified command code. The slave responds by transmitting the byte value requested.

READ BYTE

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	W	A	Command Code	A	S_R	Slave Address	R	A	Data Byte	N	P

PMBUS Read Word

The Read Word transaction also starts like a typical I^2C write by sending the slave address, plus write bit. The 2^{nd} byte contains the command code. Then a repeated start is sent, followed by the slave address with read bit, signaling the device to return data for the specified command code. The slave responds by transmitting the value requested, low data byte first, followed by the high data byte, as illustrated below:

READ WORD

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	S_R	Slave Address	R	A	Data Byte Low	A	Data Byte High	N	P

PMBUS Write Byte

The Write transaction is used by the host to send a single byte of data to the device. The OPERATION command, used to configure device operation, is an example of this type transaction.

The transaction begins with a start bit followed by the 7bit slave address with a 0 (write) appended as the 8^{th} bit the command byte, followed by the data byte, as illustrated below:

WRITE BYTE

1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte	A	P

PMBUS Write Word

The Write Word transaction is used by the host to send a single word of data (2 bytes) to the device. The TON_DELAY command is an example of this type transaction.

Similar to the write command, the only difference is that after the low data byte's ACK (3^{rd} ACK), the high data byte is sent in addition.

WRITE WORD

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

PMBUS Block Write

The Block Write begins with a slave address and a write condition. After the command code is sent, the host issues a byte count describing how many more bytes will follow.

The NCP3286 allows only 1 byte. The byte count field may only contain 01, followed by the one byte of data, as illustrated below:

BLOCK WRITE

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Byte Count (01h)	A	Data Byte	A	P

PMBUS Block Read

A Block Read differs from the Block Write because a repeated start (S_R) condition is necessary to satisfy the requirement for a change in data transfer direction. The NACK immediately preceding the stop bit signifies the end of the read transfer.

The NCP3286 allows only 1 byte. The byte count field may only contain 01, followed by the one byte of data, as illustrated below:

BLOCK READ

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	S_R	Slave Address	R	A	Byte Count (01h)	A	Data Byte	N	P

Packet Error Checking (PEC)

PEC is optionally implemented in PMBUS devices, but is highly recommended due to the critical nature of data validity in power management systems. Packet Error Code bytes are generated using the CRC−8 algorithm that is based on performing XOR operations on the input bit streams with a fixed CRC polynomial. The PEC byte is calculated on all bytes in the I^2C transaction, including device address and read/write. PEC does not include start, stop, ACK/NACK, or repeated start bits.

SEND BYTE WITH PEC

1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	PEC Byte	A	P

WRITE BYTE WITH PEC

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte	A	PEC Byte	A	P

WRITE WORD WITH PEC

1	7	1	1	8	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte Low	A	Data Byte High	A	PEC Byte	A	P

READ BYTE WITH PEC

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	S_R	Slave Address	R	A	Data Byte	A	PEC Byte	N	P

READ WORD WITH PEC

1	7	1	1	8	1	1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	S_R	Slave Address	R	A	Data Byte Low	A	Data Byte High	A	PEC Byte	N	P

BLOCK WRITE WITH PEC

1	7	1	1	8	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Byte Count (01h)	A	Data Byte	A	PEC Byte	A	P

BLOCK READ WITH PEC

1	7	1	1	8	1	1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	S_R	Slave Address	R	A	Byte Count (01h)	A	Data Byte	A	PEC Byte	N	P

Data Byte Formats

Various NCP3286 commands utilize different data byte encoding to accommodate negative numeric values, step size, and range supporting DAC and A2D values.

The type used is designated individually for each register of the PMBUS COMMAND DETAILS section of this document.

LINEAR11 Format

The LINEAR11 format consists of a 5bit, 2's complement integer exponent and 11bit linear mantissa, shown below:

LINEAR11 FORMAT

Data Byte High								Data Byte Low							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent (N)					Mantissa (Y)										

The exponent is a fixed binary value, positive or negative, which typically determines the step size or resolution for a given command.

The mantissa is an 11bit 2's complement integer typically establishing the range and may be selectively limited to discrete values.

The integer value (I) of the data byte in LINEAR11 format can be calculated using:

$$I = Y \cdot 2^N \qquad \text{(eq. 6)}$$

where: Y is a 2's complement integer from the mantissa
N is the 2's complement integer of the exponent

ULINEAR16 Format

In NCP3286, only the Linear Mode is supported: The VOUT_MODE bits are set to 100b, which establishes Linear Mode with Relative Setting, which allows the user to set VOUT related commands as a percentage or ratio of the programmed V_{OUT} level.

The VOUT_MODE data byte:

VOUT_MODE DATA BYTE

1	**0**	**0**	4	3	2	1	0
Mode			Exponent (N)				

This establishes the 5bit 2's complement exponent for the 16bit mantissa delivered as data bytes for an output voltage related command:

LINEAR16 FORMAT

Data Byte High								Data Byte Low							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Mantissa (Y)															

The integer value (V) of the full data byte in ULINEAR16 format can be calculated using:

$$V = Y \cdot 2^{N} \qquad \text{(eq. 7)}$$

where: Y is a 16bit unsigned binary integer from the mantissa

N is the 2's complement integer of the exponent

Table 7. PMBUS COMMAND SUPPORT

Reg	Name / Command	Type	To	Range	Step	Default	
						Data	Value / State
01h	OPERATION	R/W	M			00h	Immediate off
02h	ON_OFF_CONFIG	R/W	M			17h	Turn on with EN pin Turn off immediately
03h	CLEAR_FAULTS	W	M/S				
10h	WRITE_PROTECT	R/W	M/S			00h	Enable all writes
19h	CAPABILITY	R	M/S			B0h	PEC support, 400 kHz max, SMBALERT support, 4 numerical formats, No AVSBUS support
1B	SMBALERT_MASK	W	M/S	STATUS registers			Faults alert, Warns masked
20h	VOUT_MODE	R	M/S			98h	ULINEAR16 format, Linear mode with relative setting.
21h	VOUT_COMMAND	R/W	M/S	0.25 – 1.99 V (x1 scale) 0.50 – 3.99 V ($^1/_2$ scale) 1.00 – 5.5 V ($^1/_4$ scale)	3.90625 mV	→	set by $R_{VSET/FAULT}$
24h	VOUT_MAX	R/W	M/S	0.25 – 1.99 V (x1 scale) 0.50 – 3.99 V ($^1/_2$ scale) 1.00 – 5.5 V ($^1/_4$ scale)	3.90625 mV	2, 4, or 5.5 V	set by $R_{SS/MODE1}$
25h	VOUT_MARGIN_HIGH	R/W	M	102 – 110% of V_{FB}	2%	010Fh	106%
26h	VOUT_MARGIN_LOW	R/W	M	90 – 98% of V_{FB}	2%	00F1h	94%
27h	VOUT_TRANSITION_RATE	R/W	M	0.094, 0.48, 1.95, 4.88, 9.77 or 19.53 mV/μs	–	D006	94 μV/μs
29h	VOUT_SCALE_LOOP	R	M/S	0.25, 0.5 or 1.0		→	set by $R_{SS/MODE1}$
2Bh	VOUT_MIN	R/W	M/S	0.25 – 1.99 V (x1 scale) 0.50 – 3.99 V ($^1/_2$ scale) 1.00 – 5.5 V ($^1/_4$ scale)	3.90625 mV	0.25, 1.0, or 2.0 V	set by $R_{SS/MODE1}$
33h	FREQUENCY_SWITCH	R/W	M/S	200 – 1000 kHz, 1000 – 1200 kHz, 1200 – 2000 kHz	50 kHz, 100 kHz, 200 kHz	→	set by $R_{SYNC/MODE2}$
35h	VIN_ON	R/W	M	3.0 – 10.5 V_{PVIN}	0.5 V	F80Ch	PVIN = 6.0 V
36h	VIN_OFF	R/W	M	2.5 – 10.0 V_{PVIN}	0.5 V	F80Bh	PVIN = 5.5 V
37h	INTERLEAVE	R	M/S	4 options: Master, 1st, 2nd, or 3rd Slave		→	set by FB, VSNS– pin connections and $R_{SYNC/MODE2}$
39h	IOUT_CAL_OFFSET	R/W	M/S	–2.000 to 2.000 A	125 mA	E800h	0 A
40h	VOUT_OV_FAULT_LIMIT	R/W	M	105–135% of V_{FB}	2%	0136h	121%
41h	VOUT_OV_FAULT_RESPONSE	R/W	M	Latch–off, Hiccup		→	set by $R_{IMON/ILIM}$
				Hiccup Delay Time 32 – 256 ms	32 ms		32 ms
42h	VOUT_OV_WARN_LIMIT	R/W	M	103 – 118% of V_{FB}	1%	0114h	108%
43h	VOUT_UV_WARN_LIMIT	R/W	M	82 – 97% of V_{FB}	1%	00E6h	90%
44h	VOUT_UV_FAULT_LIMIT	R/W	M	20 – 95% of V_{FB}	5%	0033h	20%
45h	VOUT_UV_FAULT_RESPONSE	R/W	M	Latch–off, Hiccup		→	set by $R_{IMON/ILIM}$
				Hiccup Delay Time 32 – 256 ms	32 ms		32 ms
46h	IOUT_OC_FAULT_LIMIT	R/W	M/S	8 – 70 A	2A	→	set by $R_{IMON/ILIM}$
47h	IOUT_OC_FAULT_RESPONSE	R/W	M/S	Latch–off, Hiccup		→	set by $R_{IMON/ILIM}$
				Hiccup Delay Time 32 – 256 ms	32 ms		32 ms

Table 7. PMBUS COMMAND SUPPORT (continued)

Reg	Name / Command	Type	To	Range	Step	Default	
						Data	Value / State
4Ah	IOUT_OC_WARN_LIMIT	R/W	M/S	0 – 66 A	125 mA	→	set by $R_{IMON/ILIM}$
4Fh	OT_FAULT_LIMIT	R/W	M/S	80 – 160°C	0.5°C	F92Ch	150°C
50h	OT_FAULT_RESPONSE	R/W	M/S	Latch−off, Hiccup, Ignore		00h	ignore
				Hiccup Delay Time 32 – 256 ms	32 ms		32 ms
51h	OT_WARN_LIMIT	R/W	M/S	70°C to 150°C	0.5°C	F904h	130°C
55h	VIN_OV_FAULT_LIMIT	R/W	M	5 – 20 V_{PVIN}	1 V	0012h	PVIN = 18 V
56h	VIN_OV_FAULT_RESPONSE	R/W	M	Latch−off, Hiccup, Ignore		00h	ignore
				Hiccup Delay Time 32 – 256 ms	32 ms		32 ms
5Eh	POWER_GOOD_ON	R/W	M	84 – 98% of V_{FB}	2%	00E6	90%
5Fh	POWER_GOOD_OFF	R/W	M	82 – 96% of V_{FB}	2%	00D7	84%
60h	TON_DELAY	R/W	M	1 – 10 ms	1 ms	0001h	1 ms
61h	TON_RISE	R/W	M/S	1 – 20 ms	1 ms		set by $R_{SS/MODE1}$
64h	TOFF_DELAY	R/W	M	0 – 10 ms	1 ms	0000h	0 ms
65h	TOFF_FALL	R/W	M	1 – 20 ms	1 ms	0005h	5 ms
78h	STATUS_BYTE	R	M/S				
79h	STATUS_WORD	R	M/S				
7Ah	STATUS_VOUT	R	M/S				
7Bh	STATUS_IOUT	R	M/S				
7Ch	STATUS_INPUT	R	M/S				
7Dh	STATUS_TEMPERATURE	R	M/S				
7Eh	STATUS_CML	R	M/S				
80h	STATUS_MFR_SPECIFIC	R	M/S				
88h	READ_VIN	R	M/S	0 – 32 V_{PVIN}	31.25 mV		
8Bh	READ_VOUT	R	M	0 – 5.5 V	3.90625 mV		
8Ch	READ_IOUT	R	M/S	−64 to 64 A	125 mA		
8Dh	READ_TEMPERATURE	R	M/S	−256 to 256°C	0.5°C		
98h	PMBUS_REVISION	R	M/S			33h	PMBUS rev 1.3
A4h	MFR_VOUT_MIN	R	M/S		3.90625 mV	0040h	0.25 V
A5h	MFR_VOUT_MAX	R	M/S		3.90625 mV	0580h	5.5 V
ADh	IC_DEVICE_ID	RB	M/S			8601h	NCP3286
AEh	IC_DEVICE_REV	RB	M/S			XY01h	XY = revision
C4h	I_BALANCE_OFFSET	R/W	M/S	−3.875 to 3.875 A	125 mA	E800h	0A
C5h	MFR_PMBUS_BASE	R	M/S			10h	10h base address

Legend: R Read W Write RB Block Read M Master S Slave

PMBUS COMMAND DETAILS

Default bit values are identified by **BOLD** text.

OPERATION (Reg01h)

This single byte command is used to configure the operational state of the regulator in conjunction with the EN pin. The OPERATION command can be used to:

- Turn the regulator on/off with PMBUS commands.
- Select the margin state of the device (margin low, margin high, or margin off).
- Select whether fault conditions induced by margining are ignored or acted upon.
- Select whether the regulator powers down immediately or executes the TOFF_DELAY and TOFF_FALL settings.

Table 8. OPERATION COMMAND BIT FUNCTIONS

Bit	Type	Value	Description
7	R/W	**0**	Regulator is off.
		1	Regulator enabled with EN conditions.
6	R/W	**0**	Turn off immediately.
		1	Power−down sequence using TOFF_DELAY and TOFF_FALL.
5:4	R/W	**00**	V_{OUT} per VOUT_COMMAND.
		01	VOUT_MARGIN_LOW control.
		10	VOUT_MARGIN_HIGH control.
		11	not care
3:2	R/W	**00**	not care
		01	Ignore faults during margining.
		10	Act on faults during margining.
		11	not care
1:0	R	**00**	reserved

The default register value is **00h**.

Table 9. SUPPORTED OPERATION COMMANDS SUMMARY

Data (b)	Device Operation Response
00XX XXXX	Immediate power down
01XX XXXX	Sequenced power down using TOFF_DELAY and TOFF_FALL
1X00 XXXX	V_{OUT} controlled by VOUT_COMMAND
1X11 XXXX	
1X01 01XX	VOUT_MARGIN_LOW control, faults ignored
1X01 10XX	VOUT_MARGIN_LOW control, act on faults
1X10 01XX	VOUT_MARGIN_HIGH control, faults ignored
1X10 10XX	VOUT_MARGIN_HIGH control, act on faults

Table 10. INVALID OPERATION COMMANDS, BITS [7:2]

Data (b)	Data (b)
1001 00	1101 00
1001 11	1101 11
1010 00	1110 00
1010 11	1110 11

Sending data shown in the table above results in an Invalid Data Fault and is rejected. Any other data is accepted.

Writes to bits 1:0 are ignored and will not result in an Invalid Data fault.

ON_OFF_CONFIG (Reg02h)

This one byte command configures the combination of EN pin input and serial bus commands needed to turn the device on and/or off, including how the device responds when input power is applied.

Table 11. ON_OFF_CONFIG SINGLE BYTE FORMAT

Bit	Type	Value	Description
7:5	R	**000**	reserved
4	R/W	0	Device starts when VCC present.
		1	Device starts when EN asserted and when commanded by OPERATION [3:0].
3	R/W	**0**	Bit [7] of OPERATION command is ignored.
		1	OPERATION [7] must be 1 for device to start. Also depends on ON_OFF_CONFIG [2].
2	R/W	0	EN pin ignored. On/off control by OPERATION only.
		1	EN must be asserted to start/run. Also depends on ON_OFF_CONFIG [3].
1	R/W	0	EN pin polarity = asserted low.
		1	EN pin polarity = asserted high.
0	R/W	0	EN pin de−assert commands delayed turn off set by TOFF_DELAY and TOFF_FALL registers.
		1	EN pin de−assert commands immediate turn off.

The default register value is **17h**.

Writes to bits 7:5 are ignored and do not result in an Invalid Data Fault.

Table 12. VALID ON_OFF_CONFIG COMMANDS, BITS [4:1]

Data (b)	Description
0XX1	Turn on when input power present.
1011	Turn on when EN pin asserts.
1101	Turn on (soft enable) with OPERATION [7] high.
1111	Turn on requires both EN asserted and OPERATION [7] high.

Attempts to write data other than shown in the table above will result in an Invalid Data Fault.

CLEAR_FAULTS (Reg03h)

This command is used to clear any fault bits that have been set. It clears all fault bits in all status registers and releases the ALERT# signal if asserted.

CLEAR_FAULTS will not restart a device that has latched−off due to a fault condition. A latched−off device will remain off until:

- The output is commanded through the EN pin, the OPERATION command, or the combined action of both, to turn off and then back on again.
- Removing, and then restoring VCC bias power. Device will restart in its default state. Fault bits are cleared when VCC < V_{CC_UV} threshold.
- Faults are also cleared based on the turn on settings established by ON_OFF_CONFIG:
  If EN is used for turn−on, faults are cleared when EN goes low.
  If soft enable used for turn−on, faults clear when OPERATION [7] is set to 0.
  If soft enable and the EN pin are both used for turn−on, faults clear when OPERATION [7] and EN are both low.
  When set to turn on with input voltage present, the faults are cleared when VCC power cycles.

If a fault condition persists after the fault bit is cleared, the fault bit shall immediately be set again and the host notified via the ALERT# signal.

Any or all fault bits in any status register except STATUS_BYTE and STATUS_WORD can be directly cleared by issuing the status command with 1 binary data byte. The binary data byte bits align with the corresponding status registers bits. To clear fault bits, write a 1 to the corresponding bit in the binary data byte. For example:

Table 13. EXAMPLE FAULT/STATUS BIT CLEARING

Data (b)	Description
0001 0000	Bit [4] is cleared. All others remain unchanged.
0110 0010	Bits [6], [5], and [1] are cleared. All others remain unchanged.
1111 1111	Writing FFh clears all bits in the specified register.

Additional details are located in the PMBUS Device Fault Management section.

WRITE_PROTECT (Reg10h)

This command can be used to prevent unintentional configuration or settings changes. All supported commands may have their parameters read, regardless of WRITE_PROTECT settings

The single byte is formatted as shown below:

Table 14. WRITE_PROTECT FORMAT

Data (h)	Description
80	Disable all writes, except to the WRITE_PROTECT register
40	Disable all writes, except to the WRITE_PROTECT and OPERATION registers
20	Disable all writes, except to the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG, and VOUT_COMMAND registers
00	Enable writes to all commands

The default register value is **00h**.

If the device receives a data byte other than listed in the table above, it is treated as invalid data and triggers a data fault. The device responds by:

- Ignores/flushes the command code and received data
- Sets the CML bit in STATUS_BYTE
- Sets the Invalid Data Fault bit in the STATUS_CML register

CAPABILITY (Reg19h)

This register provides a quick method for the system/host to determine some key capabilities of a PMBUS device.

The register is read only and **returns B0h**.

The single byte is formatted as shown below:

Table 15. CAPABILITY BYTE FORMAT

Bit	Type	Value	Description
7	R	0	PEC format not supported
		1	PEC format supported
6:5	R	00	Maximum bus speed 100 kHz
		01	Maximum bus speed 400 kHz
		10	Maximum bus speed 1 MHz
		11	Reserved
4	R	0	No ALERT# pin/function
		1	ALERT# pin and support
3	R	**0**	Numeric data LINEAR11, ULINEAR16 or direct format
		1	Numeric data is IEEE half precision floating point format
2	R	**0**	AVSBus not supported
		1	AVSBus support
1:0	R	**00**	reserved

SMBALERT_MASK (Reg1Bh)

This command can be used to prevent WARN or FAULT conditions from asserting the open−drain ALERT# signal.

By default: **WARNS are masked**

FAULTS are not masked

This command has 2 data bytes, as illustrated below:

SMBALERT_MASK FORMAT

7	1		8		8		8	
Slave Address	W	A	SMBALERT_ MASK Command Code	A	STATUS_X Command Code	A	Mask Byte	A

The Mask Byte bits align with the corresponding STATUS_REGISTERX bits. For detailed bit locations and descriptions, refer to the STATUS_REGISTERX command tables.

For example, to mask an over−temperature warning (OT_WARN), the STATUS_ TEMPERATURE command code is sent along with the mask byte of 01000000b (40h).

VOUT_MODE (Reg20h)

This read only register provisions the ULINEAR16 format settings.

VOUT_MODE reads back 98h. Attempts to write to this register will be rejected, but an Invalid Data Fault is not issued.

VOUT_MODE FORMAT

Data Byte High								Data Byte Low							
1	**0**	**0**	**1**	**1**	**0**	**0**	**0**	7	6	5	4	3	2	1	0
Mode			Exponent												
Mantissa V															

The exponent is fixed −8 (11000b) and the Mode bits are fixed to 100b, indicating Linear Mode with Relative setting, which allows users to set the following V_{OUT} related commands as a percentage of V_{OUT}:

- VOUT_MARGIN_HIGH (Reg25h)
- VOUT_MARGIN_LOW (Reg26h)
- VOUT_OV_FAULT_LIMIT (Reg40h)
- VOUT_OV_WARN_LIMIT (Reg42h)
- VOUT_UV_WARN_LIMIT (Reg43h)
- VOUT_UV_FAULT_LIMIT (Reg44h)
- POWER_GOOD_ON (Reg5Eh)
- POWER_GOOD_OFF (Reg5Fh)

VOUT_COMMAND (Reg21h)

This command sets the target value of V_{OUT} when the OPERATION command is set for PMBUS nominal operation.

The VOUT_COMMAND follows the ULINEAR16 format, Linear Mode only.

Table 16. VOUT_COMMAND RANGE AND RESOLUTION

Range	Resolution	Default
0.25 V – 5.5 V	3.90625 mV	$R_{VSET/FAULT}$

The exponent is fixed −8 (11000b) and the allowable mantissa range extends from 40h to 580h. Any data outside this range flags an Invalid Data Fault.

Table 17. EXAMPLE VOUT_COMMAND SETTINGS

V_{OUT} (V)	Data (h)		V_{OUT} (V)	Data (h)
0.8	00CD		2.0	0200
1.0	0100		3.3	034D
1.5	0180		5.0	0500
1.8	01CD		5.5	0580

The default V_{OUT} level is set by $R_{VSET/FAULT}$ and the VOUT_SCALE_LOOP setting, established by $R_{SS/MODE1}$.

Table 18. RECOMMENDED VOUT_SCALE_LOOP SETTINGS

	VOUT_SCALE_LOOP	
V_{OUT} Range (V)	Scale (N)	Data (h)
0.25 – 1.99	1	F004
0.50 – 3.99	1/2	F002
1.00 – 5.50	1/4	F001

Table 19. VOUT_COMMAND REGISTER SETTINGS PER $R_{VSET/FAULT}$

$R_{VSET/FAULT}$ (kΩ)	Default V_{OUT} (V)			Scale (N)
	1 Scale	1/2 Scale	1/4 Scale	
10.0	0.50	1.30	2.40	1
15.0	0.55	1.35	2.50	
18.2	0.60	1.40	2.60	
22.1	0.65	1.45	2.70	
27.4	0.70	1.50	2.80	
33.2	0.75	1.55	2.90	1/2
39.2	0.80	1.60	3.00	
47.5	0.85	1.65	3.10	
56.2	0.90	1.70	3.20	
68.1	0.95	1.75	3.30	
82.5	1.00	1.80	3.40	1/4
100	1.05	1.90	3.50	
121	1.10	2.00	4.00	
150	1.15	2.10	4.50	
182	1.20	2.20	5.00	
221	1.25	2.30	5.50	

If VOUT_COMMAND register contents change when the device is regulating, the system moves to the new V_{OUT} level as set by VOUT_TRANSITION_RATE. Until regulation is achieved at the new V_{OUT} level, further VOUT_COMMAND changes should not be made.

VOUT_MAX (Reg24h)

This register sets the absolute maximum allowed V_{OUT} target, regardless of any other commands.

VOUT_MAX follows the ULINEAR16 format.

Table 20. VOUT_MAX RANGE AND RESOLUTION

Range	Resolution	Default
0.25 V – 5.5 V	3.90625 mV	$R_{SS/MODE1}$

The default value of VOUT_MAX is determined by the VOUT_SCALE_LOOP setting established by $R_{SS/MODE1}$.

Table 21. VOUT_MAX SETTINGS PER $R_{SS/MODE1}$

$R_{SS/MODE1}$ (kΩ)	Scale (N)	V_{OUT_MAX} (V)	Data (h)
10.0	1	2.0 V	0200
15.0			
18.2			
22.1			
27.4			
33.2	1/2	4.0 V	0400
39.2			
47.5			
56.2			
68.1			
82.5	1/4	5.5 V	0580
100			
121			
150			
182			
221			

For VOUT_SCALE_LOOP = 1, if VOUT_MAX data is not within the range of 0041−0200h (0.25 − 1.99 V), an Invalid Data Fault will flag.

For VOUT_SCALE_LOOP = 1/2, if VOUT_MAX data is not within the range of 0080−0400h (0.50 − 3.99 V), it flags an Invalid Data Fault.

For VOUT_SCALE_LOOP = 1/4, if VOUT_MAX data is not within the range of 0100−0580h (1.0 − 5.5 V), an Invalid Data Fault flags.

If VOUT_MAX is set less than or equal to the VOUT_MIN setting, an Invalid Data Fault is flagged.

VOUT_MARGIN_HIGH (Reg25h)

This register is used to set the target V_{OUT} value when the OPERATION command is configured for Margin High.

Table 22. VALID VOUT_MARGIN_HIGH SETTINGS

MARGIN_HIGH (%V_{FB})	Data (h)
102	0105
104	010A
106	**010F**
108	0114
110	011A

All supported options are shown in the table.
Attempts to write data, other than shown in the table, will result in an Invalid Data Fault.

VOUT_MARGIN_LOW (Reg26h)

This register is used to set the target V_{OUT} value when the OPERATION command is configured for Margin Low.

Table 23. VALID VOUT_MARGIN_LOW SETTINGS

MARGIN_LOW (%V_{FB})	Data (h)
98	00FB
96	00F6
94	**00F1**
92	00EC
90	00E6

All supported options are shown in the table. Attempts to write data, other than shown in the table, will result in an Invalid Data Fault.

VOUT_TRANSITION_RATE (Reg27h)

This register sets the V_{OUT} transition/slew rate whenever V_{OUT} is instructed to change by VOUT_COMMAND or OPERATION (Margin: High, Low, or Off).

The VOUT_TRANSITION_RATE command has 2 data bytes encoded in LINEAR11 format.

Table 24. VALID VOUT_TRANSITION RATE SETTINGS

Rate (mV/μs)	Data (h)		Rate (mV/μs)	Data (h)
0.094	**D006**		4.883	D139
0.484	D01F		9.766	D271
1.953	D07D		19.531	D4E2

Attempts to write data other than shown in the table above will result in an Invalid Data Fault.

VOUT_SCALE_LOOP (Reg29h)

This read only register contains the output voltage sense scaling ratio for the V_{OUT} control loop, as set by $R_{SS/MODE1}$.

For V_{OUT} Scale settings other than 1, a resistor divider of equivalent ratio is required from V_{OUT} to FB to VSNS−.

Table 25. VOUT_SCALE_LOOP SETTINGS PER $R_{SS/MODE1}$

$R_{SS/MODE1}$ (kΩ)	Scale (N)	Data (h)		$R_{SS/MODE1}$ (kΩ)	Scale (N)	Data (h)
10.0	1	F004		82.5	1/4	F001
15.0				100		
18.2				121		
22.1				150		
27.4				182		
33.2	1/2	F002		221		
39.2						
47.5						
56.2						
68.1						

The VOUT_SCALE_LOOP command has 2 data bytes encoded in LINEAR11 format.

VOUT_MIN (Reg2Bh)

This register sets the absolute minimum allowed V_{OUT} target, regardless of any other commands.

VOUT_MIN follows the ULINEAR16 format.

Table 26. VOUT_MIN RANGE AND RESOLUTION

Range	Resolution	Default
0.25 V – 5.5 V	3.90625 mV	$R_{SS/MODE1}$

The default value of VOUT_MIN is determined by the VOUT_SCALE_LOOP setting established by $R_{SS/MODE1}$.

Table 27. VOUT_MIN SETTINGS PER $R_{SS/MODE1}$

$R_{SS/MODE1}$ (kΩ)	Scale (N)	V_{OUT_MIN} (V)	Data (h)
10.0	1	0.25 V	0041
15.0			
18.2			
22.1			
27.4			
33.2	1/2	1.0 V	0101
39.2			
47.5			
56.2			
68.1			
82.5	1/4	2.0 V	0201
100			
121			
150			
182			
221			

For VOUT_SCALE_LOOP = 1, if VOUT_MIN data is not within the range of 0041−0200h (0.25 − 1.99 V), an Invalid Data Fault will flag.

For VOUT_SCALE_LOOP = 1/2, if VOUT_MIN data is not within the range of 0080−0400h (0.50 – 3.99 V), it flags an Invalid Data Fault.

For VOUT_SCALE_LOOP = 1/4, if VOUT_MIN data is not within the range of 0100−0580h (1.0 – 5.5 V), an Invalid Data Fault flags.

If the VOUT_MIN data is greater than or equal to the VOUT_MAX setting, an Invalid Data Fault is flagged.

FREQUENCY_SWITCH (Reg33h)

This command sets the fundamental switching frequency, per phase, in kHz. The default value, at power−up, is established by the $R_{SYNC/MODE2}$ value.

Table 28. VALID DEFAULT F_{SW} SETTINGS PER $R_{SYNC/MODE2}$

R_{SYNC} (kΩ)	Phases (N)	F_{SW} (kHz)		R_{SYNC} (kΩ)	Phases (N)	F_{SW} (kHz)
10.0	1	500		56.2	3	300
15.0		600		68.1		400
18.2		700		82.5		500
22.1		800		100		600
27.4	2	500		121	4	350
33.2		600		150		400
39.2		700		182		450
47.5		800		221		500

Table 29. VALID F_{SW} SETTINGS VIA PMBUS

Switching Frequency (kHz)				
1 Phase	2 Phase	3 Phase	4 Phase	Data (h)
200	200	200	200	0864
250	250	250	250	087D
300	300	300	300	0896
350	350	350	350	08AF
400	400	400	400	08C8
450	450	450	450	08E1
500	500	500	500	08FA
550	550	550		0913
600	600	600		092C
650	650	650		0945
700	700			095E
750	750			0977
800	800			0990
850	850			09A9
900	900			09C2
950	950			09DB
1,000	1,000			09F4
1,100				0A26
1,200				0A58
1,400				0ABC
1,600				0B20
1,800				0B84
2,000				0BE8

Attempts to write data, other than that permitted in the table above, will result in an Invalid Data Fault.

VIN_ON (Reg35h)

This command sets the value of rising V_{IN} where power switching is allowed.

VIN_ON has 2 data bytes encoded in LINEAR11 format. The fixed −1 exponent (11111b) is in 2's Complement format and the mantissa is un−signed binary.

Table 30. VALID VIN_ON SETTINGS

Threshold (V)	Data (h)		Threshold (V)	Data (h)
3.0	F806		7.0	F80E
3.5	F807		7.5	F80F
4.0	F808		8.0	F810
4.5	F809		8.5	F811
5.0	F80A		9.0	F812
5.5	F80B		9.5	F813
6.0	**F80C**		10.0	F814
6.5	F80D		10.5	F815

All supported options are shown in the table above. Attempts to write data other than shown in the table above will result in an Invalid Data Fault.

If the VIN_ON threshold value is set equal or lower than the VIN_OFF threshold, an Invalid Data Flag is set.

VIN_OFF (Reg36h)

This command sets the value of falling V_{IN} where power conversion ceases.

VIN_OFF has 2 data bytes encoded in LINEAR11 format. The fixed −1 exponent (11111b) is in 2's Complement format and the mantissa is un−signed binary.

Table 31. VALID VIN_OFF SETTINGS

Threshold (V)	Data (h)		Threshold (V)	Data (h)
2.5	F805		6.5	F80E
3.0	F806		7.0	F80E
3.5	F807		7.5	F80F
4.0	F808		8.0	F810
4.5	F809		8.5	F811
5.0	F80A		9.0	F812
5.5	**F80B**		9.5	F813
6.0	F80C		10.0	F814

All supported options are shown in the table above. Attempts to write data other than shown in the table above will result in an Invalid Data Fault.

If the VIN_OFF threshold value is set greater or equal than the VIN_ON threshold, an Invalid Data Flag is set.

INTERLEAVE (Reg37h)

This register contains the interleaved timing positions of the master and slaves when used in a stackable, multi−phase configuration.

INTERLEAVE is a read only 16 bit read only command with 4 components illustrated below:

INTERLEAVE REGISTER FORMAT

Data Byte High								Data Byte Low							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
reserved				Group ID				Number in Group				Interleave Order			
0000				**0000**				**$R_{SYNC/MODE2}$**				**VSNS− and FB pins**			

Bit values are shown in **BOLD** text. Two components are determined by hardware configuration.

Number in Group (how many phases) is established by the $R_{SYNC/MODE2}$ value:

Table 32. PHASE COUNT SETTINGS

$R_{SYNC/MODE2}$ (kΩ)	Number in Group		$R_{SYNC/MODE2}$ (kΩ)	Number in Group
10.0	1		56.2	3
15.0			68.1	
18.2			82.5	
22.1			100	
27.4	2		121	4
33.2			150	
39.2			182	
47.5			221	

Interleave Order is established by the VSNS− and FB pin connections:

Table 33. INTERLEAVE ORDER SETTINGS

Phase	FB	VSNS−	Interleave Order
Master	V_{OUT}	GND	0
1st Slave	VCC	GND	1
2nd Slave	VCC	VCC	2
3rd Slave	VCC	100kΩ	3

IOUT_CAL_OFFSET (Reg39h)

The IOUT_CAL_OFFSET command can be used to null offsets in the current sensing circuit.

The two data bytes are encoded in LINEAR11 format. The exponent is fixed −3(11101b) in 2's complement format with binary signed mantissa.

Table 34. VALID IOUT_CAL_OFFSET SETTINGS

Offset (A)	Data (h)		Offset (A)	Data (h)
2.000	E810		−0.125	EFFF
1.875	E80F		−0.250	EFFE
1.750	E80E		−0.375	EFFD
1.625	E80D		−0.500	EFFC
1.500	E80C		−0.625	EFFB
1.375	E80B		−0.750	EFFA
1.250	E80A		−0.875	EFF9
1.125	E809		−1.000	EFF8
1.000	E808		−1.125	EFF7
0.875	E807		−1.250	EFF6
0.750	E806		−1.375	EFF5
0.625	E805		−1.500	EFF4
0.500	E804		−1.625	EFF3
0.375	E803		−1.750	EFF2
0.250	E802		−1.875	EFF1
0.125	E801		−2.000	EFF0
0	**E800**			

Attempts to write data, other than shown in the table above, will result in an Invalid Data Fault.

VOUT_OV_FAULT_LIMIT (Reg40h)

This command sets the threshold for a V_{OUT} Over−Voltage Fault.

Table 35. VALID VOUT_OV_FAULT_LIMIT SETTINGS

Limit (%V_{FB})	Data (h)		Limit (%V_{FB})	Data (h)
105	010D		**121**	**0136**
107	0112		123	013B
109	0117		125	0140
111	011C		127	0145
113	0121		129	014A
115	0126		131	014F
117	012C		133	0154
119	0131		135	015A

Attempts to write data, other than shown in the table above, will result in an Invalid Data Fault.

Setting the VOUT_OV_FAULT_LIMIT less than or equal to the VOUT_OV_WARN_LIMIT results in an Invalid Data Fault.

VOUT_OV_FAULT_RESPONSE (Reg41h)

This command instructs the device what action to take in response to a VOUT_OV_FAULT_LIMIT induced fault.

The device also:

- Sets the VOUT_OV bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT_OV fault bit in STATUS_VOUT
- Notifies the host by asserting ALERT#

Table 36. VALID VOUT_OV_FAULT_RESPONSE SETTINGS

Bit	Name	Value	Description
7:6	Ignore, latch−off, or recover	**10**	Device shuts down and responds according to the Restart Setting [5:3]
5:3	Restart Setting (default value established by $R_{IMON/ILIM}$)	000	Latch−off: device does not attempt restart. 56 kΩ < $R_{IMON/ILIM}$ ≤ 221 kΩ
		111	Hiccup: continuous periodic restart attempts at rate set by Restart Delay Time [2:0]. 10 kΩ ≤ $R_{IMON/ILIM}$ < 48 kΩ
2:0	Restart Delay Time	**000**	32 ms
		001	64 ms
		010	96 ms
		011	128 ms
		100	160 ms
		101	192 ms
		110	224 ms
		111	256 ms

Attempts to write data, other than permitted in the table above, will result in an Invalid Data Fault.

Once the fault bit is set, it is latched and can only be cleared in accordance with the Clear Faults section. Fault bits do not automatically clear when the fault ceases.

VOUT_OV_WARN_LIMIT (Reg42h)

This command sets the threshold for a V_{OUT} Over−Voltage warning.

Table 37. VALID VOUT_OV_WARN_LIMIT SETTINGS

Limit (%V_{FB})	Data (h)		Limit (%V_{FB})	Data (h)
103	0108		111	011C
104	010A		112	011F
105	010D		113	0121
106	010F		114	0124
107	0112		115	0126
108	**0114**		116	0129
109	0117		117	012C
110	011A		118	012E

Attempts to write data, other than shown in the table above, will result in an Invalid Data Fault being set.

Setting the VOUT_OV_WARN_LIMIT higher or equal to the VOUT_OV_FAULT_LIMIT will result in an Invalid Data Fault.

During a VOUT_OV warn condition, the device also:

- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT_OV warn bit in STATUS_VOUT
- Notifies the host by asserting ALERT#, if not masked

VOUT_UV_WARN_LIMIT (Reg43h)

This command sets the threshold for a V_{OUT} Under−Voltage warning.

Table 38. VALID VOUT_UV_WARN_LIMIT SETTINGS

Limit (%V_{FB})	Data (h)		Limit (%V_{FB})	Data (h)
82	00D2		**90**	**00E6**
83	00D5		91	00E9
84	00D7		92	00EC
85	00D9		93	00EE
86	00DC		94	00F1
87	00DF		95	00F3
88	00E1		96	00F6
89	00E4		97	00F8

Attempts to write data, other than permitted by the table above, will result in an Invalid Data Fault.

Setting the VOUT_UV_WARN_LIMIT lower or equal to the VOUT_UV_FAULT_LIMIT will flag an Invalid Data Fault.

During a VOUT_UV warn condition, the device also:

- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT_UV warn bit in STATUS_VOUT
- Notifies the host by asserting ALERT#, if not masked

VOUT_UV_FAULT_LIMIT (Reg44h)

This command sets the threshold for a V_{OUT} Under−Voltage Fault.

Table 39. VALID VOUT_UV_FAULT_LIMIT SETTINGS

Limit (%V_{FB})	Data (h)		Limit (%V_{FB})	Data (h)
20	**0033**		60	009A
25	0040		65	00A6
30	004D		70	00B3
35	005A		75	00C0
40	0066		80	00CD
45	0073		85	00DA
50	0080		90	00E6
55	008D		95	00F3

Attempts to write data, other than shown in the table above, will result in an Invalid Data Fault.

Setting the VOUT_UV_FAULT_LIMIT greater or equal to the VOUT_UV_WARN_LIMIT results in an Invalid Data Fault.

VOUT_UV_FAULT_RESPONSE (Reg45h)

This command instructs the device what action to take in response to a VOUT_UV_FAULT_LIMIT induced fault.

The device also:

- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT_UV fault bit in STATUS_VOUT
- Notifies the host by asserting ALERT#

Table 40. VALID VOUT_UV_FAULT_RESPONSE SETTINGS

Bit	Name	Value	Description
7:6	Ignore, latch−off, or recover	**10**	Device shuts down and responds according to the Restart Setting [5:3]
5:3	Restart Setting (default value established by $R_{IMON/ILIM}$)	000	Latch−off: device does not attempt restart. 56 kΩ < $R_{IMON/ILIM}$ ≤ 221 kΩ
		111	Hiccup: continuous periodic restart attempts at rate set by Restart Delay Time [2:0]. 10 kΩ ≤ $R_{IMON/ILIM}$ < 48 kΩ
2:0	Restart Delay Time	**000**	32 ms
		001	64 ms
		010	96 ms
		011	128 ms
		100	160 ms
		101	192 ms
		110	224 ms
		111	256 ms

Attempts to write data, other than shown in the table above, will result in an Invalid Data Fault.

Once the fault bit is set, it is latched and can only be cleared in accordance with the Clear Faults section. The fault bit does not automatically clear when the fault condition ceases.

IOUT_OC_FAULT_LIMIT (Reg46h)

This command determines the valley over−current (I_{VLY}) protection fault threshold.

The two data bytes are encoded in LINEAR11 format.

Table 41. VALID IOUT_OC_FAULT_LIMIT SETTINGS

Threshold (A)	Data (h)	Threshold (A)	Data (h)
8	0804	40	0814
10	0805	42	0815
12	0806	44	0816
14	0807	46	0817
16	0808	48	0818
18	0809	50	0819
20	080A	52	081A
22	080B	54	081B
24	080C	56	081C
26	080D	58	081D
28	080E	60	081E
30	080F	62	081F
32	0810	64	0820
34	0811	66	0821
36	0812	68	0822
38	0813	70	0823

Attempts to write data, other than indicated in the table above, will result in an Invalid Data Fault.

The default IOUT_OC_FAULT_LIMIT value is set by the selection of $R_{IMON/ILIM}$. The associated default thresholds are shown in the table below:

Table 42. DEFAULT I_{VLY} SETTING ESTABLISHED BY $R_{IMON/ILIM}$

	$R_{IMON/ILIM}$ (kΩ)		
Threshold (A)	Hiccup	Latch−Off	Data (h)
14	10.0	56.2	0807
18	15.0	68.1	0809
24	18.2	82.5	080C
30	22.1	100	080F
36	27.4	121	0812
42	33.2	150	0815
50	39.2	182	0819
60	47.5	221	081E

IOUT_OC_FAULT_RESPONSE (Reg47h)

This command instructs the device what action to take in response to an IOUT_OC_FAULT_LIMIT induced fault.

The device also:

- Sets the IOUT OCP bit in the STATUS_BYTE
- Sets the IOUT bit in the STATUS_WORD
- Sets the OCP Peak fault bit in STATUS_IOUT
- Notifies the host by asserting ALERT#

Table 43. VALID IOUT_OC_FAULT_RESPONSE SETTINGS

Bit	Name	Value	Description
7:6	Ignore, latch−off, or recover	**11**	Device shuts down and responds according to the Restart Setting [5:3]
5:3	Restart Setting (default value established by $R_{IMON/ILIM}$)	000	Latch−off: device does not attempt restart. 56 kΩ < $R_{IMON/ILIM}$ ≤ 221 kΩ
		111	Hiccup: continuous periodic restart attempts at rate set by Restart Delay Time [2:0]. 10 kΩ ≤ $R_{IMON/ILIM}$ < 48 kΩ
2:0	Restart Delay Time	**000**	32 ms
		001	64 ms
		010	96 ms
		011	128 ms
		100	160 ms
		101	192 ms
		110	224 ms
		111	256 ms

Attempts to write data, other than shown in the table above, will result in an Invalid Data Fault.

Once the fault bit is set, it is latched and can only be cleared in accordance with the Clear Faults section. The fault bit does not automatically clear when the fault condition ceases.

IOUT_OC_WARN_LIMIT (Reg4Ah)

This command sets the Over−Current Warning limit (I_{LIM}).

The device also:

- Sets the IOUT/POUT bit in the STATUS_WORD
- Sets the OCP Warn fault bit in STATUS_IOUT

Table 44. IOUT_OC_WARN_LIMIT RANGE AND RESOLUTION

Range	Resolution	Default
0 V – 66 V	125 mA	$R_{IMON/ILIM}$

The two data bytes are encoded in LINEAR11 format. The read only exponent is fixed −3 (11101b). Writing an exponent other than −3 will result in an Invalid Data Fault.

Writing negative Warn Limits to this register is not allowed. If the MSB of the mantissa (bit 10) is high, an Invalid Data Fault is flagged.

Once set, the Warn bit can only be cleared according to the Clear Faults section. The warn bit does not automatically clear when the warn condition ceases.

The default IOUT_OC_WARN_LIMIT (I_{LIM}) value is set by the selection of $R_{IMON/ILIM}$.

Table 45. DEFAULT I_{VLY} WARN LIMIT SETTINGS

Threshold (A)	$R_{IMON/ILIM}$ (kΩ)		Data (h)
	Hiccup	Latch−Off	
10	10.0	56.2	E850
14	15.0	68.1	E870
20	18.2	82.5	E8A0
26	22.1	100	E800
32	27.4	121	E900
38	33.2	150	E930
46	39.2	182	E970
56	47.5	221	E9C0

OT_FAULT_LIMIT (Reg4Fh)

This command sets the temperature threshold (°C) for an over−temperature fault.

The OT_FAULT_LIMIT has 2 data bytes encoded in LINEAR11 format with 5bits exponent, 11 bits mantissa.

The exponent is read only. Writing any exponent other than −1 (11111b), an Invalid Data Fault is flagged.

The mantissa range is 80dec to 160dec. Writing any mantissa outside this range asserts an Invalid Data Fault.

Table 46. OT FAULT RANGE AND RESOLUTION

Range	Resolution	Default
80°C – 160°C	0.5°C	150°C

If the OT_FAULT_LIMIT is set lower than or equal to the OT_WARN_LIMIT threshold, an Invalid Data Fault sets.

Table 47. EXAMPLE OT_FAULT_LIMIT SETTINGS

Threshold (°C)	Data (h)		Threshold (°C)	Data (h)
80	F8A0		120	F8F0
90	F8B4		135	F90E
100	F8C8		**150**	**F92C**
105	F8D2		160	F940

OT_FAULT_RESPONSE (Reg50h)

This command instructs the device what action to take in response to an OT_FAULT_LIMIT event.

The device also:

- Sets the TEMP bit in the STATUS_BYTE
- Sets the Over−Temp fault bit in STATUS_TEMP
- Notifies the host by asserting ALERT#

Table 48. VALID OT_FAULT_RESPONSE SETTINGS

Bit	Name	Value	Description
7:6	Ignore, latch−off, or recover	**00**	Ignore. Device continues operation without interruption
		10	Device shuts down and responds according to the Restart Setting [5:3]
5:3	Restart Setting	**000**	Latch−off: device does not attempt restart. 56 kΩ < $R_{IMON/ILIM}$ ≤ 221 kΩ
		111	Hiccup: continuous periodic restart attempts at rate set by Restart Delay Time [2:0]. 10 kΩ ≤ $R_{IMON/ILIM}$ < 48 kΩ
2:0	Restart Delay Time	**000**	32 ms
		001	64 ms
		010	96 ms
		011	128 ms
		100	160 ms
		101	192 ms
		110	224 ms
		111	256 ms

Attempts to write data, other than shown in the table above, will result in an Invalid Data Fault.

Once the fault bit is set, it is latched and can only be cleared in accordance with the Clear Faults section. The fault bit does not automatically clear when the fault condition ceases.

OT_WARN_LIMIT (Reg51h)

This command instructs the device what action to take in response to an OT_WARN_LIMIT event.

The OT_WARN_LIMIT has 2 data bytes encoded in LINEAR11 format with 5bits exponent, 11bits mantissa.

The exponent is read only. Writing any exponent other than −1 (11111b), results in an Invalid Data Fault flag.

The mantissa range is 70dec to 170dec. Writing any mantissa outside this range asserts an Invalid Data Fault.

Table 49. OT_WARN_LIMIT RANGE AND RESOLUTION

Range	Resolution	Default
70°C – 150°C	0.5°C	130°C

If the OT_WARN_LIMIT is set higher than or equal to the OT_FAULT_LIMIT threshold, an Invalid Data Fault sets.

Table 50. EXAMPLE OT_WARN_LIMIT SETTINGS

Threshold (°C)	Data (h)		Threshold (°C)	Data (h)
80	F8A0		120	F8F0
90	F8B4		**130**	**F904**
100	F8C8		140	F918
110	F8DC		150	F92C

During an Over−Temp warn condition, the device also:

- Sets the TEMP bit in the STATUS_BYTE
- Sets the OT warn bit in STATUS_TEMPERATURE
- Notifies the host by asserting ALERT#, if not masked

VIN_OV_FAULT_LIMIT (Reg55h)

This command instructs the device what action to take when VIN exceeds the VIN _OV_FAULT_LIMIT.

VIN_OV_FAULT_LIMIT has 2 data bytes encoded in LINEAR11 format with 11bits mantissa and 5bits un−signed exponent.

The exponent is read only. Writing any exponent other than 0 (00000b), results in an Invalid Data Fault.

Table 51. VALID VIN_OV_FAULT_LIMIT SETTINGS

Threshold (V)	Data (h)		Threshold (V)	Data (h)
5	0005		13	000D
6	0006		14	000E
7	0007		15	000F
8	0008		16	0010
9	0009		17	0011
10	000A		**18**	**0012**
11	000B		19	0013
12	000C		20	0014

All supported options are shown in the table above. Attempts to write data other than shown in the table above will result in an Invalid Data Fault.

In a stacked/parallel application, the slaves ignore this threshold. Input OVP response fully controlled by the master.

VIN_OV_FAULT_RESPONSE (Reg56h)

This command instructs the device what action to take in the event of a VIN_OV_FAULT_LIMIT incursion.

The device also:

- Sets the VIN_OVP bit in the STATUS_WORD
- Sets the VIN_OV fault bit in STATUS_INPUT
- Notifies the host by asserting ALERT#

Table 52. VIN_OV_FAULT_RESPONSE SETTINGS

Bit	Name	Value	Description
7:6	Ignore, latch−off, or recover	**00**	Ignore. Device continues operation without interruption
		10	Device shuts down and responds according to the Restart Setting [5:3]
5:3	Restart Setting	**000**	Latch−off: device does not attempt restart. 56 kΩ < $R_{IMON/ILIM}$ ≤ 221 kΩ
		111	Hiccup: continuous periodic restart attempts at rate set by Restart Delay Time [2:0]. 10 kΩ ≤ $R_{IMON/ILIM}$ < 48 kΩ
2:0	Restart Delay Time	**000**	32 ms
		001	64 ms
		010	96 ms
		011	128 ms
		100	160 ms
		101	192 ms
		110	224 ms
		111	256 ms

Attempts to write data other than shown in the table above will result in an Invalid Data Fault.

Once the fault bit is set, it is latched and can only be cleared in accordance with the Clear Faults section. The fault bit does not automatically clear when the fault condition ceases.

POWER_GOOD_ON (Reg5Eh)

Sets the value at which the PGOOD pin asserts, indicating the output is in regulation.

Table 53. VALID POWER_GOOD_ON SETTINGS

Threshold (%V_{FB})	Data (h)		Threshold (%V_{FB})	Data (h)
84	00D7		92	00EC
86	00DC		94	00F1
88	00E1		96	00F6
90	**00E6**		98	00FB

Attempts to write data other than shown in the table above will result in an Invalid Data Fault.

If the POWER_GOOD_ON threshold is set at or below the POWER_GOOD_OFF threshold, an Invalid Data Fault is triggered.

POWER_GOOD_OFF (Reg5Fh)

This register sets the value at which the PGOOD pin de−asserts, indicating the output is not fully regulated.

Table 54. VALID POWER_GOOD_OFF SETTINGS

Threshold (%V_{FB})	Data (h)		Threshold (%V_{FB})	Data (h)
82	00D2		90	00E6
84	**00D7**		92	00EC
86	00DC		94	00F1
88	00E1		96	00F6

Attempts to write data other than shown in the table above will result in an Invalid Data Fault.

If the POWER_GOOD_OFF threshold is set at or above the POWER_GOOD_ON threshold, an Invalid Data Fault sets.

TON_DELAY (Reg60h)

This register sets the TON_DELAY time from receipt of a start condition until V_{OUT} starts rising.

The TON_DELAY command has 2 data bytes encoded in LINEAR11 format with 5bits un−signed exponent and 11bits mantissa.

Table 55. VALID TON_DELAY SETTINGS

Delay (ms)	Data (h)		Threshold (V)	Data (h)
1	**0001**		6	0006
2	0002		7	0007
3	0003		8	0008
4	0004		9	0009
5	0005		10	000A

Writing any mantissa (bit [10:4]) value not 00h will result in an Invalid Data Fault, as will writing the 0msec setting.

TON_RISE (Reg61h)

This register sets the time it takes the output to reach the regulation band.

The TON_RISE command has 2 data bytes encoded in LINEAR11 format with 5bits un−signed exponent and 11bits mantissa.

The exponent is read only. Writing any exponent other than 0 (00000b), results in an Invalid Data Fault flag.

Table 56. VALID TON_RISE SETTINGS

T_{RISE} (ms)	Data (h)		T_{RISE} (ms)	Data (h)
1	0001		11	000B
2	0002		12	000C
3	0003		13	000D
4	0004		14	000E
5	0005		15	000F
6	0006		16	0010
7	0007		17	0011
8	0008		18	0012
9	0009		19	0013
10	000A		20	0014

Writing any mantissa (bit [10:5]) to a value not 00h will result in an Invalid Data Fault, including writing the 0 ms setting.

The default value of this register is established by the $R_{SS/MODE1}$ value according to the table below:

Table 57. DEFAULT TON_RISE SETTING PER $R_{SS/MODE1}$

T_{RISE} (ms)	$R_{SS/MODE1}$ (kΩ)			Data (h)
	1 Scale	$^1/_2$ Scale	$^1/_4$ Scale	
1	10.0	33.2	82.5	0001
3	15.0	39.2	100	0003
5	18.2	47.5	121	0005
10	22.1	56.2	150	000A
15	27.4	68.1	182	000F
20			221	0014

TOFF_DELAY (Reg64h)

This register sets the TOFF_DELAY time from receipt of a stop condition until switching ceases.

The TOFF_DELAY command has 2 data bytes encoded in LINEAR11 format with 5bits un−signed exponent and 11bits mantissa.

The exponent is read only. Writing any exponent other than 0 (00000b), results in an Invalid Data Fault flag.

Any non−zero (00h) mantissa (bit [10:4]) written will assert an Invalid Data Fault.

Table 58. VALID TOFF_DELAY SETTINGS

Delay (ms)	Data (h)		Threshold (V)	Data (h)
0	**0000**		6	0006
1	0001		7	0007
2	0002		8	0008
3	0003		9	0009
4	0004		10	000A
5	0005			

TOFF_FALL (Reg65h)

This register sets the elapsed time from the end of TOFF_DELAY until the output is discharged.

The TOFF_FALL command has 2 data bytes encoded in LINEAR11 format with 5bits un−signed exponent and 11bits mantissa.

The exponent is read only. Writing any exponent other than 0 (00000b), results in an Invalid Data Fault flag.

Table 59. VALID TOFF_FALL SETTINGS

T_{FALL} (ms)	Data (h)		T_{FALL} (ms)	Data (h)
1	0001		11	000B
2	0002		12	000C
3	0003		13	000D
4	0004		14	000E
5	**0005**		15	000F
6	0006		16	0010
7	0007		17	0011
8	0008		18	0012
9	0009		19	0013
10	000A		20	0014

Writing any mantissa (bit [10:5]) value not 00h will result in an Invalid Data Fault, including writing the 0 ms setting.

STATUS_BYTE (Reg78h)

This command returns a summary of the critical faults in a single byte.

Table 60. CRITICAL FAULT SUMMARY BYTE

Bit	Support	Function
7	No	Busy: non−volatile memory being accessed for read/write.
6	Yes	OFF
5	Yes	VOUT_OVP Fault
4	Yes	IOUT_OCP Fault
3	No	VIN_UV Fault
2	Yes	TEMP Fault or Warning
1	Yes	CML: PEC failed or Invalid Data Fault
0	Yes	VIN_OVP, VIN_OFF, Thermal Shutdown, OCP_WARN, VOUT_UV fault, VOUT_UV warn, PGOOD fault, Master/Slave and Slave/Master faults

Un−supported bits (7, 3) return 0.

STATUS_WORD (Reg79h)

This command returns 2 bytes of information with the summary of critical faults. The lower byte of STATUS_WORD is the same as STATUS_BYTE.

The table below applies only to the upper of the 2 bytes:

Table 61. CRITICAL FAULT SUMMARY WORD

Bit	Support	Function
7	Yes	VOUT: all STATUS_VOUT
6	Yes	IOUT/POUT: OCP Fault, Average OCP warn.
5	Yes	INPUT: VIN_OVP fault, VIN_OFF fault
4	Yes	MFR: all STATUS_MFR
3	Yes	POWERGOOD#
2	No	FANS
1	No	Other
0	No	Unknown

Un−supported bits (2:0) return 0.
If V_{OUT} is in regulation, the POWERGOOD# bit clears real time − it is not latched until read. If V_{OUT} falls out of regulation, the POWERGOOD# bit sets real−time.

STATUS_VOUT (Reg7Ah)

This register returns a summary of VOUT faults in 1 byte.

Table 62. VOUT FAULT SUMMARY

Bit	Support	Function	ALERT Mask	
			Support	Default
7	Yes	VOUT_OV Fault	Yes	No Mask
6	Yes	VOUT_OV Warn	Yes	Mask
5	Yes	VOUT_UV Warn	Yes	Mask
4	Yes	VOUT_UV Fault	Yes	No Mask
3	Yes	VOUT_MAX or VOUT_MIN warn	Yes	Mask
2	No	TON_MAX Fault	No	NA
1	No	TON_MAX Warn	No	NA
0	No	VOUT Tracking Error	No	NA

Un−supported bits (2:0) return 0.

STATUS_IOUT (Reg7Bh)

This register returns a summary of IOUT faults in 1 byte.

Table 63. IOUT FAULT SUMMARY

Bit	Support	Function	ALERT Mask	
			Support	Default
7	Yes	IOUT_OC Fault	Yes	No Mask
6	No	IOUT_OC_LV Fault	No	NA
5	Yes	IOUT_OC Warn	Yes	Mask
4	No	IOUT_UC Fault	No	NA
3	No	Current Share Fault	No	NA
2	No	Power Limit mode	No	NA
1	No	POUT Fault	No	NA
0	No	POUT Warn	No	NA

Un−supported bits (6, 4:0) return 0.

STATUS_INPUT (Reg7Ch)

This register returns a summary of VIN faults in 1 byte.

Table 64. VIN FAULT SUMMARY

Bit	Support	Function	ALERT Mask	
			Support	Default
7	Yes	VIN_OV Fault	Yes	No Mask
6	No	VIN_OV Warn	No	NA
5	No	VIN_UV Warn	No	NA
4	No	VIN_UV Fault	No	NA
3	Yes	VIN_UVLO	Yes	No Mask
2	No	IIN_OCP Fault	No	NA
1	No	IIN_OCP Warn	No	NA
0	No	PIN Warn	No	NA

Un−supported bits (6:4, 2:0) return 0.

STATUS_TEMPERATURE (Reg7Dh)

This register returns a 1 byte summary of Temperature faults.

Table 65. TEMPERATURE FAULT SUMMARY

Bit	Support	Function	ALERT Mask	
			Support	Default
7	Yes	Over−Temp Fault	Yes	No Mask
6	Yes	Over−Temp Warn	Yes	Mask
5	No	Under−Temp Warn	No	NA
4	No	Under−Temp Fault	No	NA
3:0	No	Reserved	No	NA

Bit 5 and “reserved” bits (3:0) return 0.

STATUS_CML (Reg7Eh)

Register returns a 1 byte summary of the following faults:

Table 66. COMMUNICATION FAULT SUMMARY

Bit	Support	Function	ALERT Mask	
			Support	Default
7	Yes	Invalid Command Fault	Yes	No Mask
6	Yes	Invalid Data Fault	Yes	No Mask
5	Yes	PEC Fault	Yes	No Mask
4	No	Memory Fault	No	NA
3	No	Processor Fault	No	NA
2	No	Reserved	No	NA
1	No	Communication Fault, other	No	NA
0	No	Memory/Logic Fault, other	No	NA

Un−supported bits (4:0) return 0.

STATUS_MFR_SPECIFIC (Reg80h)

Register returns a 1 byte summary of the following faults:

Table 67. VENDOR SPECIFIC FAULT SUMMARY

Bit	Support	Function	ALERT Mask	
			Support	Default
7:5	No	Reserved	No	NA
4	Yes	Master to Slave OV Fault	Yes	No Mask
3	Yes	Thermal Shutdown	Yes	No Mask
2	Yes	Slave to Master Fault	Yes	No Mask
1:0	No	Reserved	No	NA

Un−supported bits (7:5, 1:0) return 0.

READ_VIN (Reg88h)

The READ_VIN command returns the measured input voltage (V_{IN}), in Volts.

Two data bytes are encoded in LINEAR11 format with 5bits signed exponent and 11bits mantissa. The exponent is fixed −5 (11011b).

Table 68. READ_VIN RANGE AND RESOLUTION

Range	Resolution
0 V − 32 V	31.25 mV

Table 69. EXAMPLE READ_VIN VALUES

V_{IN} (V)	Data (h)		V_{IN} (V)	Data (h)
6	D8C0		12	D980
9	D920		15	D9E0
10	D940		18	DA40

READ_VOUT (Reg8Bh)

The READ_VOUT command returns the measured output voltage (V_{OUT}), in Volts. Applies only to Master.

Table 70. READ_VOUT RANGE AND RESOLUTION

Range	Resolution
0 V − 5.5 V	3.90625 mV

Two data bytes are encoded in ULINEAR16 format, as shown below:

READ_VOUT FORMAT

Data Byte High								Data Byte Low							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Mantissa V															

Table 71. EXAMPLE READ_VOUT VALUES

V_{OUT} (V)	Data (h)		V_{OUT} (V)	Data (h)
0.8	00CD		1.8	01CD
1.0	0100		3.3	034D
1.2	0133		5.0	0500

READ_IOUT (Reg8Ch)

The READ_IOUT command returns the measured output current (I_{OUT}), in Amperes.

Table 72. READ_IOUT RANGE AND RESOLUTION

Range	Resolution
−64 A to 64 A	125 mA

Two data bytes are encoded in LINEAR11 format with 5bits signed exponent and 11bits mantissa. The exponent is fixed −3 (11101b).

Table 73. EXAMPLE READ_IOUT VALUES

I_{OUT} (A)	Data (h)		I_{OUT} (A)	Data (h)
−25	EF38		20	E8A0
−10	EFB0		30	E8F0
0	E800		40	E940
10	E850		50	E990

READ_TEMPERATURE (Reg8Dh)

This register returns measured internal device temperature.

Table 74. READ_TEMP RANGE AND RESOLUTION

Range	Resolution
−256°C − 256°C	0.5°C

Two data bytes are encoded in LINEAR11 format with 5bits signed exponent and 11bits signed mantissa. The exponent is fixed −1 (11111b).

Table 75. EXAMPLE READ_TEMP VALUES

IC Temp (°C)	Data (h)		IC Temp (°C)	Data (h)
−40	FFB0		50	F864
−20	FFD8		100	F8C8
0	F800		125	F8FA
25	F832		150	F92C

PMBUS_REVISION (Reg98h)

The PMBUS_REVISION register stores the revision of PMBUS to which the device is compliant.

This read only, 1 byte command indicates compliance to Part I (bits [7:4]) or Part II (bits [3:0]) of the PMBUS specification.

Table 76. PMBUS REVISION VALUES

Bits [7:4]	Part I Revision		Bits [3:0]	Part II Revision
0000b	1.0		0000b	1.0
0001b	1.1		0001b	1.1
0010b	1.2		0010b	1.2
0011b	**1.3**		**0011b**	**1.3**

NCP3286 is revision 1.3 compliant. PMBUS_REVISION reads back 33h.

MFR_VOUT_MIN (RegA4h)

This read only register contains the manufacturer specific minimum programmable VOUT value.

Two data bytes are encoded in ULINEAR16 with a fixed exponent of −8 (11000b).

Table 77. MFR_VOUT_MIN VALUE

V_{OUT}_MIN (V)	Data (h)
0.25	**0040**

MFR_VOUT_MAX (RegA5h)

This read only register contains the manufacturer specific maximum programmable VOUT value.

Two data bytes are encoded in ULINEAR16 with a fixed exponent of −8 (11000b).

Table 78. MFR_VOUT_MAX VALUE

V_{OUT}_MAX (V)	Data (h)
5.5	**0580**

IC_DEVICE_ID (RegADh)

The read only IC_DEVICE_ID register contains manufacturer specific type or part number information.

The Block Read format must be used to access this 2 byte read. The lower byte represents the number of bytes and is fixed to 1 (01h). The upper byte contains an encoded device identifier (86h).

Table 79. DEVICE IDENTIFICATION VALUE

DEVICE_ID	Data (h)
NCP3286	**8601**

IC_DEVICE_REV (RegAEh)

The read only IC_DEVICE_REV register contains manufacturer specific type or part number information.

The Block Read format must be used to access this 2 byte read. The lower byte represents the number of bytes and is fixed to 1 (01h). The upper byte contains the device revision.

Table 80. DEVICE REVISION VALUE

DEVICE_REV	Data (h)
XY	XY**01**

I_BALANCE_OFFSET (RegC4h)

This manufacturer unique command can be used to manually offset phase current in a multi−phase/stackable system.

Table 81. CURRENT BALANCE OFFSET RANGE/RESOLUTION

Range	Resolution	Default
−3.875 A to 3.875 A	125 mA	0 A

Two data bytes are encoded in LINEAR11 format. The exponent is fixed −3 (11101b). Mantissa bit [5] is the polarity bit (0 negative, 1 positive). Mantissa bits [4:0] are unsigned binary.

Table 82. EXAMPLE CURRENT BALANCE OFFSET VALUES

I_{OUT} (A)	Data (h)		I_{OUT} (A)	Data (h)
−2.50	E818		0.75	E826
−1.50	E80C		1.50	E82C
−1.00	E808		2.25	E831
0	**E800**		3.00	E838

If any exponent other than −3 (11101b) is written, an Invalid Data Fault is set. Writing any mantissa bit [10:6], other than 00000b, will also assert an Invalid Data Fault.

MFR_PMBUS_BASE (RegC5h)

This read only manufacturer specific command is used to set the base part of the PMBUS slave address.

The **default base address is 10h**.

The base address is added to the offset to set the full 7bit PMBUS slave address.

A 1% resistor at the ADDR/SFAULT pin ($R_{ADDR/SFAULT}$) determines the offset portion of the device slave address, per the following table:

Table 83. VALID PMBUS ADDRESS OFFSET VALUES

R_{ADDR} (kΩ)	PMBUS Address			
	Master	1st Slave	2nd Slave	3rd Slave
10.0	base+00h	base+01h	base+02h	base+03h
15.0	base+01h	base+02h	base+03h	base+04h
18.2	base+02h	base+03h	base+04h	base+05h
22.1	base+03h	base+04h	base+05h	base+06h
27.4	base+04h	base+05h	base+06h	base+07h
33.2	base+05h	base+06h	base+07h	base+08h
39.2	base+06h	base+07h	base+08h	base+09h
47.5	base+07h	base+08h	base+09h	base+0Ah
56.2	base+08h	base+09h	base+0Ah	base+0Bh
68.1	base+09h	base+0Ah	base+0Bh	base+0Ch
82.5	base+0Ah	base+0Bh	base+0Ch	base+0Dh
100	base+0Bh	base+0Ch	base+0Dh	base+0Eh
121	base+0Ch	base+0Dh	base+0Eh	base+0Fh
150	base+0Dh	base+0Eh	base+0Fh	base+10h
182	base+0Eh	base+0Fh	base+10h	base+11h
221	0Fh	0Fh	0Fh	0Fh

If base+offset exceeds 7Fh, fixed slave address 0Fh is used.

PMBUS DEVICE FAULT MANAGEMENT

Clearing Warn or Fault Bits

All warning or fault bits, except the PGOOD fault, set in the STATUS registers remain set, even if the warn/fault condition is no longer present, until one of the following occur:

- Bits are individually cleared.
- The device receives a CLEAR_FAULTS command.
- The output is commanded through the EN pin, the OPERATION command, or combination of both, to turn off, then back on.
- Bias power (VCC) is removed from the device.

Two exceptions to the rule that STATUS bits remain set are the OFF and POWERGOOD# bits. These bits always reflect the current state of the device and POWER_GOOD signal.

Clearing Individual Bits

Any or all fault bits in any status register except STATUS_BYTE and STATUS_WORD can be directly cleared by issuing the status command with 1 binary data byte. The binary data byte bits align with the associated status registers bits. To clear fault bits, write a 1 to the corresponding bit in the binary data byte. For example:

Table 84. EXAMPLE FAULT/STATUS BIT CLEARING

Data (b)	Description
0001 0000	Bit [4] is cleared. All others remain unchanged.
0110 0010	Bits [6], [5], and [1] are cleared. All others remain unchanged.
1111 1111	Writing FFh clears all bits in the specified register.

Clearing Bits in STATUS_BYTE or STATUS_WORD

Most bits in STATUS_BYTE and STATUS_WORD are cleared by clearing the bit or bits that caused the bits in STATUS_BYTE and STATUS_WORD to be set.

In general, STATUS_BYTE and STATUS_WORD are the logical OR of the bits in the lower level status register, as illustrated in the example below:

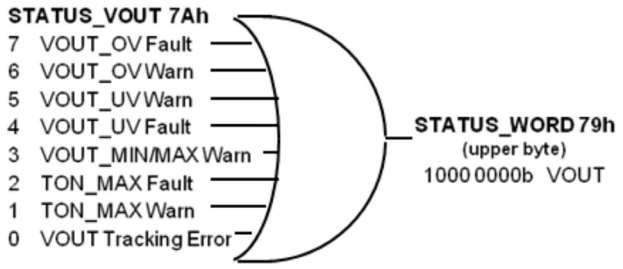


Figure 39.

For instance, if the VOUT_OV_Fault bit in the STATUS_VOUT register sets, then the VOUT bit in STATUS_WORD also sets. Similarly, when the VOUT_OV_Fault bit in STATUS_VOUT is cleared, the VOUT bit in STATUS_WORD also clears if no other bits in STATUS_VOUT were also set.

The OFF and POWERGOOD# bits cannot be cleared since they always reflect the real−time state of the device.

Fault/Warn Bit Re−Assertion

If a warning or fault condition persists once the bit is cleared, it will immediately be set again. ALERT# will also re−assert after the status bit is cleared. The SMBALERT_MASK command can be used to prevent ALERT# from asserting.

Conceptual View of Status Bit and ALERT# Operation

When a warning or fault event is detected, a latch is set. The latch's output becomes the status bit in one of the lower level status registers (STATUS_VOUT, for example). The latch output may also be used by itself or ORed with other status bits, to create the corresponding bit in STATUS_BYTE or STATUS_WORD, and to toggle ALERT# if not masked.

The output of the latch passes through a gate controlled by the corresponding SMBALERT_MASK bit. If the bit is set, the latch output is blocked from driving the SMBALERT# circuit. If the SMBALERT_MASK bit is not set, the latch output is allowed to drive the SMBALERT# circuit which drives the ALERT# pin.

When the SMBALERT# circuit detects the rising edge of the latch output, it asserts the SMBALERT# signal output low.

The SMBALERT# signal remains asserted until cleared. The signal clears when the device successfully transmits its address in response to receiving the Alert Response Address. It may also be cleared by a CLEAR_FAULTS command.

The latch can also be cleared by writing a 1 to the corresponding bit in the status register.

The bit clearing commands act as pulses internally, momentarily driving the latch's reset pin. By implication, if the fault/warn condition persists (event detector remains active), the latch output will immediately set again once cleared. As described above, this will cause an un−masked SMBALERT# to re−assert if it has been previously cleared. The host may not be able to detect the momentary clearing of status bits.

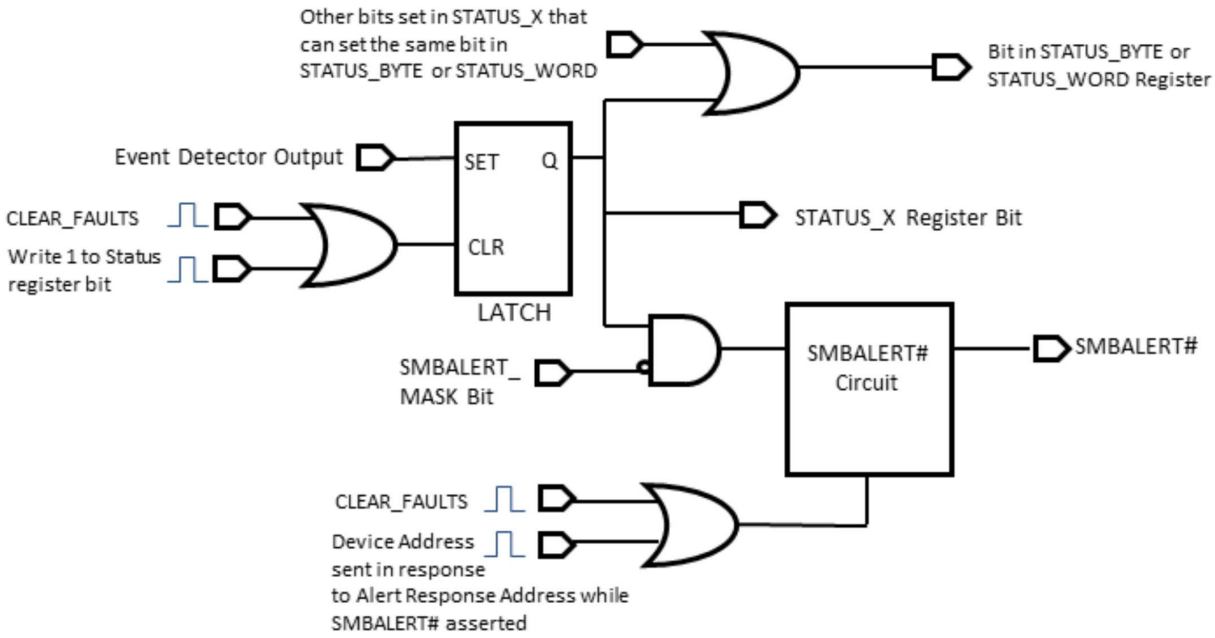


Figure 40. Status Bits and SMBALERT# Conceptual Schematic

PCB LAYOUT GUIDELINE

Good electrical layout is key to ensure proper operation, high efficiency, and noise reduction.

- *Bias Decoupling*: Place the decoupling caps as close as possible to the controller's VCC and VDRV pins. The VCC pin filter resistor should be <2.2 Ω to prevent a large voltage drop.
- *Input Supply Decoupling*: Place and route the input capacitors to maintain the shortest possible current loop length to reduce parasitic inductance, input voltage spikes, and noise emission. Commonly, a low ESL MLCC capacitor is placed adjacent to the PVIN and PGND pins for high frequency noise reduction.
- *Power Paths*: Use the widest and shortest possible traces for high current paths such as PVIN, VOUT, SW, and PGND to minimize series ESL and ESR. ESR contributes to power losses and temperature rise.
- *Switching Node*: The SW, PHASE, and BST pins contain high−voltage discontinuous switching waveforms with sharp edges. Care should be taken to avoid capacitive coupling to sensitive signals like FB, VSNS−, and COMP. Avoid routing these sensitive signals adjacent to or over/under on adjacent layers without GND shields, to the discontinuous switching signals.
  It is recommended to add RC snubber component locations to the PCB design should these be required to provide additional damping for peak SW voltages. The snubber devices should be placed adjacent to the IC, between SW and GND.
- *Bootstrap*: The bootstrap capacitor (C_{BST}) and series resistor (R_{BST}) should be connected directly between the BST and PHASE pins using a low impedance path. It is not necessary to establish a connection between PHASE and SW, as this is already accomplished within the IC. The series resistor is used for limiting peak SW voltages to safe levels, particularly at elevated V_{IN} levels. R_{BST} works similar to a RC snubber by slowing the switching edges, which may also be used, although either can negatively impact efficiency.
- *Voltage Sense*: Use a Kelvin sense pair to route from the FB and VSNS− pins to the remote sense point. The pair is best routed over solid GND plane, if possible. Avoid routing adjacent to switching nodes or other noise sources.
- *Compensation Network*: All components of the RC network connected to FB and COMP should be placed as close as possible to the IC pins with care to avoid routing traces adjacent to noise sources.
- *Ground*: Directly connect the exposed PGND pad to the GND plane using multiple vias. The use of multiple system GND planes is recommended.
  Connect AGND pin to the system GND plane at a single location, near the IC's AGND pin, using a robust, low impedance path.
- *Master/Slave Signals*: In a multi−phase/stacked system, master and slave interconnections should be routed using low impedance traces avoiding switching noise sources. This is particularly important for the COMP signal.
- *Thermal Layout Considerations*:
  Ensure the large exposed pad (DAP) under the IC, is securely soldered.
  Improved heat spreading can be achieved by using multiple GND layers with liberally applied thermal vias around the IC connected to those GND planes.
  Use large copper pours (areas), where possible, to improve thermal conduction and radiation.
  Keep the inductor away from the IC to distribute heats sources and reduce vicinity heating.

ORDERING INFORMATION

Device	Current	Package	Shipping†
NCP3286MNTXG	40 A	WQFN34, 5 x 7 mm (Pb−Free)	3000 units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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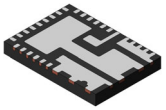
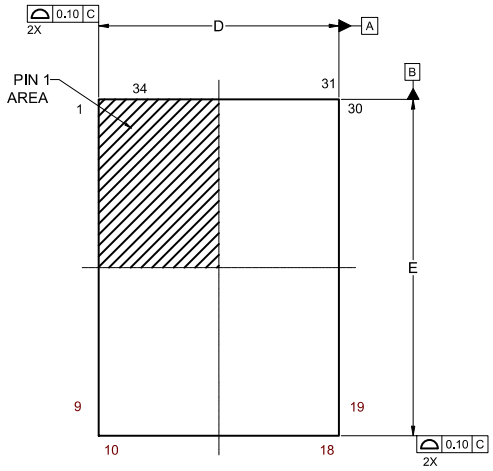
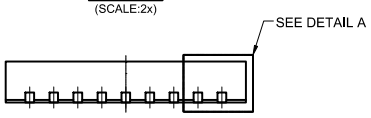


WQFN−34 5.00x7.00x0.75, 0.50P
CASE 510CL
ISSUE E

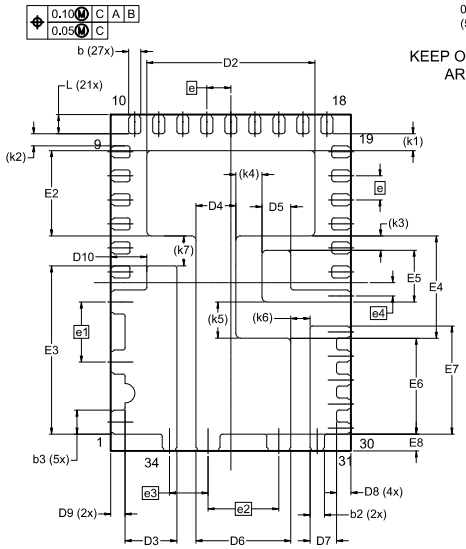
DATE 08 JUN 2026



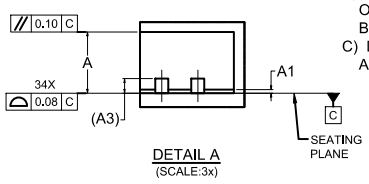
TOP VIEW
(SCALE:2x)



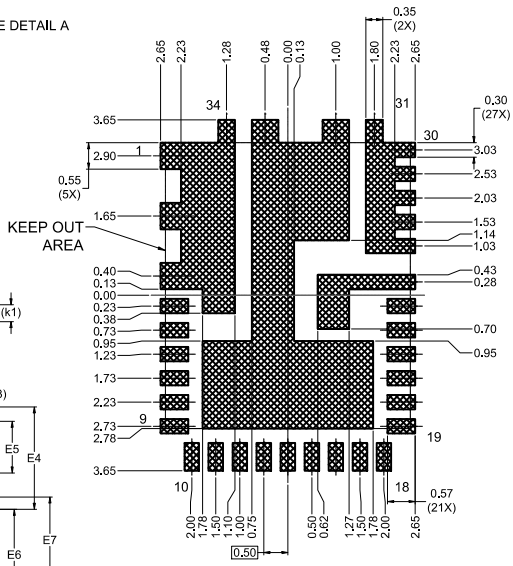
FRONT VIEW
(SCALE:2x)



BOTTOM VIEW
(SCALE:2x)



DETAIL A
(SCALE:3x)



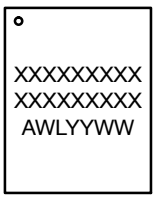
LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES: UNLESS OTHERWISE SPECIFIED
A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	–	0.50
A3		0.20 REF	
b	0.20	0.25	0.30
b2	0.25	0.30	0.35
b3	0.40	0.50	0.60
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
D3	0.98	1.08	1.18
D4	0.73	0.83	0.93
D5	0.50	0.60	0.70
D6	1.87	1.97	2.07
D7	0.45	0.55	0.65
D8	0.20	0.30	0.40
D9	0.20	0.30	0.40
D10	0.65	0.75	0.85
E	6.90	7.00	7.10
E2	1.68	1.78	1.88
E3	3.40	3.50	3.60
E4	2.03	2.13	2.23
E5	0.98	1.08	1.18
E6	1.89	1.99	2.09
E7	2.15	2.25	2.35
E8	0.25	0.35	0.45
e		0.50 BSC	
e1		1.25 BSC	
e2		1.47 BSC	
e3		0.80 BSC	
e4		0.275BSC	
k1		0.35 REF	
k2		0.25 REF	
k3		0.30 REF	
k4		0.54 REF	
k5		0.75 REF	
k6		0.40 REF	
k7		0.63 REF	
L	0.30	0.40	0.50

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WQFN−34 5.00x7.00x0.75, 0.50P**		**PAGE 1 OF 1**

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