

# LDO Regulator, 0.5 A, High Accuracy (0.7%), Adjustable, Low Noise, High PSRR with Power Good

## NCP189

The NCP189 is a 0.5 A LDO, next generation of high PSRR, low noise and low dropout regulators with Power Good open collector output. Designed to meet the requirements of RF and sensitive analog circuits, the NCP189 device provides low noise, high PSRR and low quiescent current while offering the ability to regulate output voltages down to 0.6 V. The device also offers excellent load / line transients. The NCP189 is designed to work with a 4.7  $\mu$ F input and output ceramic capacitor. It is available in industry standard WDFNW6 0.65P, 2 mm x 2 mm.

### Features

- Operating Input Voltage Range: 1.6 V to 5.5 V
- Available in Fixed Voltage Option: 0.6 V to 5.0 V
- Adjustable Version Reference Voltage: 0.6 V
- $\pm 0.7\%$  Initial Accuracy at 25°C
- $\pm 1\%$  Accuracy Over Load and Temperature
- Low Quiescent Current Typ. 35  $\mu$ A
- Shutdown Current: Typ. 0.1  $\mu$ A
- Very Low Dropout: Typ. 65 mV at 500 mA for 3.3 V Variant
- High PSRR: Typ. 85 dB at 100 mA, f = 1 kHz
- Low Noise: 10  $\mu$ V<sub>RMS</sub> (Fixed Version)
- Stable with a 4.7  $\mu$ F Small Case Size Ceramic Capacitors
- Controlled Output Voltage Slew Rate from 5 mV /  $\mu$ s
- Available in WDFNW6 2 mm x 2 mm x 0.75 mm Case 511DW
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Communication Systems
- In-Vehicle Networking
- Telematics, Infotainment and Clusters
- General Purpose Automotive

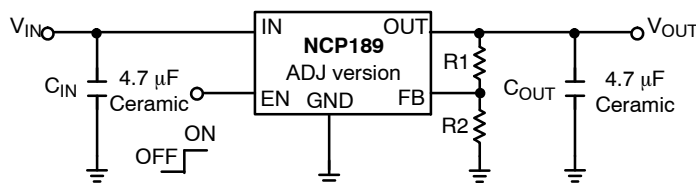
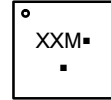


Figure 1. Typical Application Schematics

### MARKING DIAGRAMS

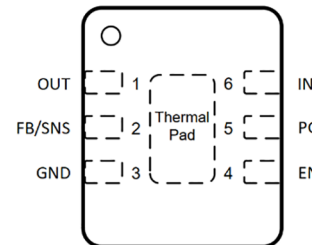


WDFNW6 2x2, 0.65P  
CASE 511DW



XXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
M = Month Code  
Y = Year  
W = Work Week  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### PIN CONNECTONS



### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 11 of this data sheet.

# NCP189

## PIN FUNCTION DESCRIPTION

Pin No. WDFNW6	Pin Name	Description
1	OUT	Regulated output voltage. The output should be bypassed with small 4.7 $\mu$ F ceramic capacitor
6	IN	Input voltage supply pin
4	EN	Chip enable: Applying $V_{EN} < 0.4$ V disables the regulator, Pulling $V_{EN} > 1$ V enables the LDO
5	PG	Power Good, open collector. Use 10 k $\Omega$ to 100 k $\Omega$ pull-up resistor connected to output or input voltage
3	GND	Common ground connection
2	FB	Adjustable output feedback pin (for adjustable version only)
2	SNS	Sense feedback pin. Must be connected to OUT pin on PCB (for fixed versions only)
PAD	PAD	Expose pad should be tied to ground plane for better power dissipation

## ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	$V_{IN}$	-0.3 to 6	V
Output Voltage	$V_{OUT}$	-0.3 to $V_{IN} + 0.3$ , max. 6	V
Chip Enable Input	$V_{EN}$	-0.3 to 6	V
Power Good Voltage	$V_{PG}$	-0.3 to 6	V
Power Good Current	$I_{PG}$	20	mA
Output Short Circuit Duration	$t_{SC}$	unlimited	s
Maximum Junction Temperature	$T_J$	150	$^{\circ}$ C
Storage Temperature	$T_{STG}$	-55 to 150	$^{\circ}$ C
ESD Capability, Human Body Model (Note 2)	$ESD_{HBM}$	2000	V
ESD Capability, Charged Device Model (Note 2)	$ESD_{CDM}$	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:  
 ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)  
 ESD Charged Device Model tested per EIA/JESD22-C101, Field Induced Charge Model

# NCP189

## THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
<b>Thermal Characteristics, WDFNW6-2x2, 0.65 Pitch Package</b>			
Thermal Resistance, Junction-to-Ambient (Note 3)	R $\theta$ JA	60	°C/W
Thermal Resistance, Junction-to-Case (top)	R $\theta$ JC(top)	167	°C/W
Thermal Resistance, Junction-to-Case (bottom) (Note 4)	R $\theta$ JC(bot)	6.9	°C/W
Thermal Resistance, Junction-to-Board	R $\theta$ JB	6.6	°C/W
Characterization Parameter, Junction-to-Top	$\Psi$ JT	4.6	°C/W
Characterization Parameter, Junction-to-Board	$\Psi$ JB	6.5	°C/W

- The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a high-K board (2s2p, 1in<sup>2</sup>, 1oz Cu) following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51-2a.
- The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30-88.

## ELECTRICAL CHARACTERISTICS

-40°C ≤ T<sub>J</sub> ≤ 125°C; V<sub>IN</sub> = V<sub>OUT(NOM)</sub> + 0.5 V or 1.6 V, whichever is greater, I<sub>OUT</sub> = 1 mA, C<sub>IN</sub> = C<sub>OUT</sub> = 4.7 μF, V<sub>EN</sub> = V<sub>IN</sub>, unless otherwise noted. Typical values are at T<sub>J</sub> = +25°C (Note 5).

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	
Operating Input Voltage	V <sub>IN</sub>		1.6	-	5.5	V	
Under Voltage Lock Out	V <sub>UVLO</sub>		-	1.5	-	V	
Output Voltage Accuracy	V <sub>OUT</sub>	V <sub>IN</sub> = V <sub>OUT(NOM)</sub> + 0.5 V, I <sub>OUT</sub> = 1 mA T <sub>J</sub> = +25°C	-0.7	V <sub>NOM</sub>	+0.7	%	
		V <sub>IN</sub> = V <sub>OUT(NOM)</sub> + 0.5 V to 5.5 V, 0.1 mA ≤ I <sub>OUT</sub> ≤ 0.5 A	-1	V <sub>NOM</sub>	+1	%	
Reference Voltage (Adjustable Ver. FB pin connected to OUT)	V <sub>FB</sub>	V <sub>IN</sub> = 1.6 V to 5.5 V, 0.1 mA ≤ I <sub>OUT</sub> ≤ 0.5 A	0.594	0.6	0.606	V	
Line Regulation	Line <sub>Reg</sub>	V <sub>OUT(NOM)</sub> + 0.5 V ≤ V <sub>IN</sub> ≤ 5.5 V	-	0.5	-	mV/V	
Load Regulation	Load <sub>Reg</sub>	I <sub>OUT</sub> = 1 mA to 0.5 A	-	2	-	mV	
Dropout Voltage (Note 5)	V <sub>DO</sub>	I <sub>OUT</sub> = 500 mA	V <sub>OUT(NOM)</sub> = 1.5 V	-	109	175	mV
			V <sub>OUT(NOM)</sub> = 1.8 V	-	93	152	
			V <sub>OUT(NOM)</sub> = 2.5 V	-	74	121	
			V <sub>OUT(NOM)</sub> = 2.8 V	-	69	113	
			V <sub>OUT(NOM)</sub> = 3.0 V	-	67	110	
			V <sub>OUT(NOM)</sub> = 3.3 V	-	65	108	
			V <sub>OUT(NOM)</sub> = 5.0 V	-	58	95	
Output Current Limit	I <sub>CL</sub>	V <sub>OUT</sub> = 90% V <sub>OUT(NOM)</sub>	-	750	850	mA	
Short Circuit Current	I <sub>SC</sub>	V <sub>OUT</sub> = 0 V	-	750	-		
Quiescent Current	I <sub>Q</sub>	I <sub>OUT</sub> = 0 mA	-	35	55	μA	
Shutdown Current	I <sub>DIS</sub>	V <sub>EN</sub> ≤ 0.4 V, T <sub>J</sub> ≤ 125°C	-	0.1	3.5	μA	
EN Pin Threshold Voltage	V <sub>ENH</sub>	EN Input Voltage "H"	1	-	V <sub>IN</sub>	V	
	V <sub>ENL</sub>	EN Input Voltage "L"	0	-	0.4		
EN Pull Down Current	I <sub>EN</sub>	V <sub>EN</sub> = 5 V	-	0.2	0.6	μA	
Power Good Threshold Voltage	V <sub>PGUP</sub>	Output Voltage Raising	-	95	-	%	
	V <sub>PGDW</sub>	Output Voltage Falling	-	90	-		
Power Good Output Voltage Low	V <sub>PGLO</sub>	I <sub>PG</sub> = 1 mA, Open drain	-	30	100	mV	
Turn-On Delay Time		C <sub>OUT</sub> = 4.7 μF, From assertion of V <sub>EN</sub> to V <sub>OUT</sub> start raise	-	85	-	μs	

# NCP189

## ELECTRICAL CHARACTERISTICS (continued)

$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ;  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.6\text{ V}$ , whichever is greater,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = C_{OUT} = 4.7\text{ }\mu\text{F}$ ,  $V_{EN} = V_{IN}$ , unless otherwise noted. Typical values are at  $T_J = +25^{\circ}\text{C}$  (Note 5).

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	
Slew Rate Time ("C" option)		$C_{OUT} = 4.7\text{ }\mu\text{F}$ , From assertion of $V_{EN}$ to $V_{OUT} = 95\% V_{OUT(NOM)}$	–	5	–	mV/ $\mu\text{s}$	
Slew Rate Time ("D" option)		$C_{OUT} = 4.7\text{ }\mu\text{F}$ , From assertion of $V_{EN}$ to $V_{OUT} = 95\% V_{OUT(NOM)}$	–	10	–	mV/ $\mu\text{s}$	
Slew Rate Time ("E" option)		$C_{OUT} = 4.7\text{ }\mu\text{F}$ , From assertion of $V_{EN}$ to $V_{OUT} = 95\% V_{OUT(NOM)}$	–	30	–	mV/ $\mu\text{s}$	
Slew Rate Time ("F" option)		$C_{OUT} = 4.7\text{ }\mu\text{F}$ , From assertion of $V_{EN}$ to $V_{OUT} = 95\% V_{OUT(NOM)}$	–	100	–	mV/ $\mu\text{s}$	
Power Supply Rejection Ratio	PSRR	$V_{OUT(NOM)} = 3.3\text{ V}$ , $I_{OUT} = 100\text{ mA}$	f = 1 kHz	–	85	–	dB
			f = 10 kHz	–	75	–	
			f = 100 kHz	–	53	–	
			f = 1 MHz	–	40	–	
Output Voltage Noise (Fixed Ver.)	$V_N$	f = 10 Hz to 100 kHz	$I_{OUT} = 100\text{ mA}$	–	10	–	$\mu\text{V}_{\text{RMS}}$
Thermal Shutdown Threshold	$T_{SDH}$	Temperature rising		–	165	–	$^{\circ}\text{C}$
	$T_{HYST}$	Temperature hysteresis		–	15	–	$^{\circ}\text{C}$
Active Output Discharge Resistance	$R_{DIS}$	$V_{EN} < 0.4\text{ V}$ , AD Version only		–	250	–	$\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at  $T_A = 25^{\circ}\text{C}$ .

Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.

6. Dropout voltage is characterized when  $V_{OUT}$  falls 3% below  $V_{OUT(NOM)}$ .

7. Guaranteed by design.

TYPICAL CHARACTERISTICS

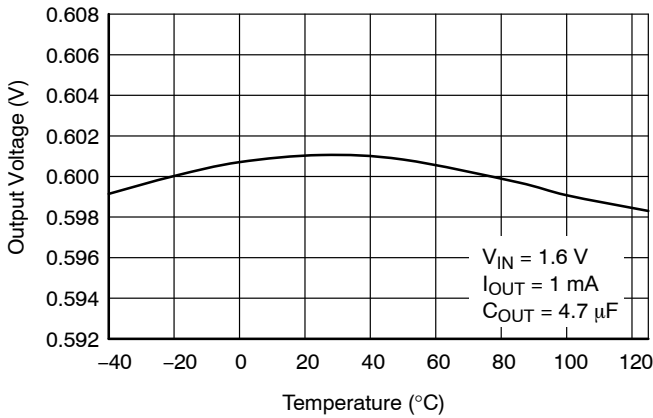


Figure 2. Output Voltage vs. Temperature –  $V_{OUT} = 0.6\text{ V}$  (Adjustable Reference)

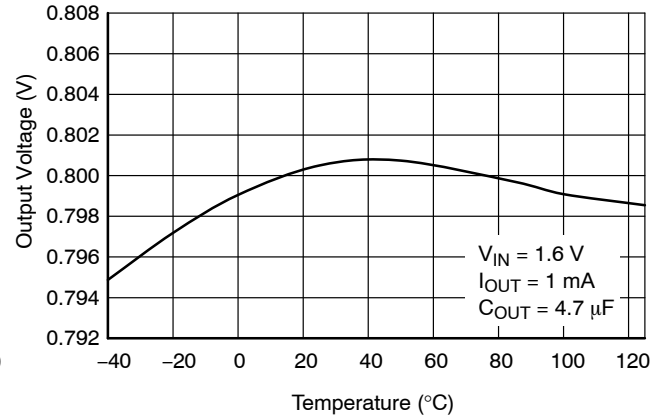


Figure 3. Output Voltage vs. Temperature –  $V_{OUT} = 0.8\text{ V}$

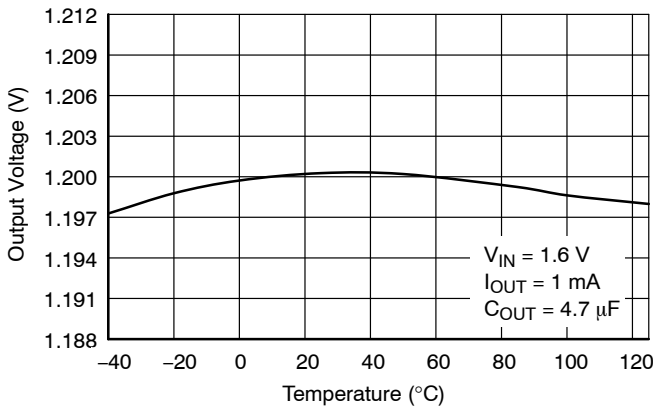


Figure 4. Output Voltage vs. Temperature –  $V_{OUT} = 1.2\text{ V}$

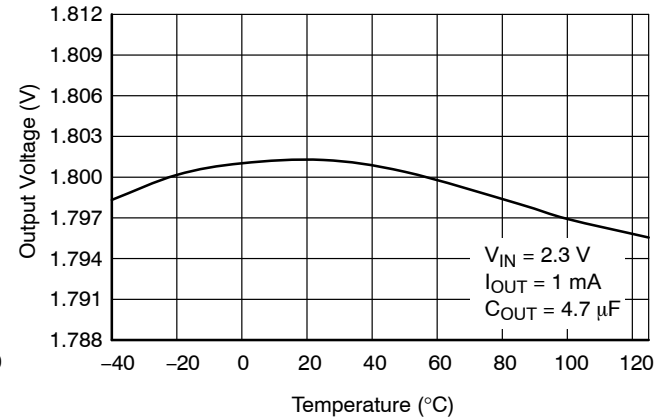


Figure 5. Output Voltage vs. Temperature –  $V_{OUT} = 1.8\text{ V}$

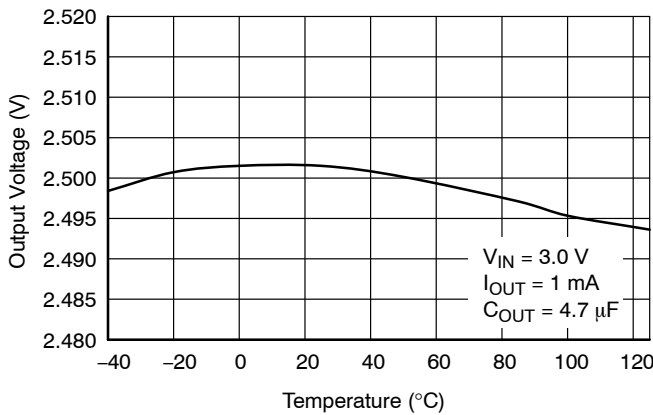


Figure 6. Output Voltage vs. Temperature –  $V_{OUT} = 2.5\text{ V}$

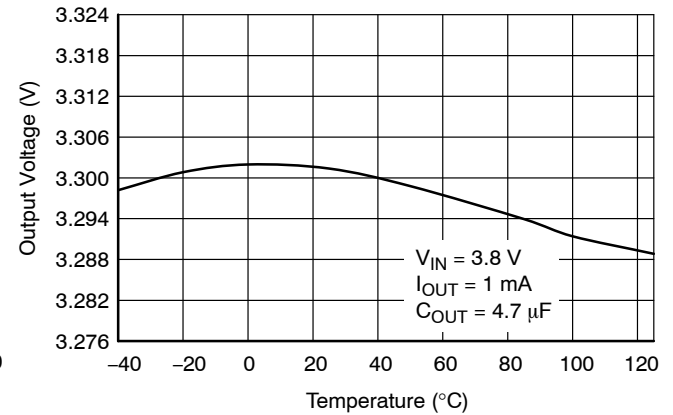


Figure 7. Output Voltage vs. Temperature –  $V_{OUT} = 3.3\text{ V}$

TYPICAL CHARACTERISTICS (continued)

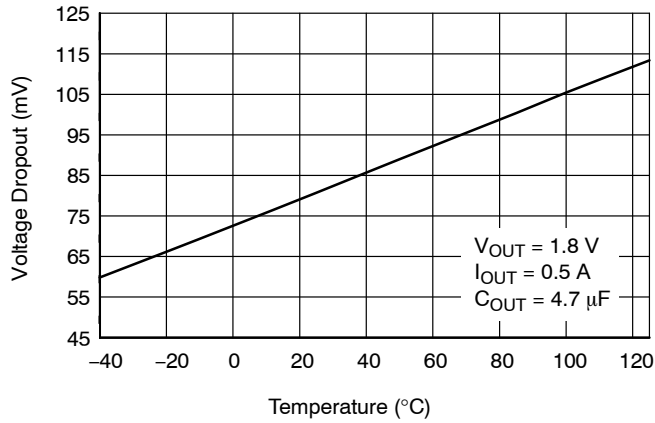


Figure 8. Dropout Voltage vs. Temperature -  $V_{OUT} = 1.8\text{ V}$

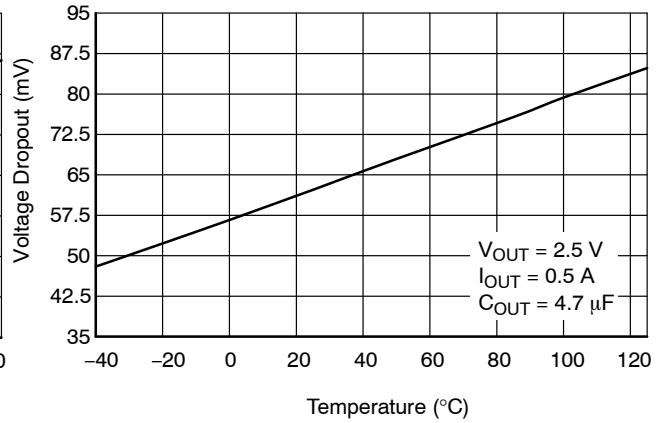


Figure 9. Dropout Voltage vs. Temperature -  $V_{OUT} = 2.5\text{ V}$

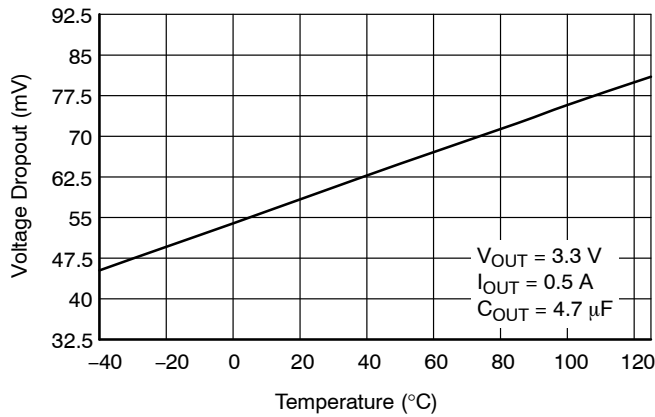


Figure 10. Dropout Voltage vs. Temperature -  $V_{OUT} = 3.3\text{ V}$

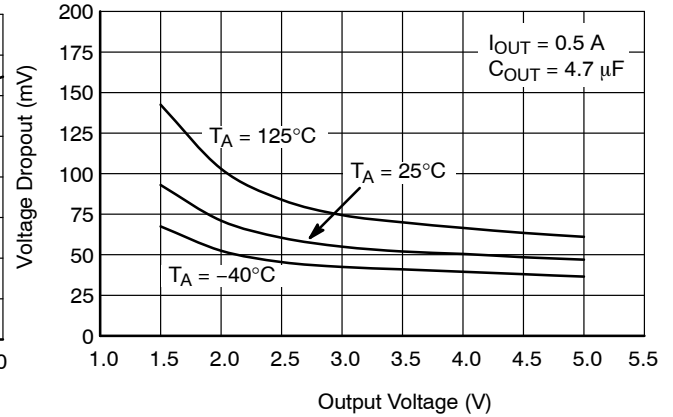


Figure 11. Dropout Voltage vs. Output Voltage

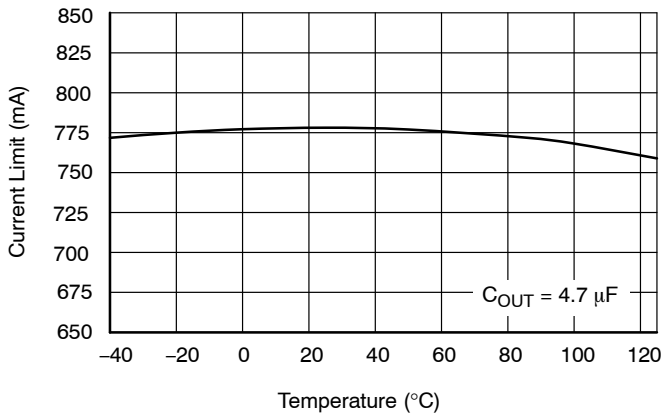


Figure 12. Current Limit vs. Temperature

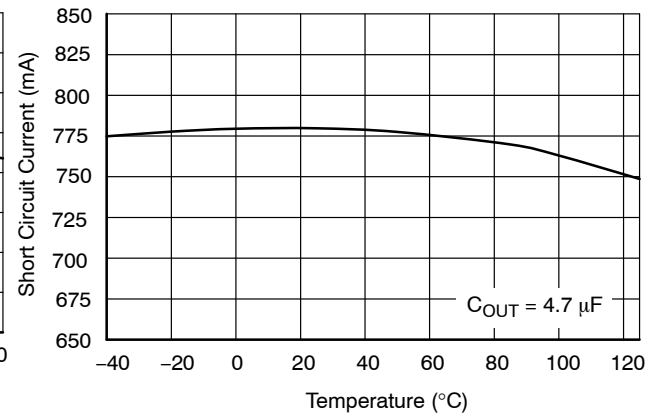


Figure 13. Short Circuit Current vs. Temperature

TYPICAL CHARACTERISTICS (continued)

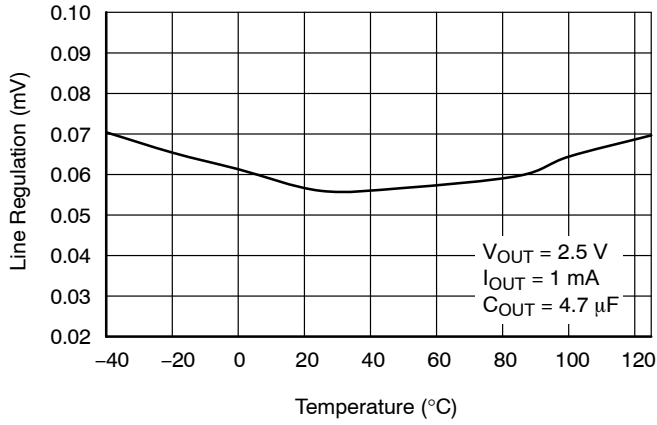


Figure 14. Line Regulation vs. Temperature

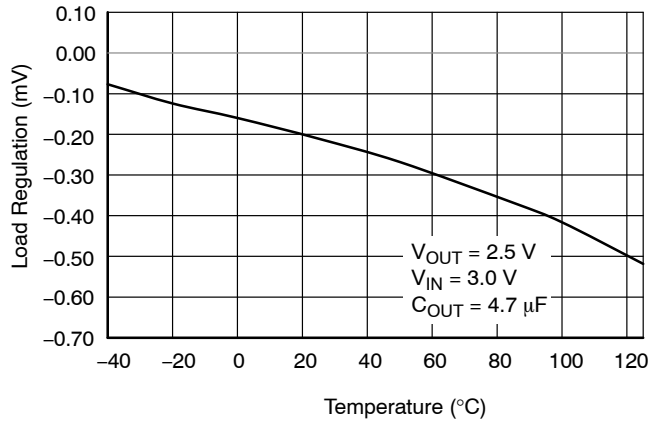


Figure 15. Load Regulation vs. Temperature

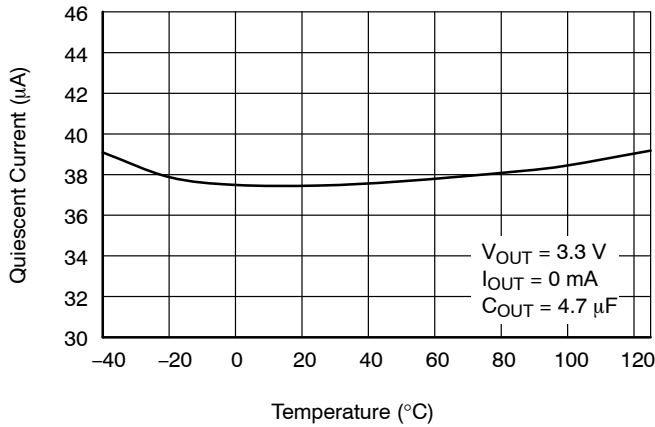


Figure 16. Quiescent Current vs. Temperature

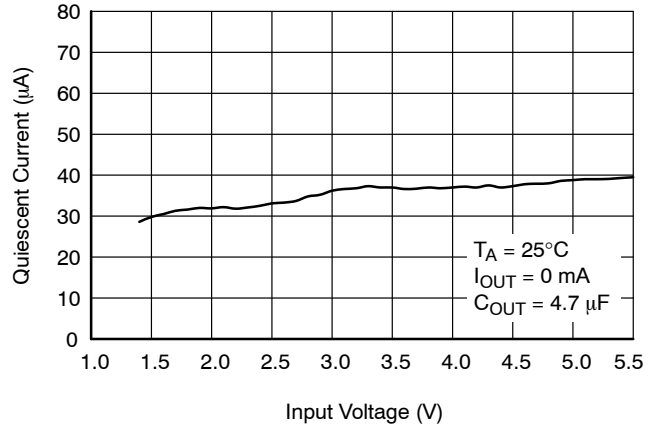


Figure 17. Quiescent Current vs. Input Voltage

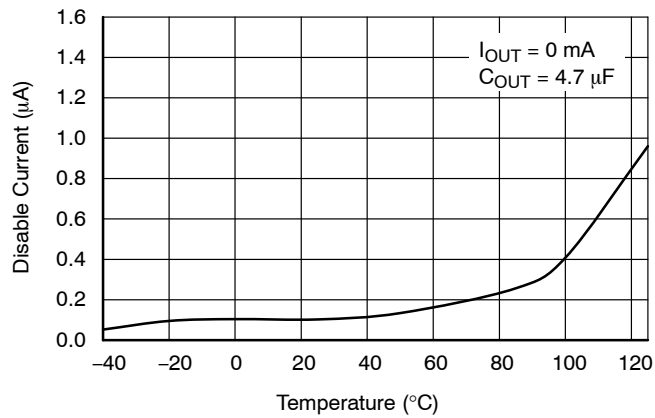


Figure 18. Disable Current vs. Temperature

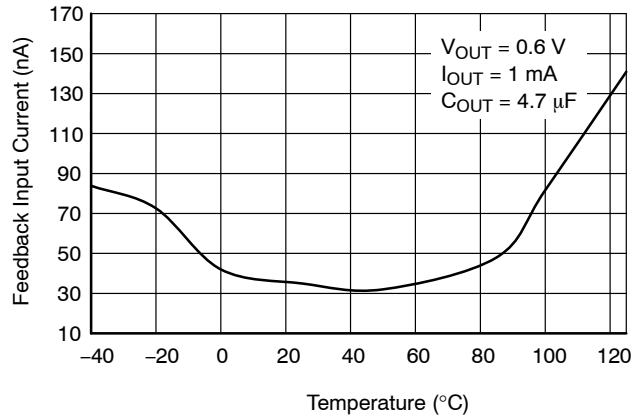


Figure 19. Feedback Input Current vs. Temperature (Adjustable Option)

TYPICAL CHARACTERISTICS (continued)

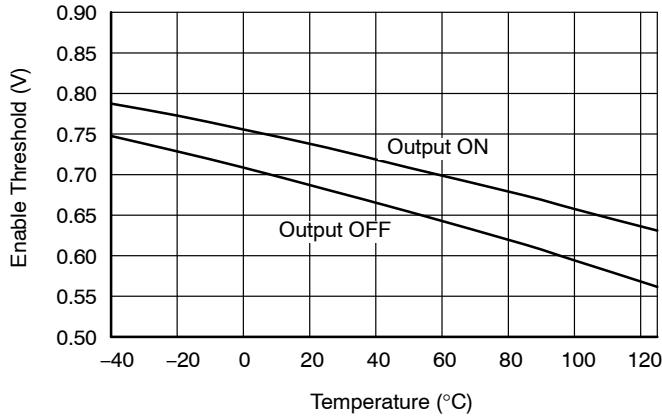


Figure 20. Enable Threshold vs. Temperature

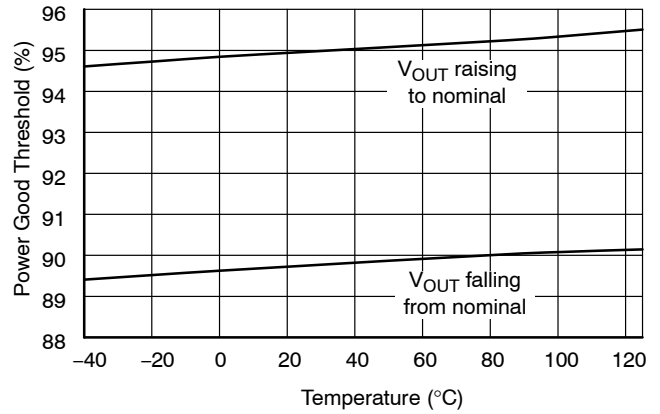


Figure 21. Power Good Threshold vs. Temperature

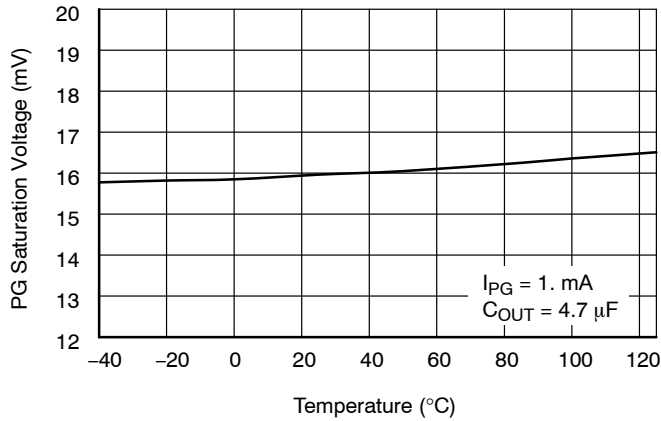


Figure 22. Power Good Saturation Voltage vs. Temperature

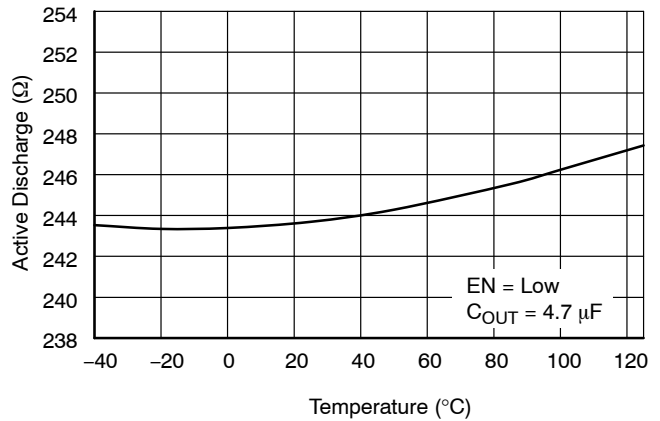


Figure 23. Active Discharge Resistance vs. Temperature

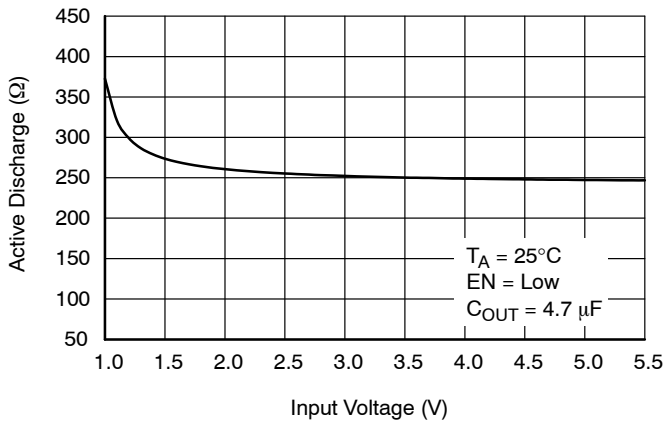


Figure 24. Active Discharge Resistance vs. Input Voltage

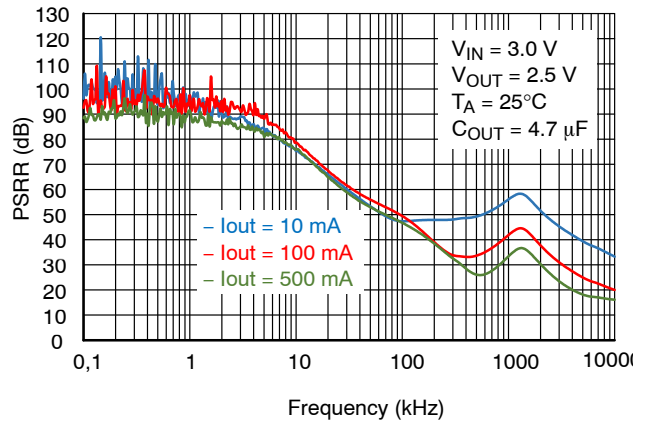


Figure 25. Power Supply Rejection Ratio for  $V_{OUT} = 2.5\text{ V}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$

## TYPICAL CHARACTERISTICS (continued)

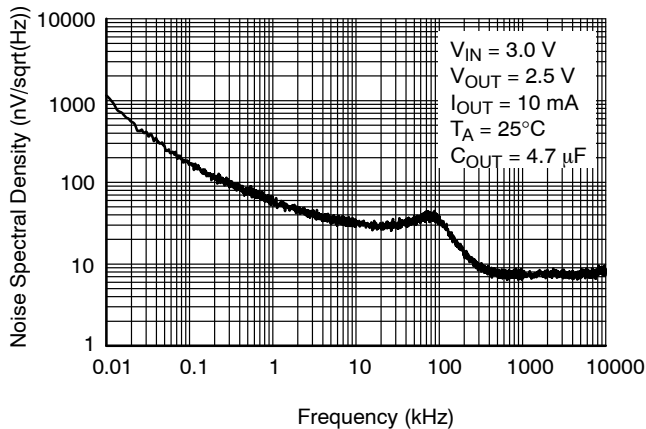


Figure 26. Output Voltage Noise Spectral Density for  $V_{OUT} = 2.5\text{ V}$ ,  $C_{OUT} = 4.7\ \mu\text{F}$

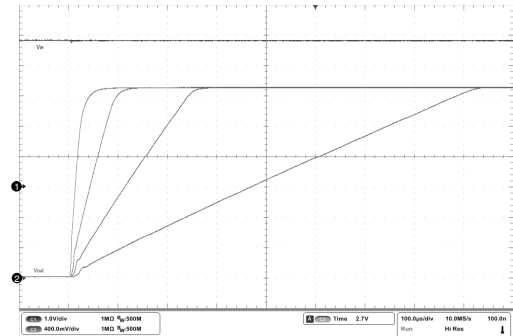


Figure 27. Controlled Output Voltage Slew Rate

## APPLICATIONS INFORMATION

The NCP189 is the member of new family of high output current and low dropout regulators which delivers low quiescent and ground current consumption, good noise and power supply ripple rejection performance. The NCP189 incorporates EN pin and power good output for simple controlling by MCU or logic. Standard features include current limiting, soft-start feature and thermal protection.

**Input Decoupling ( $C_{IN}$ )**

It is recommended to connect at least  $4.7\ \mu\text{F}$  ceramic X5R or X7R capacitor between IN and GND pin of the device. This capacitor will provide a low impedance path for any unwanted AC signals or noise superimposed onto constant input voltage. The good input capacitor will limit the influence of input trace inductances and source resistance during sudden load current changes. Higher capacitance and lower ESR capacitors will improve the overall line transient response.

**Output Decoupling ( $C_{OUT}$ )**

The NCP189 does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The device is designed to be stable with standard ceramics capacitors with values of  $2.2\ \mu\text{F}$  or greater. For the best performance and stability under all conditions (temperature, output current load etc.) is recommended to use  $4.7\ \mu\text{F}$  or higher capacitor. The X5R and X7R types have the lowest capacitance variations over temperature thus they are suitable. Please note that too high output capacity (for example  $100\ \mu\text{F}$  and more) may cause instability under some conditions, especially under very light load condition.

**Power Good Output Connection**

The NCP189 include Power Good functionality for better interfacing to MCU system. Power Good output is open collector type, capable to sink up to 10 mA. Recommended operating current is between  $10\ \mu\text{A}$  and 1 mA to obtain low saturation voltage. External pull-up resistor can be connected to any voltage up to 5.5 V (please see Absolute Maximum Ratings table above).

Please note that Power Good internal circuitry is non-functional (disabled) to achieve the lowest possible internal current consumption in case of disabled LDO through Enable input (EN = Low). In this case internal Power Good transistor is open and output logic level is defined by voltage used for pull-up resistor. When Power Good is intended to be used as part of power sequencing functionality, then please connect external pull-up resistor to output voltage of NCP189. This will allow you to get correct low PG signal when LDO is disabled. Active discharge option is recommended to discharge output capacitors connected to LDO.

Power Good signal is internally delayed avoiding reaction to short glitches in output voltage. Blanking time is about  $9\ \mu\text{s}$  when voltage is decreasing from nominal value and about  $18\ \mu\text{s}$  when voltage is increasing back to nominal value.

**Controlled Output Voltage Slew Rate**

The NCP189 has internal output voltage slew rate control (see Figure 27). After enable event there is about  $85\ \mu\text{s}$  dead time required to proper start-up of all internal LDO blocks. When this time ends, output voltage starts to raise

monotonously from zero to nominal output voltage. Total time need to settle LDO output on nominal voltage is given by voltage option and slew rate. Customer can choose from 4 available options – 5 mV/μs, 10 mV/μs, 30 mV/μs and 100 mV/μs.

In case of adjustable application please remember that selected slew rate is controlled for voltage raise from 0 V to reference voltage. It means that slew rate is multiplied by  $V_{out} / V_{ref}$  ratio.

**Power Dissipation and Heat Sinking**

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C, however device is capable to work up to junction temperature +150°C (in range from +125°C to +150°C parameters are not guaranteed). The maximum power dissipation the NCP189 can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}} \quad (eq. 1)$$

The power dissipated by the NCP189 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}(I_{GND} + I_{OUT}) + I_{OUT}(V_{IN} - V_{OUT}) \quad (eq. 2)$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + (V_{OUT} \times I_{OUT})}{I_{OUT} + I_{GND}} \quad (eq. 3)$$

**Hints**

$V_{IN}$  and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCP189, and make traces as short as possible.

**Adjustable Version**

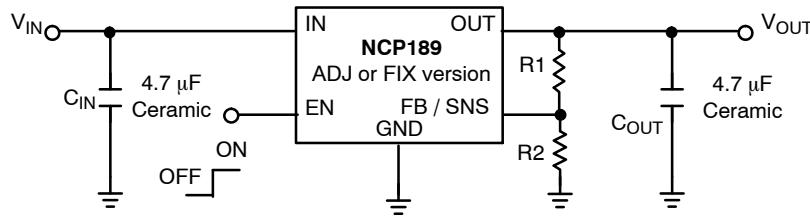
In case customer needs non-standard / special voltage option, but output noise is critical too, there is one option. In such case customer can use fixed version and connect external resistor divider between output voltage and SNS pin. Under such condition, original fixed voltage becomes reference voltage for resistor divider and feedback loop. Output voltage can be equal or higher than original fixed option, while possible range is from 0.6 V up to 5.0 V. Figure 28 shows how to add external resistors to increase output voltage above fixed value.

Output voltage is then given by equation

$$V_{OUT} = V_{FIX} * (1 + R/R2) \quad (eq. 4)$$

where  $V_{FIX}$  is voltage of original fixed version (from 0.6 V up to 5.0 V) or adjustable version (0.6 V). Do not operate the device at output voltage about 5.2 V, as device can be damaged.

Typical current flowing into FB pin is below 200 nA (adjustable option), where current flowing into SNS pin is below 900 nA (fixed options). In order to avoid influence of this current to output voltage accuracy, it is recommended use values of R1 and R2 in range from 1 kΩ to 220 kΩ.



**Figure 28. Adjustable Variant Application**

Please note that output noise is amplified by  $V_{OUT} / V_{FIX}$  or  $V_{OUT} / V_{FB}$  ratio. For example, if original 0.6 V adjustable variant is used to create non-standard 3.6 V output voltage, output noise is increased  $3.6 / 0.6 = 6$  times and real noise value will be  $6 * 10 \mu V_{rms} = 60 \mu V_{rms}$ .

For noise sensitive applications it is recommended to use as high fixed variant as possible – for example in case above it is better to use 3.3 V fixed variant to create 3.6 V output voltage, as output noise will be amplified only  $3.6 / 3.3 = 1.09x$  ( $10.9 \mu V_{rms}$ ).

# NCP189

## ORDERING INFORMATION

Device part no. *	Voltage Option	Marking	Option	Package	Shipping†
NCP189CMTWADJTAG	ADJ	AE	With Active Output Discharge, Slew Rate 5 mV/μs	WDFNW6 2x2 (Pb-Free)	3000 / Tape & Reel
NCP189CMTWADJTBG	ADJ	AE	With Active Output Discharge, Slew Rate 5 mV/μs	WDFNW6 2x2 (Pb-Free)	3000 / Tape & Reel
NCP189CMTW120TAG	1.2 V	AA	With Active Output Discharge, Slew Rate 5 mV/μs	WDFNW6 2x2 (Pb-Free)	3000 / Tape & Reel
NCP189CMTW180TAG	1.8 V	AC	With Active Output Discharge, Slew Rate 5 mV/μs	WDFNW6 2x2 (Pb-Free)	3000 / Tape & Reel
NCP189CMTW330TAG	3.3 V	AD	With Active Output Discharge, Slew Rate 5 mV/μs	WDFNW6 2x2 (Pb-Free)	3000 / Tape & Reel

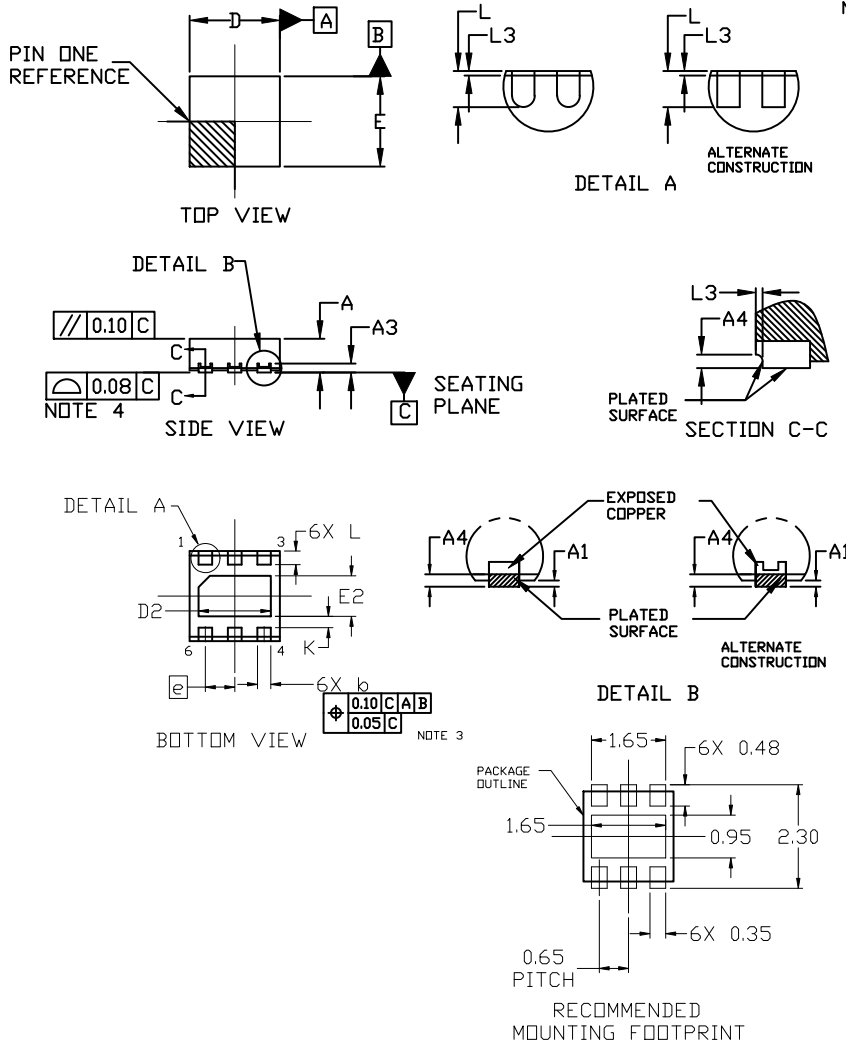
\*Other voltage options and slew rate options (D / E / F) upon request.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# NCP189

## PACKAGE DIMENSIONS

### WDFNW6 2x2, 0.65P CASE 511DW ISSUE B



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	---	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.80	0.90	1.00
e	0.65 BSC		
K	0.25 REF		
L	0.25	0.30	0.35
L3	0.05 REF		

onsemi, Onsemi, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi does not convey any license under any of its intellectual property rights nor the rights of others. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application, Buyer shall indemnify and hold onsemi and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that onsemi was negligent regarding the design or manufacture of the part. onsemi is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:  
 Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
 onsemi Website: [www.onsemi.com](http://www.onsemi.com)

ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)  
 For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)