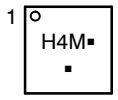
3.3 V Programmable OmniClock Generator

with Single Ended LVCMOS Output

NB3H60113GH4

WDFN8
CASE 511AT

MARKING DIAGRAM



H4 = Specific Device Code
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

The NB3H60113GH4, which is a member of the OmniClock family, is a one−time programmable (OTP), low power PLL−based clock generator that supports output frequency of 39.6 MHz. The device accepts fundamental mode parallel resonant crystal frequency of 19.8 MHz as input. It generates one single ended LVCMOS output. The output signals can be modulated using the spread spectrum feature of the PLL (programmable spread spectrum type, deviation and rate) for applications demanding low electromagnetic interference (EMI). The device can be powered down using the Power Down pin (PD#). It is possible to program the internal input crystal load capacitance and the output drive current provided by the device. The device also has automatic gain control (crystal power limiting) circuitry which avoids the device overdriving the external crystal.

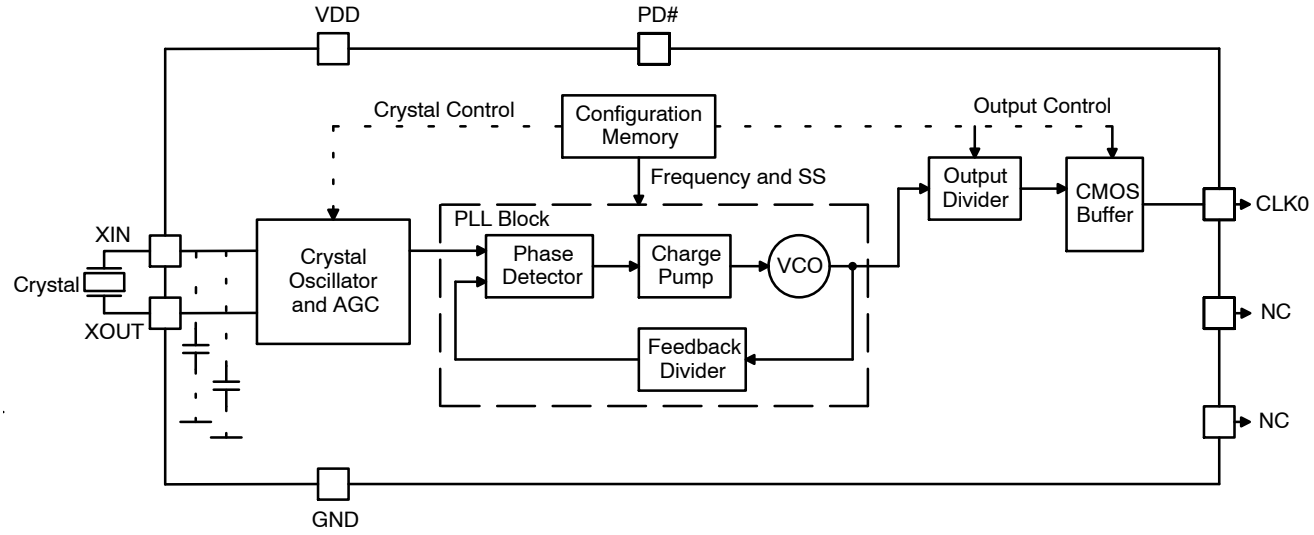
Features

- Member of the OmniClock Family of Programmable Clock Generators
- Operating Power Supply: 3.3 V ± 10%
- I/O Standards
  - Inputs: Fundamental Mode Crystal
  - Output: LVCMOS
- 1 Programmable Single Ended LVCMOS Output of 39.6 MHz
- Input Frequency Range
  - Crystal: 19.8 MHz
- Configurable Spread Spectrum Frequency Modulation Parameters (Type, Deviation, Rate)
- Programmable Internal Crystal Load Capacitors
- Programmable Output Drive Current for Single Ended Outputs
- Temperature Range −40°C to 85°C
- Packaged in 8−Pin WDFN
- These are Pb−Free Devices

Typical Applications

- Industrial Applications

BLOCK DIAGRAM



Notes:
1. CLK0 configured to be one single−ended LVCMOS output.
2. Dotted lines are the programmable control signals to internal IC blocks.
3. PD# has internal pull down resistor.

Figure 1. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

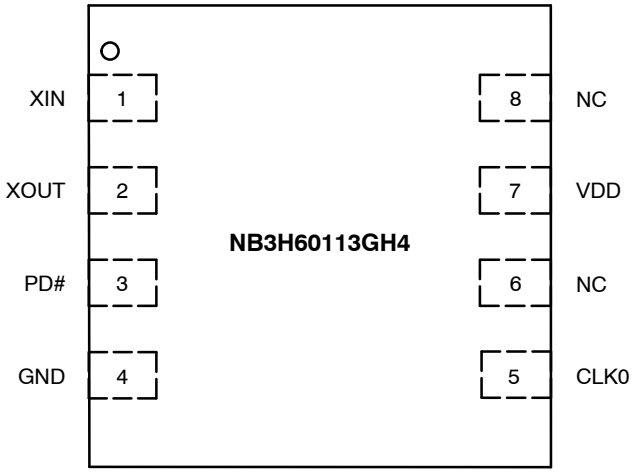


Figure 2. Pin Connections (Top View) – WDFN8

Table 1. PIN DESCRIPTION

Pin No.	Pin Name	Pin Type	Description
1	XIN	Input	19.8 MHz crystal input connection
2	XOUT	Output	Crystal output.
3	PD#	Input	Asynchronous LVCMOS input. Active Low Master Reset to disable the device and set outputs Low. Internal pull−down resistor. This pin needs to be pulled High for normal operation of the chip.
4	GND	Ground	Power supply ground
5	CLK0	Single Ended Output	Supports 39.6 MHz Single−Ended LVCMOS signals The single ended output will be LOW and will be complementary LOW/HIGH until the PLL has locked and the frequency has stabilized.
6	NC	SE Output	Not used. To be left open floating.
7	VDD	Power	3.3 V power supply
8	NC	SE Output	Not used. To be left open floating.

Table 2. POWER DOWN FUNCTION TABLE

PD#	Function
0	Device Powered Down
1	Device Powered Up

TYPICAL CRYSTAL PARAMETERS

Crystal: Fundamental Mode Parallel Resonant
Frequency: 19.8 MHz

Table 3. MAX CRYSTAL LOAD CAPACITORS RECOMMENDATION

Crystal Frequency Range	Max Cap Value
12 MHz – 27 MHz	20 pF

Shunt Capacitance (C0): 12 pF (Max)
Equivalent Series Resistance (ESR): 60 Ω (Max)

FUNCTIONAL DESCRIPTION

The NB3H60113GH4 is a 3.3 V programmable, single ended clock generator, designed to meet the clock requirements for industrial markets. It has a small package size and it requires low power during operation and while in standby. This device provides the ability to configure a number of parameters as detailed in the following section. The One−Time Programmable memory allows programming and storing of one configuration in the memory space.

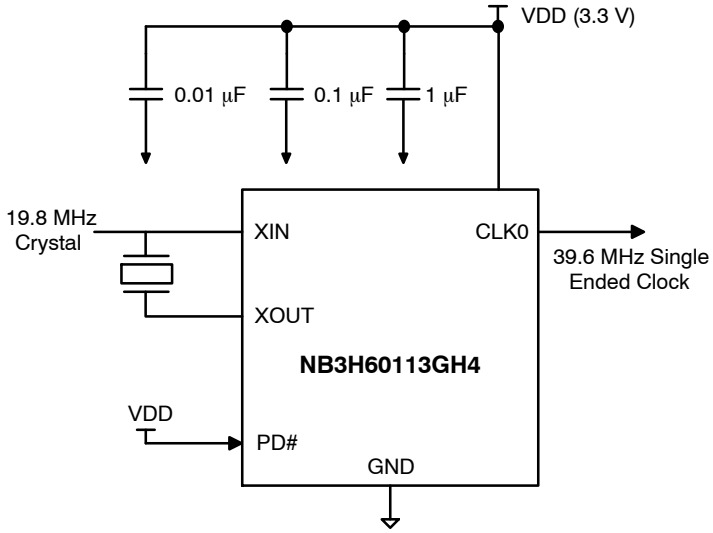


Figure 3. Power Supply Noise Suppression

Power Supply

Device Supply

The NB3H60113GH4 is designed to work with a 3.3 V VDD power supply. In order to suppress power supply noise it is recommended to connect decoupling capacitors of 0.1 μF and 0.01 μF close to the VDD pin as shown in Figure 3.

Clock Input

Input Frequency

The clock input block can be programmed to use a fundamental mode crystal 19.8 MHz. When using output frequency modulation for EMI reduction, for optimal performance, it is recommended to use crystals with frequency more than 6.75 MHz as input. Crystals with ESR values of up to 150 Ω are supported. When using a crystal input, it is important to set crystal load capacitor values correctly to achieve good performance.

Programmable Crystal Load Capacitors

The provision of internal programmable crystal load capacitors eliminates the necessity of external load capacitors for standard crystals. The internal load capacitor can be programmed to any value between 4.36 pF and 20.39 pF with a step size of 0.05 pF. Refer to Table 3 for recommended maximum load capacitor values for stable operation. There are three modes of loading the crystal – with internal chip capacitors only, with external capacitors only or with the both internal and external capacitors. Check with the crystal vendor's load capacitance specification for setting of the internal load capacitors. The minimum value of 4.36 pF internal load capacitor need to be considered while selecting external capacitor value. These will be bypassed when using an external reference clock.

Automatic Gain Control (AGC)

The Automatic Gain Control (AGC) feature adjusts the gain to the input clock based on its signal strength to maintain a good quality input clock signal level. This feature takes care of low clock swings fed from external reference clocks and ensures proper device operation. It also enables maximum compatibility with crystals from different manufacturers, processes, quality and performance. AGC also takes care of the power dissipation in the crystal; avoids over driving the crystal and thus extending the crystal life. In order to calculate the AGC gain accurately and avoid increasing the jitter on the output clocks, the user needs to provide crystal load capacitance as well as other crystal parameters like ESR and shunt capacitance (C0).

Programmable Clock Outputs

Output Type and Frequency

The NB3H60113GH4 provides one independent single ended LVCMOS output. The device supports any single ended output with frequency modulation. It should be noted that certain combinations of output frequencies and spread spectrum configurations may not be recommended for optimal and stable operation.

Programmable Output Drive

The drive strength or output current of the LVCMOS clock output is programmable. For V_{DD} of 3.3 V four distinct levels of LVCMOS output drive strengths can be selected and here max drive is selected.

Spread Spectrum Frequency Modulation

Spread spectrum is a technique using frequency modulation to achieve lower peak electromagnetic interference (EMI). It is an elegant solution compared to techniques of filtering and shielding. The NB3H60113GH4 modulates the output of its PLL in order to “spread” the bandwidth of the synthesized clock, decreasing the peak amplitude at the center frequency and at the frequency’s harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum modulation’. Refer Figure 4.

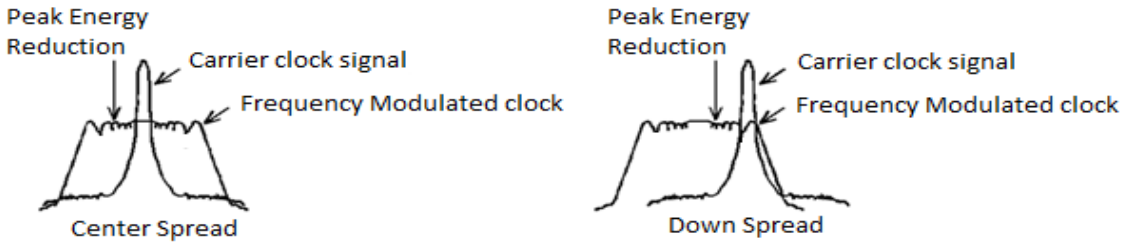


Figure 4. Frequency Modulation or Spread Spectrum Clock for EMI Reduction

The outputs of the NB3H60113GH4 is programmed to have center spread of ±1%. Additionally, the frequency modulation rate is also programmable. Frequency modulation of 30 kHz is selected. Spread spectrum, when on, applies to all the outputs of the device. There exists a tradeoff between the input clock frequency and the desired spread spectrum profile. For certain combinations of input frequency and modulation rate, the device operation could be unstable and should be avoided. For spread spectrum applications, the following limits are recommended:

Fin (Min) = 6.75 MHz

Fmod (range) = 30 kHz to 130 kHz

Fmod (Max) = Fin / 225

For any input frequency selected, above limits must be observed for a good spread spectrum profile.

Control Inputs

Power Down

Power saving mode can be activated through the power down PD# input pin. This input is an LVCMOS active Low Master Reset that disables the device and sets outputs Low. By default it has an internal pull−down resistor. The chip functions are disabled by default and when PD# pin is pulled high the chip functions are activated.

Configuration Space

NB3H60113GH4 has one Configuration. Table 4 shows the example of device configuration.

Table 4. PROGRAMMED CONFIGURATION

Input Frequency	Output Frequency	VDD	SS%	SS Mod Rate	Output Enable	Output Drive
19.8 MHz	CLK0 = 39.6 MHz	3.3 V	±1%	30 kHz	CLK0 = Y	CLK0 = 16 mA

Table 5. ATTRIBUTES

Characteristic	Value
ESD Protection Human Body Model	2 kV
Internal Input Default State Pull up/ down Resistor	50 kΩ
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)	MSL1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	130 k
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 6. ABSOLUTE MAXIMUM RATING (Note 2)

Symbol	Parameter		Rating	Unit
VDD	Positive power supply with respect to Ground		−0.5 to +4.6	V
V_I, V_O	Input/Output Voltage with respect to chip ground		−0.5 to VDD + 0.5	V
T_A	Operating Ambient Temperature Range (Industrial Grade)		−40 to +85	°C
T_{STG}	Storage temperature		−65 to +150	°C
T_{SOL}	Max. Soldering Temperature (10 sec)		265	°C
θ_{JA}	Thermal Resistance (Junction−to−ambient) (Note 3)	0 lfpm 500 lfpm	129 84	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−case)		35 to 40	°C/W
T_J	Junction temperature		125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power). ESD51.7 type board. Back side Copper heat spreader area 100 sq mm, 2 oz (0.070 mm) copper thickness.

Table 7. RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Core Power Supply Voltage	3.3 V operation	2.97	3.3	3.63	V
CL	Clock output load capacitance for LVCMOS clock	f_{out} < 100 MHz			15	pF
fclkin	Crystal Input Frequency	Fundamental Crystal		19.8		MHz
C_X	XIN / XOUT pin stray Capacitance	Note 4		4.5		pF
C_{XL}	Crystal Load Capacitance			10		pF
ESR	Crystal ESR				60	Ω

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. The XIN / XOUT pin stray capacitance needs to be subtracted from crystal load capacitance (along with PCB and trace capacitance) while selecting appropriate load for the crystal in order to get minimum ppm error.

Table 8. DC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3 V ± 10%, GND = 0 V, T_A = −40°C to 85°C, Notes 5, 6)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{DD\_3.3\ V}$	Power Supply current	Configuration Dependent. V_{DD} = 3.3 V, T_A = 25°C, XTAL = 19.8 MHz CLK0 = 39.6 MHz, 16 mA output drive		26		mA
I_{PD}	Power Down Supply Current	PD# is Low to make all outputs OFF			20	μA
V_{IH}	Input HIGH Voltage	Pin XIN	0.65 V_{DD}		V_{DD}	V
		Pin PD#	0.85 V_{DD}		V_{DD}	
V_{IL}	Input LOW Voltage	Pin XIN	0		0.35 V_{DD}	V
		Pin PD#	0		0.15 V_{DD}	
Zo	Nominal Output Impedance	Configuration Dependent. 16 mA drive		22		Ω
$R_{PUP/PD}$	Internal Pull up/ Pull down resistor	V_{DD} = 3.3 V		50		kΩ
Cprog	Programmable Internal Crystal Load Capacitance	Configuration Dependent	4.36		20.39	pF
	Programmable Internal Crystal Load Capacitance Resolution			0.05		pF
Cin	Input Capacitance	Pin PD#		4	6	pF
LVCMOS OUTPUT						
V_{OH}	Output HIGH Voltage	V_{DD} = 3.3 V I_{OH} = 16 mA	0.75*V_{DD}			V
V_{OL}	Output LOW Voltage	V_{DD} = 3.3 V I_{OL} = 16 mA			0.25*V_{DD}	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Measurement taken with single ended clock outputs terminated with test load capacitance of 5 pF and 15 pF. See Figure 6.
6. Parameter guaranteed by design verification not tested in production.

Table 9. AC ELECTRICAL CHARACTERISTICS
(V_{DD} = 3.3 V ± 10%; GND = 0 V, T_A = −40°C to 85°C, Notes 7, 8 and 10)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fout	Single Ended Output Frequency			39.6		MHz
f_{MOD}	Spread Spectrum Modulation Rate	fclkin ≥ 6.75 MHz		30		kHz
SS	Percent Spread Spectrum (deviation from nominal frequency)	Center Spread		±1		%
SSC_{RED}	Spectral Reduction, 3rd harmonic	@SS = ±1%, f_{out} = 39.6 MHz, fclkin = 19.8 MHz crystal, RES BW at 30 kHz, LVCMOS Output		−10		dB
t_{PU}	Stabilization time from Power−up	V_{DD} = 3.3 V with Frequency Modulation		3.0		ms
t_{PD}	Stabilization time from Power Down	Time from falling edge on PD# pin to tri−stated outputs (Asynchronous)		3.0		ms
Eppm	Synthesis Error	Configuration Dependent		0		ppm

SINGLE ENDED OUTPUTS (V_{DD} = 3.3 V ±10%, T_A = −40°C to 85°C, Notes 7, 8 and 10)

$t_{JITTER-3.3\ V}$	Period Jitter Peak−to−Peak	Configuration Dependent. 19.8 MHz xtal input , f_{out} = 39.6 MHz, SS off (Notes 9, 10 and 11, see Figure 8)		100		ps
	Cycle−Cycle Peak Jitter	Configuration Dependent. 19.8 MHz xtal input, f_{out} = 39.6 MHz, SS off (Notes 9, 10 and 11, see Figure 8)		100		
t_r / $t_{f\ 3.3\ V}$	Rise/Fall Time	Measured between 20% to 80% with 15 pF load, f_{out} = 39.6 MHz, V_{DD} = 3.3 V, Max Drive		1		ns
t_{DC}	Output Clock Duty Cycle	V_{DD} = 3.3 V Duty Cycle of Ref clock is 50% PLL Clock	45	50	55	%

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Parameter guaranteed by design verification not tested in production.
8. Measurement taken from single ended clock terminated with test load capacitance of 5 pF and 15 pF. See Figures 5, 6 and 7.
9. Measurement taken from single−ended waveform
10. AC performance parameters like jitter change based on the output frequency, spread selection, power supply and loading conditions of the output. For application specific AC performance parameters, please contact **onsemi**.
11. Period jitter Sampled with 10000 cycles, Cycle−cycle jitter sampled with 1000 cycles. Jitter measurement may vary. Actual jitter is dependent on Input jitter and edge rate, number of active outputs, inputs and output frequencies, supply voltage, temperature, and output load.

SCHEMATIC FOR OUTPUT TERMINATION

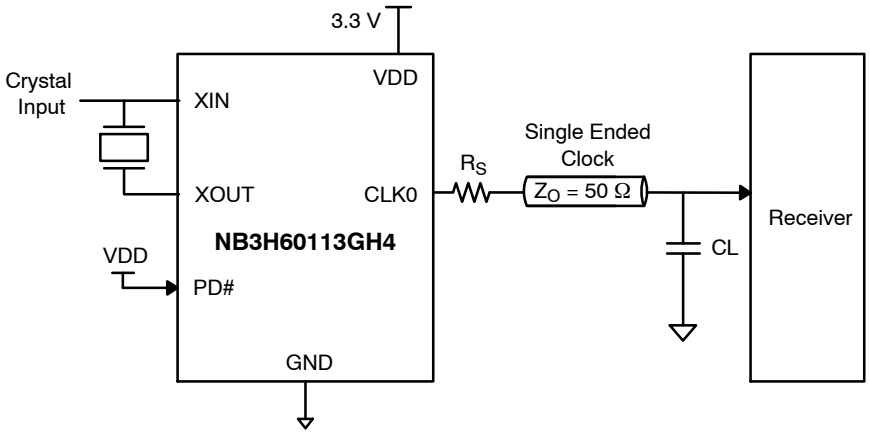


Figure 5. Typical Termination for Single−Ended Device Load

PARAMETER MEASUREMENT TEST CIRCUITS

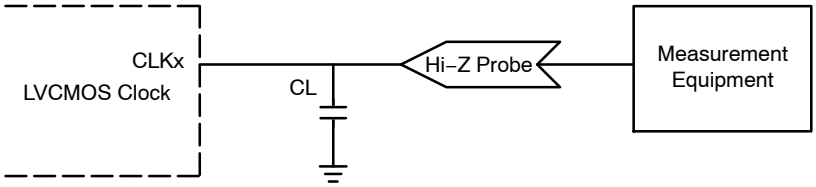


Figure 6. LVCMOS Parameter Measurement

TIMING MEASUREMENT DEFINITIONS

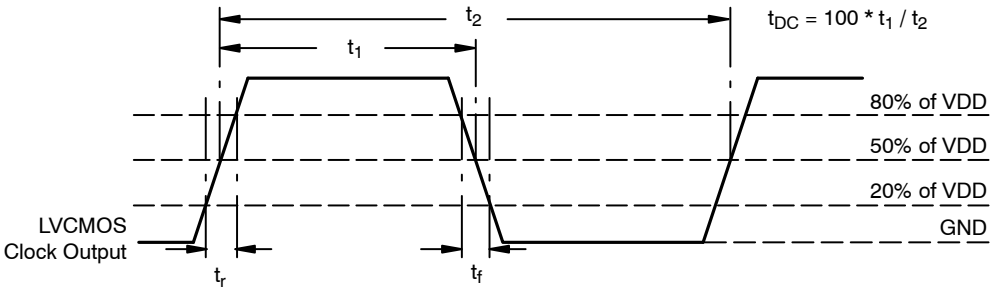


Figure 7. LVCMOS Measurement for AC Parameters

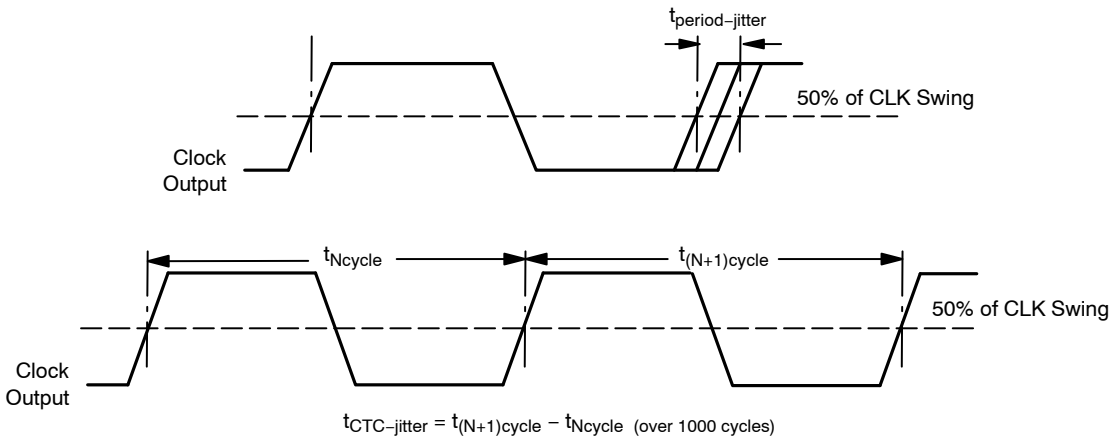


Figure 8. Period and Cycle−Cycle Jitter Measurement

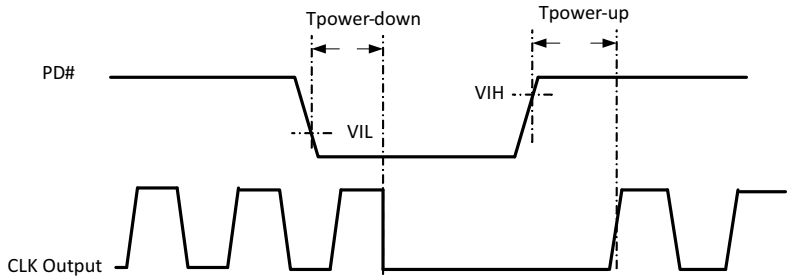


Figure 9. Output Enable/ Disable and Power Down Functions

APPLICATION GUIDELINES

Crystal Input Interface

Figure 10 shows the NB3H60113GH4 device crystal oscillator interface using a typical parallel resonant fundamental mode crystal. A parallel crystal with loading capacitance C_L = 18 pF would use C1 = 32 pF and C2 = 32 pF as nominal values, assuming 4 pF of stray capacitance per line.

$$C_L = (C1 + Cstray)/2;\ C1 = C2$$

The frequency accuracy and duty cycle skew can be fine−tuned by adjusting the C1 and C2 values. For example, increasing the C1 and C2 values will reduce the operational frequency. Note R1 is optional and may be 0 Ω.

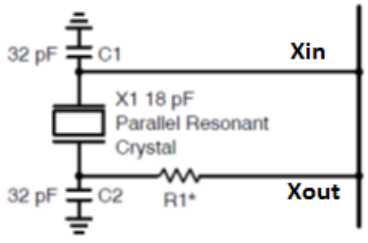


Figure 10. Crystal Interface Loading

Output Interface and Terminations

The NB3H60113GH4 consists of a unique Multi Standard Output Driver to support LVCMOS standards. The required termination changes must be considered and taken care of by the system designer.

LVCMOS Interface

LVCMOS output swings rail−to−rail up to V_{DD} supply and can drive up to 15 pF load at higher drive strengths. The output buffer's drive is programmable up to four steps, here in this device maximum drive current setting is choosen. (See Figure 11 and Table 10). Drive strength must be configured high for driving higher loads. The slew rate of the clock signal increases with higher output current drive for the same load. The software lets the user choose the load drive current value per LVCMOS output based on the V_{DD} supply selected.

Table 10. LVCMOS DRIVE LEVEL SETTINGS

VDD Supply	Load Current Setting Max Load Current
3.3 V	16 mA

The load current consists of the static current component (varies with drive) and dynamic current component. For any

supply voltage, the dynamic load current range per LVCMOS output can be approximated by formula –

$$IDD = f_{out} * C_{load} * VDD$$

C_{load} includes the load capacitor connected to the output, the pin capacitor posed by the output pin (typically 5 pF) and the cap load posed by the receiver input pin. C_{load} = (CL + Cpin+ Cin)

An optional series resistor Rs can be connected at the output for impedance matching, to limit the overshoots and ringings.

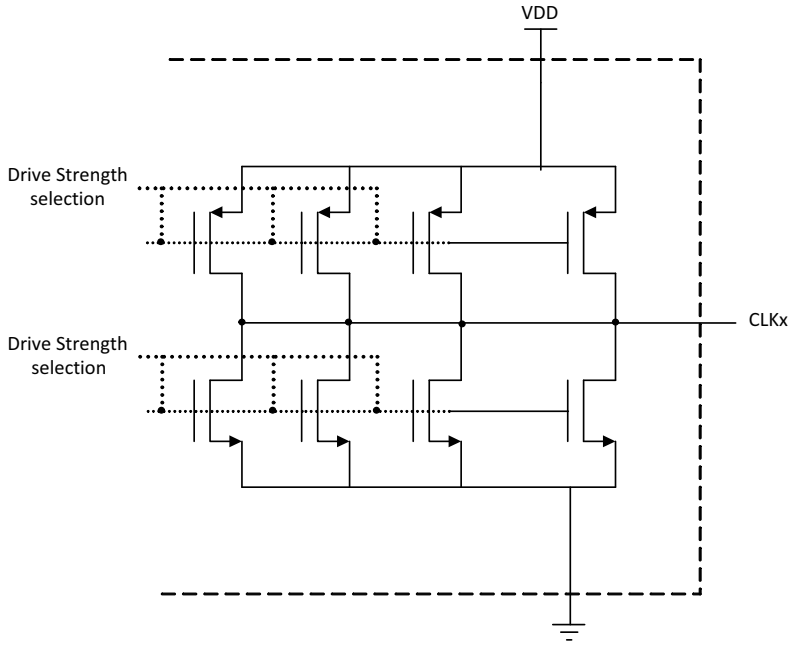


Figure 11. Simplified LVCMOS Output Structure

Recommendation for Clock Performance

Clock performance is specified in terms of Jitter in time the domain and Phase noise in frequency domain. Details and measurement techniques of Cycle−cycle jitter, period jitter, TIE jitter and Phase Noise are explained in application note AND8459/D.

In order to have a good clock signal integrity for minimum data errors, it is necessary to reduce the signal reflections. Reflection coefficient can be zero only when the source impedance equals the load impedance. Reflections are based on signal transition time (slew rate) and due to impedance mismatch. Impedance matching with proper termination is required to reduce the signal reflections. The amplitude of overshoots is due to the difference in impedance and can be minimized by adding a series resistor (Rs) near the output pin. Greater the difference in impedance, greater is the amplitude of the overshoots and subsequent ripples. The ripple frequency is dependant on the signal travel time from the receiver to the source. Shorter traces results in higher ripple frequency, as the trace gets longer the travel time increases, reducing the ripple frequency. The ripple frequency is independent of signal frequency, and only depends on the trace length and the propagation delay. For eg. On an FR4 PCB with approximately 150 ps/ inch of propagation rate, on a 2 inch trace, the ripple frequency = 1 / (150 ps * 2 inch * 5) = 666.6 MHz; [5 = number of times the signal travels, 1 trip to receiver plus 2 additional round trips]

PCB traces should be terminated when trace length tr/f / (2* tprate); tr/f = rise/ fall time of signal, tprate = propagation rate of trace.

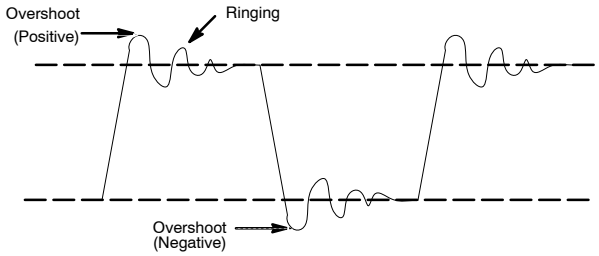


Figure 12. Signal Reflection Components

PCB Design Recommendation

For a clean clock signal waveform it is necessary to have a clean power supply for the device. The device must be isolated from system power supply noise. A 0.1 μF and a 2.2 μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin and the ground via should be kept thicker and as short as possible. All the VDD pins should have decoupling capacitors.

Stacked power and ground planes on the PCB should be large. Signal traces should be on the top layer with minimum vias and discontinuities and should not cross the reference planes. The termination components must be placed near the source or the receiver. In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

Device Applications

The NB3H60113GH4 is targeted mainly for the Industrial market segment and can be used as per the examples below as per Figure 13.

Clock Generator

Consumer applications require single reference clock sources at various locations in the system. This part can function as a clock generating IC for applications requiring a reference clock for interface.

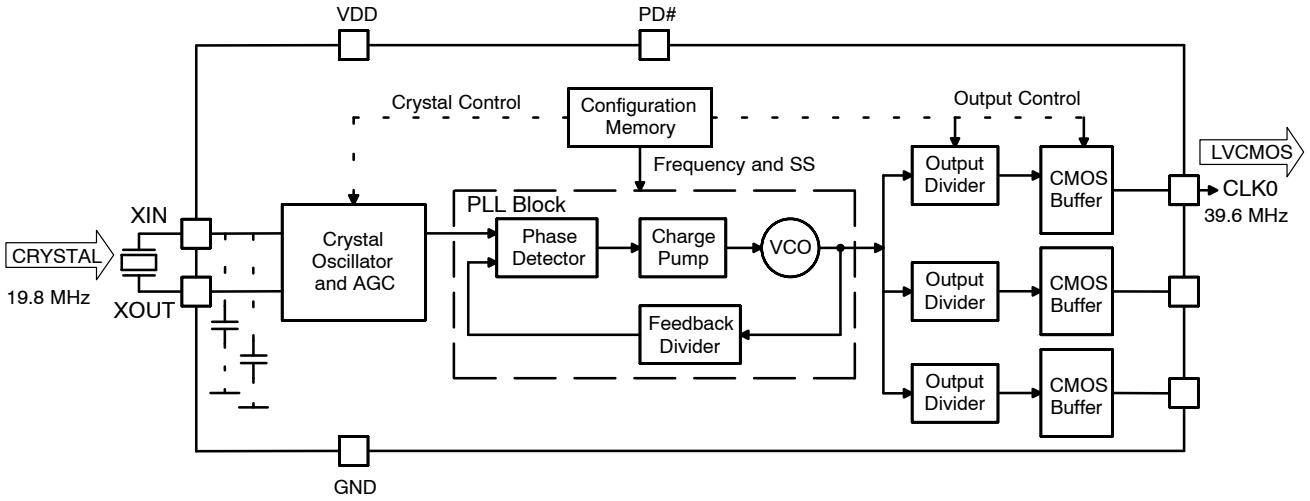


Figure 13. Application as Clock Generator

NOTE: LVCMOS signal level cannot be translated to a higher level of LVCMOS voltage.

ORDERING INFORMATION

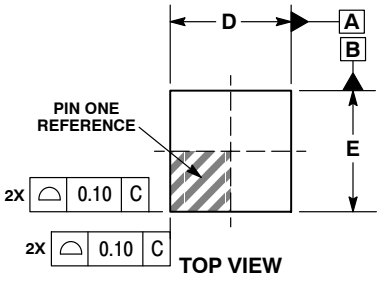
Device	Case	Package	Shipping†
NB3H60113GH4MTR2G	511AT	DFN−8 (Pb−Free)	3000 / Tape & Reel

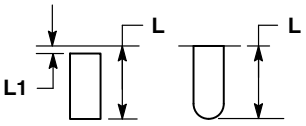
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB3H60113GH4

PACKAGE DIMENSIONS

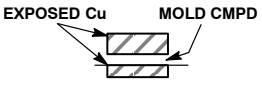
WDFN8 2x2, 0.5P
CASE 511AT−01
ISSUE O



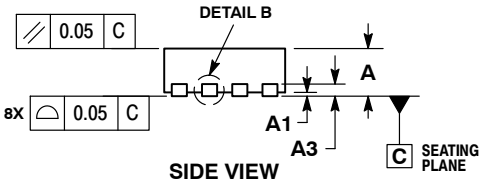


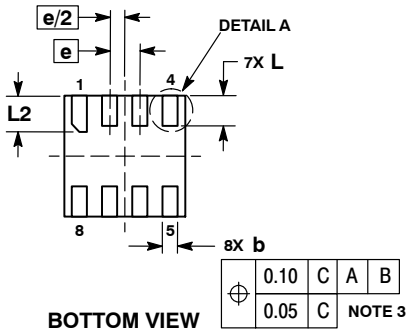
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70

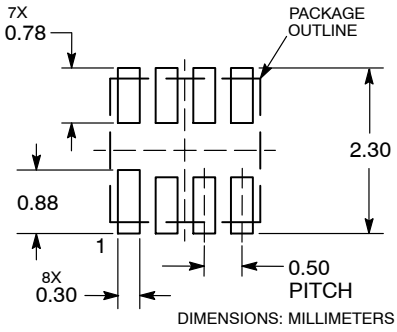


DETAIL B
ALTERNATE CONSTRUCTIONS





RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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