N-Channel JFET

MMBFJ110

Features

- This Device is Designed for Digital Switching Applications where Very Low On Resistance is Mandatory
- Sourced from Process 58
- This is a Pb−Free Device

MAXIMUM RATINGS (T_A = 25°C unless otherwise specified) (Notes 1, 2)

Symbol	Parameter	Value	Unit
V_{DG}	Drain−Gate Voltage	25	V
V_{GS}	Gate−Source Voltage	−25	V
I_{GF}	Forward Gate Current	10	mA
T_J	Junction Temperature	150	°C
T_J, T_{STG}	Storage Temperature Range	−55 to 150	°C

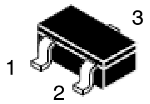
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. These ratings are based on a maximum junction temperature of 150°C.
2. These are steady−state limits. **onsemi** should be consulted on applications involving pulsed or low−duty−cycle operations.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 3)

Symbol	Parameter	Max	Unit
P_D	Total Device Dissipation	460	mW
	Derate Above 25°C	3.68	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	270	°C/W

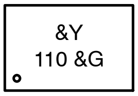
3. Device mounted on FR−4 PCB 36 mm x 18 mm x 1.5 mm; mounting pad for the collector lead minimum 6 cm^2.



SOT−23/SUPERSOT™−23,
3 LEAD, 1.4x2.9
CASE 527AG

1. Drain, 2. Source, 3. Gate

MARKING DIAGRAM



110 = Specific Device Code
&Y = Year Coding
&G = Weekly Date Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Max	Unit
OFF CHARACTERISTICS					
$V_{(BR)GSS}$	Gate−Source Breakdown Voltage	$I_G = -10\ \mu A$, $V_{DS} = 0$	−25	–	V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15$ V, $V_{DS} = 0$	–	−3.0	nA
		$V_{GS} = -15$ V, $V_{DS} = 0$, $T_A = 100°C$	–	−200	
$V_{GS}(off)$	Gate−Source Cut−Off Voltage	$V_{DS} = 15$ V, $I_D = 10$ nA	−0.5	−4.0	V
ON CHARACTERISTICS					
I_{DSS}	Zero−Gate Voltage Drain Current (Note 4)	$V_{DS} = 15$ V, $V_{GS} = 0$	10	–	mA
$r_{DS}(on)$	Drain−Source On Resistance	$V_{DS} \leq 0.1$ V, $V_{GS} = 0$	–	18	Ω
SMALL SIGNAL CHARACTERISTICS					
$C_{dg}(on)$ $C_{sg}(on)$	Drain−Gate & Source−Gate On Capacitance	$V_{DS} = 0$, $V_{GS} = 0$, f = 1.0 MHz	–	85	pF
$C_{dg}(off)$ $C_{sg}(off)$	Drain−Gate & Source−Gate Off Capacitance	$V_{DS} = 0$, $V_{GS} = -10$ V, f = 1.0 MHz	–	15	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

TYPICAL PERFORMANCE CHARACTERISTICS

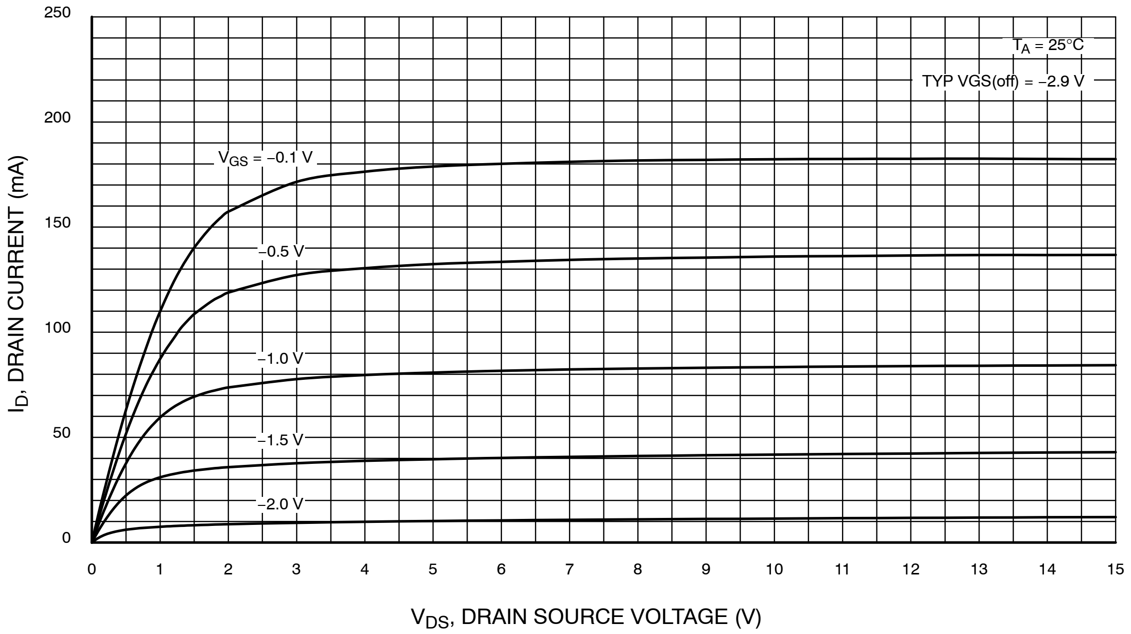


Figure 1. Common Drain−Source

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

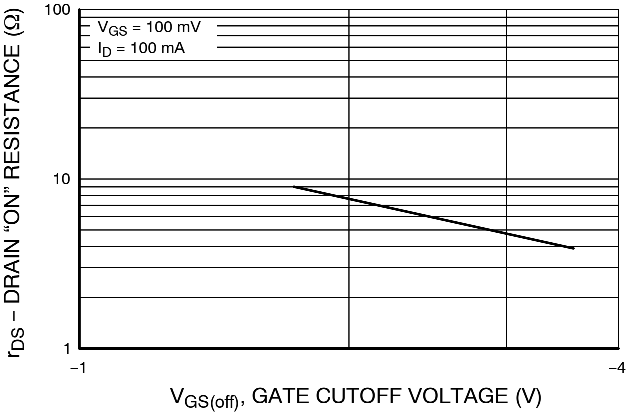


Figure 2. Drain ON Resistance

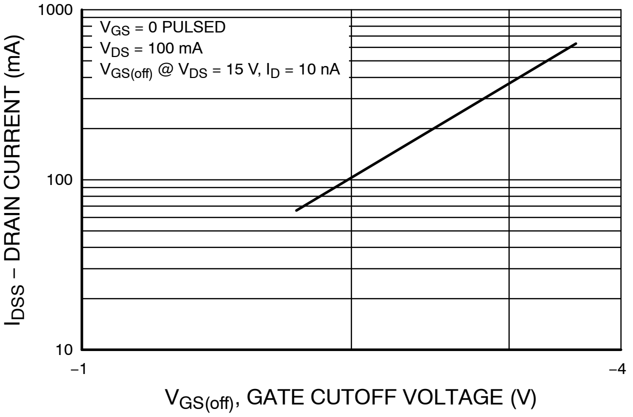


Figure 3. Drain Current vs. Gate–Source Cut–Off Voltage

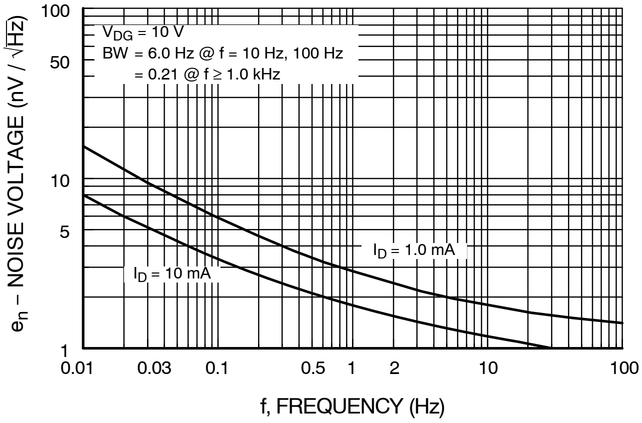


Figure 4. Noise Voltage vs. Frequency

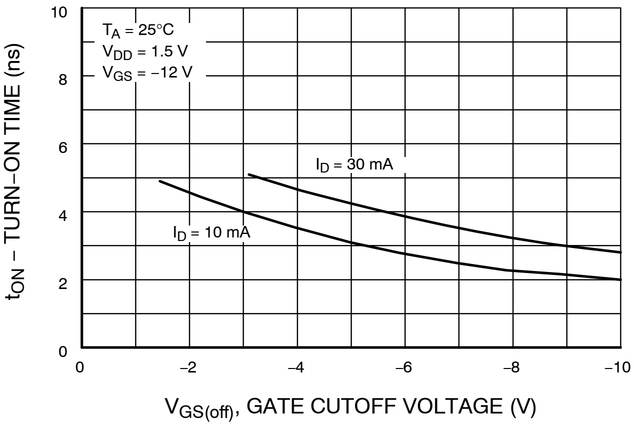


Figure 5. Switching Turn–On Time vs. Gate–Source Cut–Off Voltage

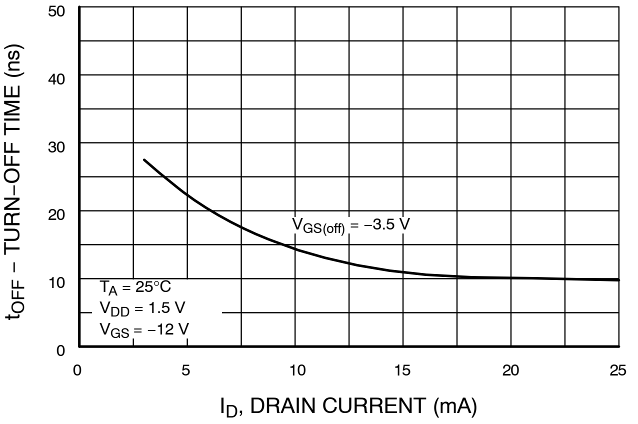


Figure 6. Switching Turn–On Time vs. Drain Current

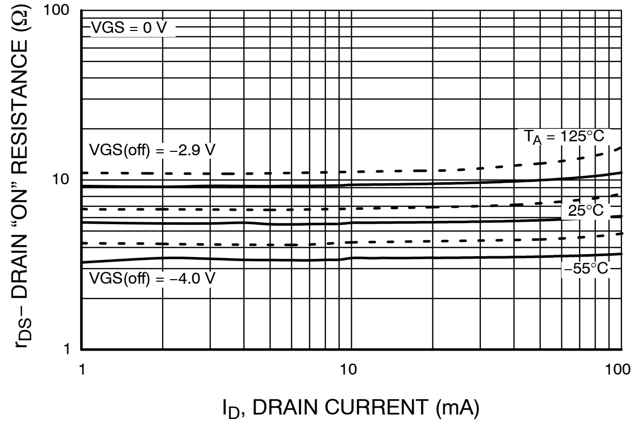


Figure 7. On Resistance vs. Drain Current

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

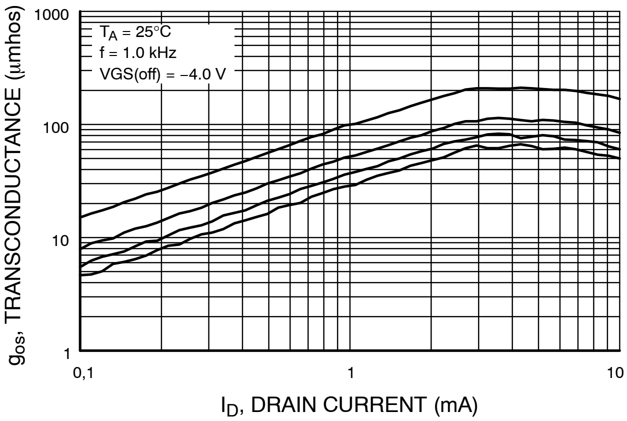


Figure 8. Output Conductance vs. Drain Current

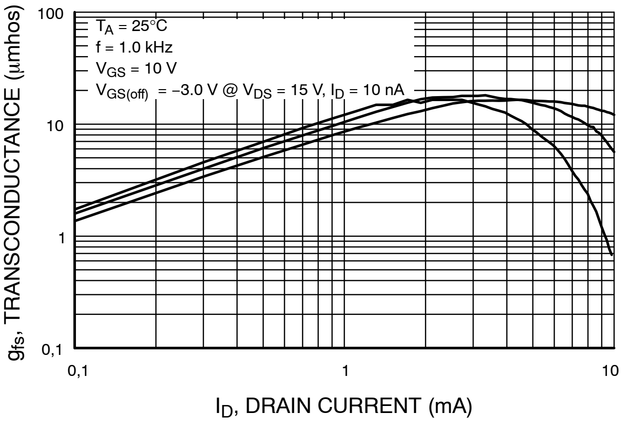


Figure 9. Output Conductance vs. Drain Current

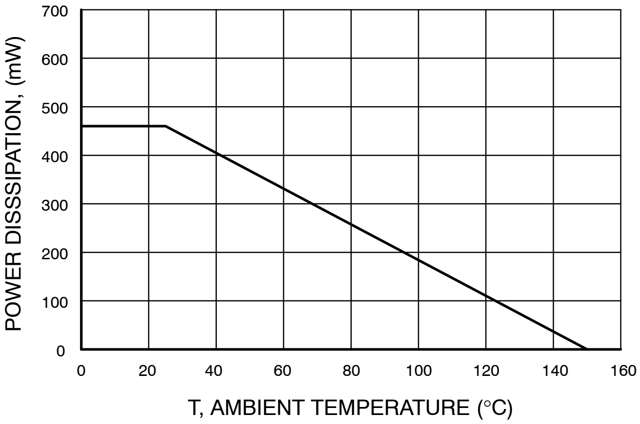
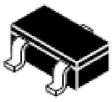


Figure 10. Power Dissipation vs. Ambient Temperature

ORDERING INFORMATION

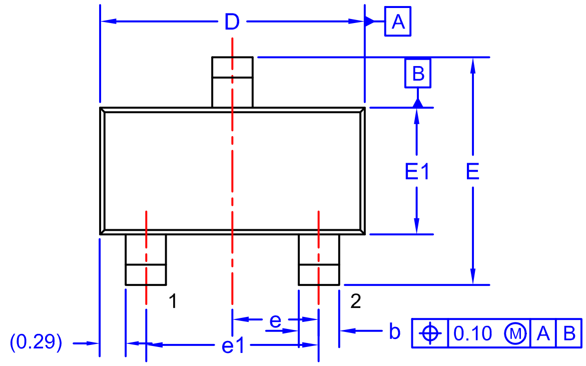
Part Number	Top Mark	Package	Shipping†
MMBFJ110	110	SSOT 3L (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SOT−23/SUPERSOT™−23, 3 LEAD, 1.4x2.9
CASE 527AG
ISSUE A

DATE 09 DEC 2019

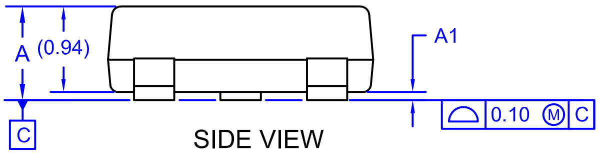


TOP VIEW

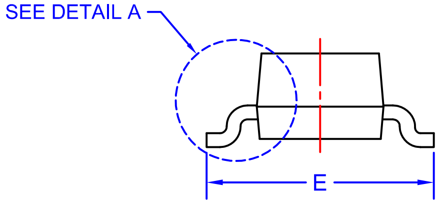
NOTES: UNLESS OTHERWISE SPECIFIED

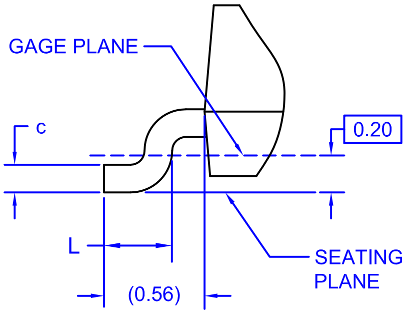
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e	0.95 BSC		
e1	1.90 BSC		
L	0.33	0.38	0.43

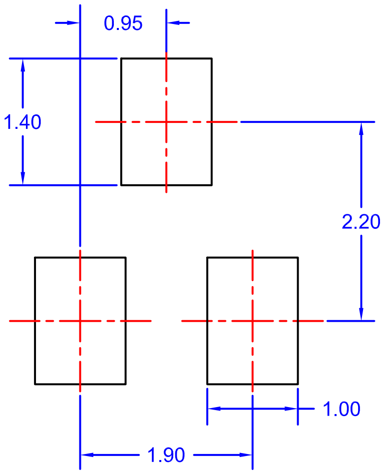


SIDE VIEW





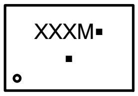
DETAIL A



LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOT−23/SUPERSOT−23, 3 LEAD, 1.4X2.9**	**PAGE 1 OF 1**

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