

Dual Type D Flip-Flop

MC14013B

The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and \bar{Q}). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

Features

- Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design
- Logic State is Retained Indefinitely with Clock Level either High or Low; Information is Transferred to the Output only on the Positive-going Edge of the Clock Pulse
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

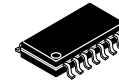
1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65 °C To 125 °C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



SOIC-14
D SUFFIX
CASE 751A

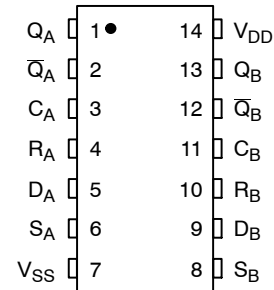


SOEIAJ-14
F SUFFIX
CASE 965

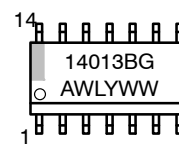


TSSOP-14
DT SUFFIX
CASE 948G

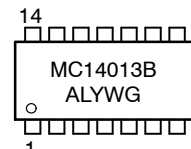
PIN ASSIGNMENT



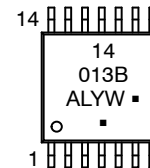
MARKING DIAGRAMS



SOIC-14



SOEIAJ-14



TSSOP-14

- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)




ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 3.

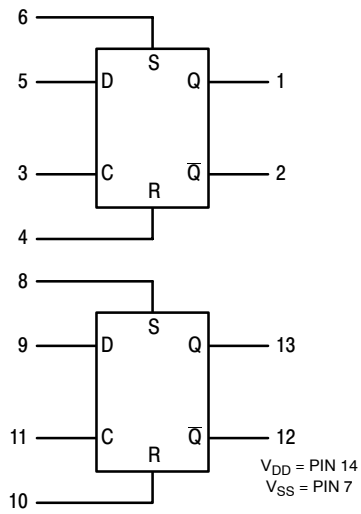
MC14013B

TRUTH TABLE

Inputs				Outputs		No Change
Clock [†]	Data	Reset	Set	Q	Q	
	0	0	0	0	1	
	1	0	0	1	0	
	X	0	0	Q	Q	
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = Don't Care
 † = Level Change

BLOCK DIAGRAM



MC14013B

ORDERING INFORMATION

Device	Package	Shipping†
MC14013BDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14013BDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NLV14013BDR2G*	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC14013BDTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV14013BDTR2G*	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 2)

NLV14013BDG*	SOIC-14 (Pb-Free)	55 Units / Rail
MC14013BFG	SOEIAJ-14 (Pb-Free)	50 Units / Rail
MC14013BFELG	SOEIAJ-14 (Pb-Free)	2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

* NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

2. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55 °C		25 °C			125 °C		Unit	
			Min	Max	Min	Typ (Note3)	Max	Min	Max		
Output Voltage "0" Level V _{in} = V _{DD} or 0	V _{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc	
		10	-	0.05	-	0	0.05	-	0.05		
15		-	0.05	-	0	0.05	-	0.05			
V _{in} = 0 or V _{DD} "1" Level	V _{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc	
		10	9.95	-	9.95	10	-	9.95	-		
		15	14.95	-	14.95	15	-	14.95	-		
Input Voltage "0" Level (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc	
		10	-	3.0	-	4.50	3.0	-	3.0		
		15	-	4.0	-	6.75	4.0	-	4.0		
	"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
			10	7.0	-	7.0	5.50	-	7.0	-	
			15	11	-	11	8.25	-	11	-	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc	
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-		
		10	-1.6	-	-1.3	-2.25	-	-0.9	-		
	Sink I _{OL}	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc	
		10	1.6	-	1.3	2.25	-	0.9	-		
		15	4.2	-	3.4	8.8	-	2.4	-		
Input Current	I _{in}	15	-	±0.1	-	±0.0000 1	±0.1	-	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	-	1.0	-	0.002	1.0	-	30	μAdc	
		10	-	2.0	-	0.004	2.0	-	60		
		15	-	4.0	-	0.006	4.0	-	120		
Total Supply Current (Notes 4, 5) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	$I_T = (0.75 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (1.5 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (2.3 \mu\text{A/kHz}) f + I_{DD}$							μAdc	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25 °C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

MC14013B

SWITCHING CHARACTERISTICS (Note 6) ($C_L = 50 \text{ pF}$, $T_A = 25 \text{ }^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	Min	Typ (Note 7)	Max	Unit
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q, \bar{Q} t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ Set to Q, \bar{Q} t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ Reset to Q, \bar{Q} t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 67 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 50 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15 5.0 10 15 5.0 10 15	– – – – – – – – –	175 75 50 175 75 50 225 100 75	350 150 100 350 150 100 450 200 150	ns
Setup Times (Note 8)	t_{su}	5.0 10 15	40 20 15	20 10 7.5	– – –	ns
Hold Times (Note 8)	t_h	5.0 10 15	40 20 15	20 10 7.5	– – –	ns
Clock Pulse Width	t_{WL} , t_{WH}	5.0 10 15	250 100 70	125 50 35	– – –	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	– – –	4.0 10 14	2.0 5.0 7.0	MHz
Clock Pulse Rise and Fall Time	t_{TLH} t_{THL}	5.0 10 15	– – –	– – –	15 5.0 4.0	μs
Set and Reset Pulse Width	t_{WL} , t_{WH}	5.0 10 15	250 100 70	125 50 35	– – –	ns
Removal Times Set	t_{rem}	5 10 15	80 45 35	0 5 5	– – –	ns
Reset		5 10 15	50 30 25	–35 –10 –5	– – –	

6. The formulas given are for the typical characteristics only at 25 °C.

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

8. Data must be valid for 250 ns with a 5 V supply, 100 ns with 10 V, and 70 ns with 15 V.

MC14013B

LOGIC DIAGRAM (1/2 of Device Shown)

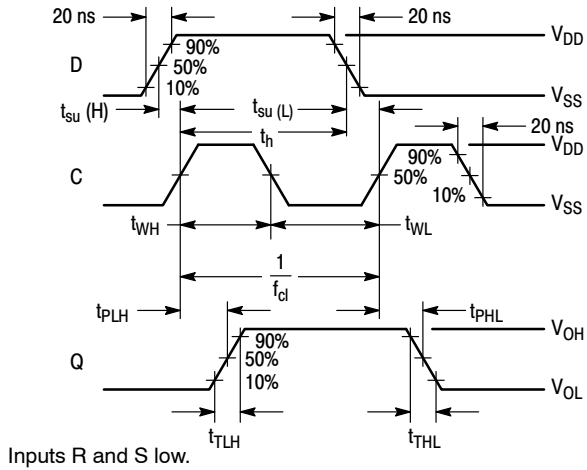
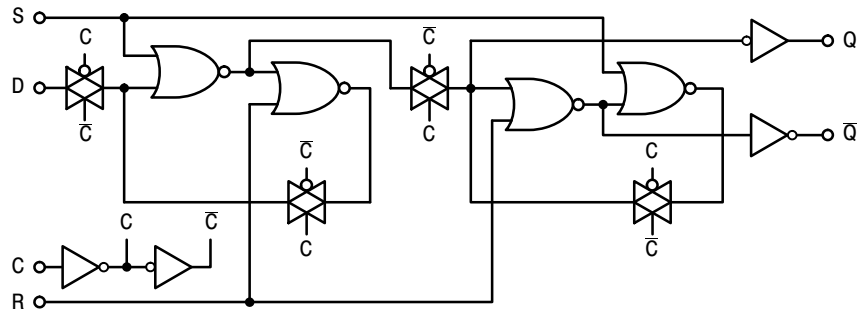


Figure 1. Dynamic Signal Waveforms (Data, Clock, and Output)

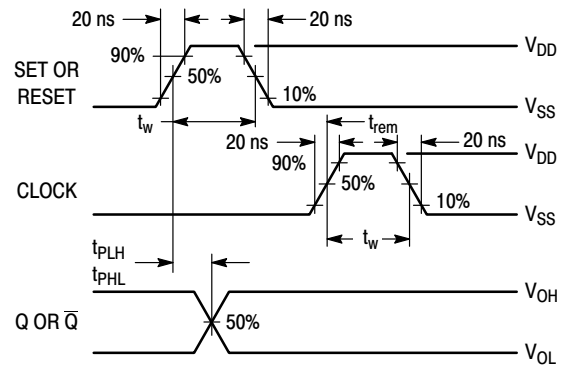
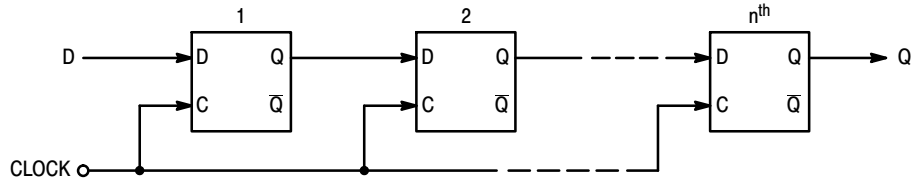


Figure 2. Dynamic Signal Waveforms (Set, Reset, Clock, and Output)

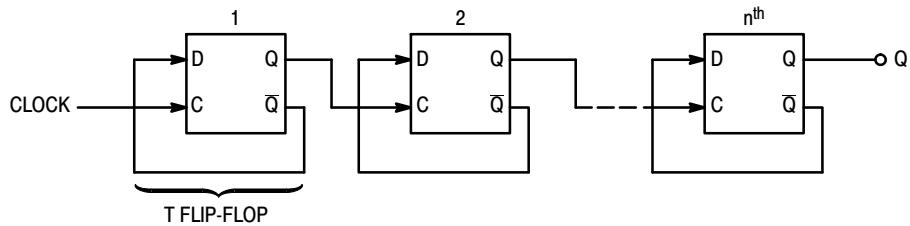
MC14013B

TYPICAL APPLICATIONS

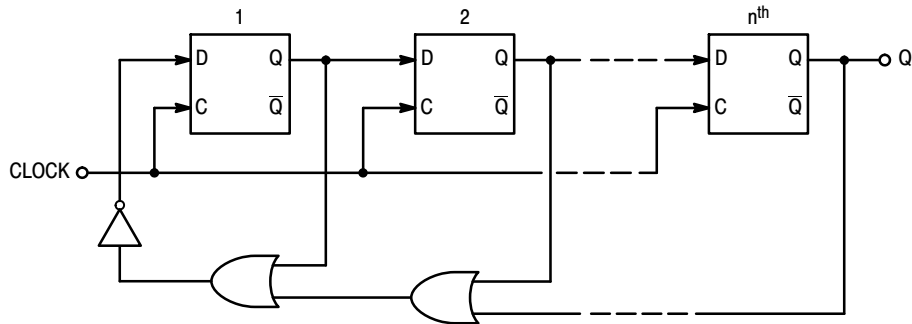
n-STAGE SHIFT REGISTER



BINARY RIPPLE UP-COUNTER (Divide-by- 2^n)



MODIFIED RING COUNTER (Divide-by- $(n+1)$)



REVISION HISTORY

Revision	Description of Changes	Date
11	Rebranded the Data Sheet to onsemi format. NLV14013BDG, MC14013BFG, MC14013BFELG OPNs Marked as Discontinued.	07/11/2025

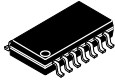
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

MC14013B

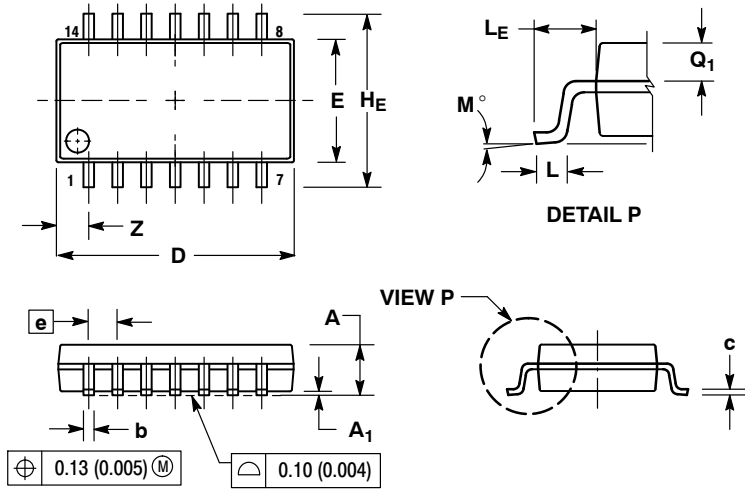
PACKAGE DIMENSIONS

SOEIAJ-14
CASE 965-01
ISSUE B

DATE 29 FEB 2008



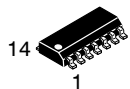
SCALE 1:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

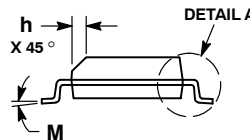
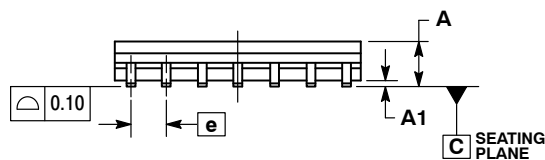
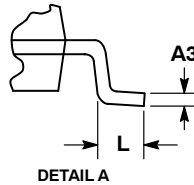
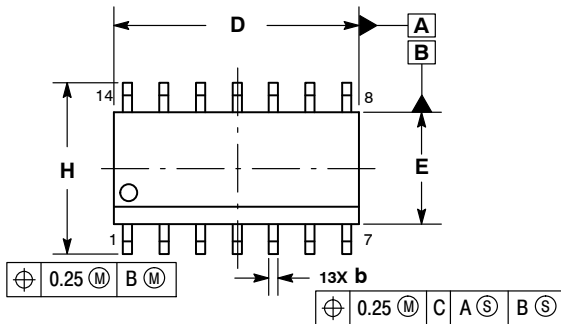
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

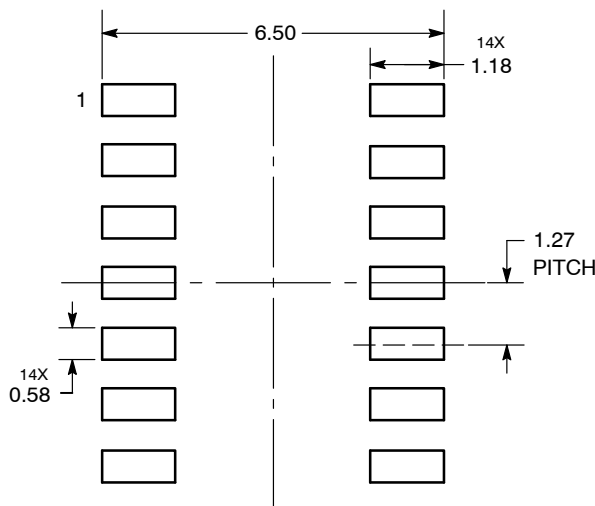


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

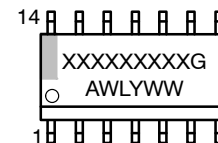
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-14 NB	PAGE 1 OF 2

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

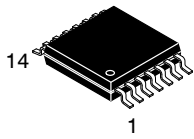
STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

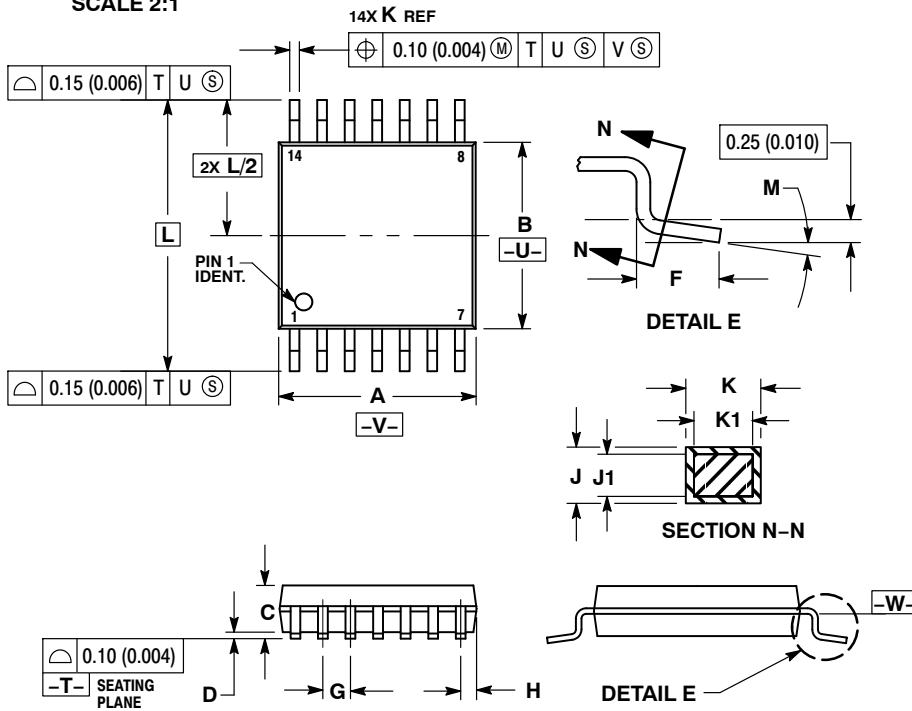
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DESCRIPTION:	SOIC-14 NB	PAGE 2 OF 2

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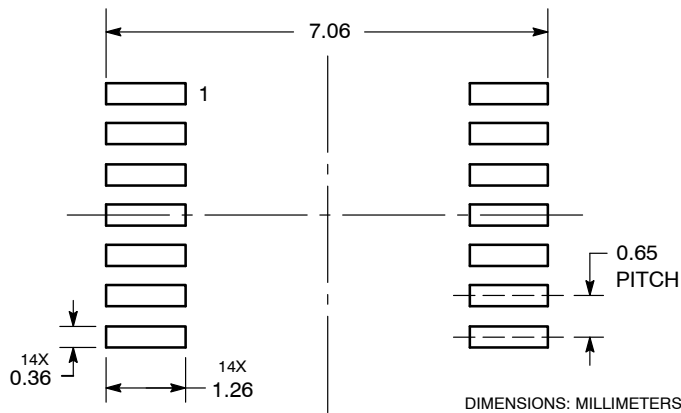
TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



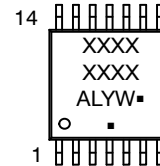
- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: MILLIMETER.
 - DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 - DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 - DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 - TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 - DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

RECOMMENDED
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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