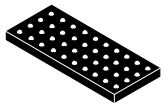
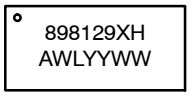
Summary of Specification for OIS & CL-AF Control LSI

LC898129DP1XHTBG



WLCSP40, 1.60x4.15x0.33
CASE 567XS

MARKING DIAGRAM



898129XH	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year of Production
WW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

Overview

LC898129DP1XHTBG is a system LSI integrating an on−chip 32 bit DSP, a FLASH ROM and peripherals including analog circuits for OIS (Optical Image Stabilization) / Closed Loop−AF (Auto Focus) control and drivers.

Features

- On−chip 32 bit DSP
  - Built−in Software for Digital Servo Filter
  - Built−in Software for Gyro Filter
- Memory
  - Flash Memory
  - Program ROM
  - Program SRAM
  - Data SRAM
- Peripherals
  - AD Converter
  - DA Converter
  - 2−wire Serial I/F Circuit (The Communication Protocol is Compatible with I^2C)
  - Hall Bias Circuit
  - Hall Amp
  - OSC (Oscillator)
  - LDO (Low Drop−Out Regulator)
  - Digital Gyro I/F (SPI)
  - Interrupt I/F
- Driver
  - OIS
    Linear Driver (x2ch, I_{full} = 200 mA)
  - CL−AF (bi−direction)
    Linear Driver (x1ch, I_{full} = 150 mA)
- Power Supply Voltage
  - AD/DA/VGA/LDO/OSC/Flash: AVDD30 = 2.7 V to 3.3 V
  - Driver: VM = 1.8 V to 3.3 V
  - 1.8 V I/O: IOVDD = 1.7 V to 3.3 V
  - Core Logic: Generated by On−chip LDO
    Connect 1 μF Capacitor to LDPO pin
- Package
  - WLCSP40 (4 x 10 Pin) Thickness Max. 0.35 mm, with Back Coat
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

BLOCK DIAGRAM

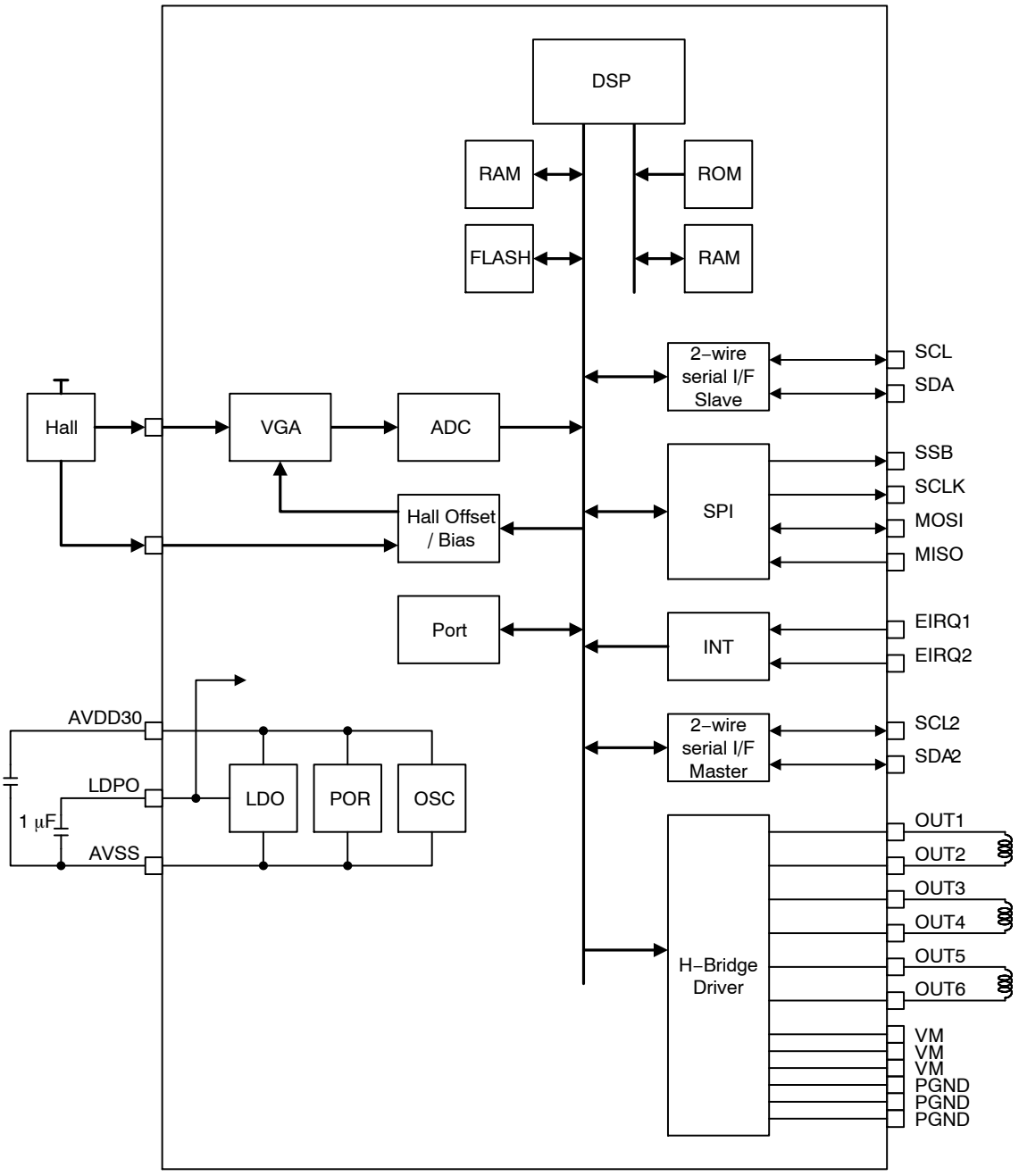


Figure 1. Block Diagram

PIN LAYOUT

	1	2	3	4	5	6	7	8	9	10
D	OUT1	VM	OUT5	OUT6	VM	HLBO2	HLBO3	EIRQ1	SSB	SCL
C	OUT2	PGND	PGND	HLBO1	AVSS	MON1	SCL2	EIRQ2	SCLK	SDA
B	OUT3	PGND	OPINM1	OPINM2	OPINM3	MON2	SDA2	AVSS	MOSI	MISO
A	OUT4	VM	OPINP1	OPINP2	OPINP3	AVSS	AVDD30	LDPO	AVSS	IOVDD

Driver
VDD/VSS
Internal VDD Output
1.8 V I/O

Figure 2. Pin Layout (Bottom View)

Table 1. PIN DESCRIPTION

No.	Pin	I/O	I/O Pwr	Function	Init
1	MON1	B	AVDD30	Servo Monitor Analog In/Out	Z
2	MON2	B	AVDD30	Servo Monitor Analog In/Out	Z
3	SCL	B	IOVDD	2−wire serial HOST I/F Clock Slave	Z
4	SDA	B	IOVDD	2−wire serial HOST I/F Data Slave	Z
5	IOVDD	P		I/O Power (1.7 V to 3.3 V)	−
6	SSB	B	IOVDD	Digital Gyro Data I/F Chip Select Out (3/4−wire Master)	Z
7	SCLK	B	IOVDD	Digital Gyro Data I/F Clock Out (3/4−wire Master)	Z
8	MOSI	B	IOVDD	Digital Gyro Data I/F Data InOut (3−wire Master) Digital Gyro Data I/F Data Out (4−wire Master)	Z
9	MISO	B	IOVDD	Digital Gyro Data I/F Data In (4−wire Master)	U
10	EIRQ1	B	IOVDD	Interrupt Input 1	Z
11	EIRQ2	B	IOVDD	Interrupt Input 2	Z
12	SCL2	B	AVDD30	2−wire serial I/F Clock Master	Z
13	SDA2	B	AVDD30	2−wire serial I/F Data Master	Z
14	HLBO1	O	AVDD30	Hall Bias Output 1	Z
15	HLBO2	O	AVDD30	Hall Bias Output 2	Z
16	HLBO3	O	AVDD30	Hall Bias Output 3	Z
17	OPINM1	I	AVDD30	Hall Opamp Input Minus 1	−

Table 1. PIN DESCRIPTION (continued)

No.	Pin	I/O	I/O Pwr	Function	Init
18	OPINP1	I	AVDD30	Hall Opamp Input Plus 1	–
19	OPINM2	I	AVDD30	Hall Opamp Input Minus 2	–
20	OPINP2	I	AVDD30	Hall Opamp Input Plus 2	–
21	OPINM3	I	AVDD30	Hall Opamp Input Minus 3	–
22	OPINP3	I	AVDD30	Hall Opamp Input Plus 3	–
23	OUT1	O	VM	OIS Driver Output	Z
24	OUT2	O	VM	OIS Driver Output	Z
25	OUT3	O	VM	OIS Driver Output	Z
26	OUT4	O	VM	OIS Driver Output	Z
27	OUT5	O	VM	CL−AF Driver Output	Z
28	OUT6	O	VM	CL−AF Driver Output	Z
29	AVDD30	P		Analog Power (2.7 V to 3.3 V)	–
30	AVSS	P		Analog GND	–
31	VM	P		Driver Power (1.8 V to 3.3 V)	–
32	VM	P		Driver Power (1.8 V to 3.3 V)	–
33	VM	P		Driver Power (1.8 V to 3.3 V)	–
34	PGND	P		Driver GND	–
35	LDPO	P		Internal 1.38 V LDO Power Output	–
36	AVSS	P		Analog GND	
37	AVSS	P		Analog GND	
38	AVSS	P		Analog GND	
39	PGND	P		Driver GND	
40	PGND	P		Driver GND	

*Process when pins are not used
PIN TYPE “O” – Ensure that it is set to OPEN.
PIN TYPE “I” – OPEN is inhibited. Ensure that it is connected to the V_{DD} or V_{SS} even when it is unused.
(Please contact **onsemi** for more information about selection of V_{DD} or V_{SS}.)
PIN TYPE “B” – If you are unsure about processing method on the pin description of pin layout table, please contact us.

Note that incorrect processing of unused pins may result in defects.

ELECTRICAL CHARACTERISTICS

Table 2. ABSOLUTE MAXIMUM RATINGS (AVSS = 0 V, PGND = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	$V_{AD}30$ max	Ta ≤ 25°C	−0.3 to 4.6	V
	V_M max	Ta ≤ 25°C	−0.3 to 4.6	
	V_{IO} max	Ta ≤ 25°C	−0.3 to 4.6	
Input/Output voltage	$V_{AI}30$, $V_{AO}30$	Ta ≤ 25°C	−0.3 to $V_{AD}30$ + 0.3	V
	V_{MI}, V_{MO}	Ta ≤ 25°C	−0.3 to V_M + 0.3	
	V_{II}, V_{IOO}	Ta ≤ 25°C	−0.3 to V_{IO} + 0.3	
Storage temperature	Tstg		−55 to 125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. ALLOWABLE OPERATING RATINGS (Ta = −30 to 85°C, AVSS = 0 V, PGND = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
3.0 V POWER SUPPLY (AVDD30)					
Power supply voltage	$V_{AD}30$	2.7	2.8	3.3	V
Input voltage range	V_{INA}	0	–	$V_{AD}30$	V
3.0 V POWER SUPPLY (VM) (Note 1)					
Power supply voltage	V_M	1.8	2.8	3.3	V
Input voltage range	V_{INM}	0	–	V_M	V
1.8 V POWER SUPPLY (IOVDD)					
Power supply voltage	V_{IO}	1.7	1.8	3.3	V
Input voltage range	V_{INI}	0	–	V_{IO}	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Three VM pins should be connected.

Table 4. D.C. CHARACTERISTICS: INPUT/OUTPUT
(Ta = −30 to 85°C, AVSS = 0 V, PGND = 0 V, AVDD30 = 2.7 to 3.3 V, IOVDD = 1.7 to 3.3 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Applicable Pins
High−level input voltage	VIH	CMOS schmitt	0.7 IOVDD	−	−	V	SCL, SDA, SSB, SCLK, MOSI, MISO, EIRQ1, EIRQ2
Low−level input voltage	VIL		−	−	0.3 IOVDD	V	
High−level input voltage	VIH	CMOS schmitt	1.4	−	−	V	SCL2, SDA2
Low−level input voltage	VIL		−	−	0.4	V	
High−level input voltage	VIH	CMOS schmitt	0.7 AVDD30	−		V	MON1, MON2
Low−level input voltage	VIL			−	0.3 AVDD30	V	
High−level output voltage	VOH	IOH = −3 mA	IOVDD − 0.2	−	−	V	SDA, SSB, SCLK, MOSI, MISO, EIRQ1, EIRQ2
Low−level output voltage	VOL	IOL = 3 mA	−	−	0.2	V	SCL, SDA, SSB, SCLK, MOSI, MISO, EIRQ1, EIRQ2
High−level output voltage	VOH	IOH = −3 mA	AVDD30 − 0.2	−		V	SCL2, SDA2
Low−level output voltage	VOL	IOL = 3 mA		−	0.2	V	
High−level output voltage	VOH	IOH = −2 mA	AVDD30 − 0.2	−	−	V	MON1, MON2
Low−level output voltage	VOL	IOL = 2 mA		−	0.2	V	
Analog input voltage	VAI		AVSS	−	AVDD30	V	MON1, MON2, OPINP1, OPINM1, OPINP2, OPINM2, OPINP3, OPINM3
Pull Up resistor	Rup		20	−	250	kΩ	SSB, SCLK, MOSI, MISO, EIRQ1, EIRQ2, MON1, MON2, SCL2, SDA2
Pull Down resistor	Rdn		20	−	250	kΩ	

Table 5. DRIVER OUTPUT (Ta = 25°C, AVSS = 0 V, PGND = 0 V, AVDD30 = VM = 2.8 V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Current OUT1~OUT4	Ifull	Full code	190	200	210	mA
Output Current OUT5, OUT6		Full code, OP−AF (bidirection)	142.5	150	157.5	mA

Table 6. NON−VOLATILE MEMORY CHARACTERISTICS

Operating temperature	Topr1	Read for FLASH	−30~85	°C
	Topr2	Program & Erase for FLASH	−10~65 (Note 2)	°C

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable Circuit
Endurance	EN		−	−	1000	Cycles	Flash Memory
Data retention	RT		10	−	−	Years	
Write time	tWT		−	−	3	ms	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2. All drivers must be in the standby state.

AC CHARACTERISTICS

Power Supply Timing

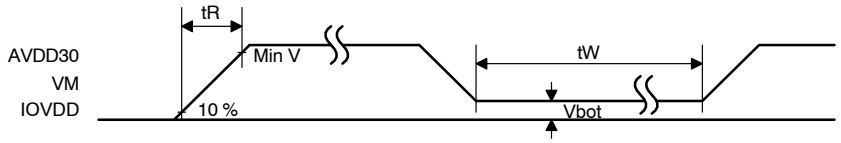


Figure 3. V_{DD} Supply Timing

Table 7.

Item	Symbol	Min	Typ	Max	Units
Rise time	tR	–	–	3	ms
Wait time	tW	100	–	–	ms
Bottom Voltage	Vbot	–	–	0.2	V

Injection order between AVDD30, VM and IOVDD is below.

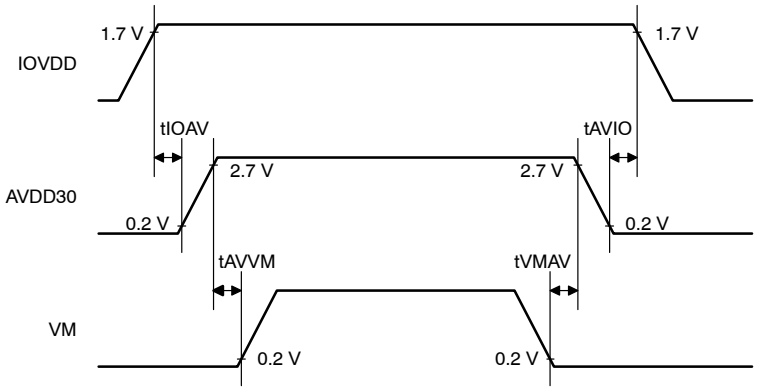


Figure 4.

Table 8.

Item	Symbol	Min	Typ	Max	Units
IOVDD ON to AVDD30 ON	tIOAV	0	–	–	ms
AVDD30 ON to VM ON	tAVVM	0	–	–	ms
VM OFF to AVDD30 OFF	tVMAV	0	–	–	ms
AVDD30 OFF to IOVDD OFF	tAVIO	0	–	*	ms

SDA, SCL, SSB, SCLK, MOSI, MISO, EIRQ1 and EIRQ2 tolerate 3 V input at the time of IOVDD power off.

SCL2 and SDA2 tolerate 3 V input at the time of AVDD30 power off.

The data in the Flash memory may be rewritten unintentionally if you do not keep specifications.

And it is forbidden to power off during Flash memory access. The data in the Flash memory may be rewritten unintentionally.

OIS,AF driver is recommended to set standby before VM power off.

*Please make IOPRSTB(D0_0064h, bit0) = 0 before turning OFF AVDD30 when AVDD30 is turned off with keeping IOVDD on.

2−wire Serial Interface Timing

The 2−wire serial interface timing definition and electric characteristics are shown below. The communication protocol is compatible with I^{2}C. This circuit has clock stretch function.

Static Address : 7'b0100100

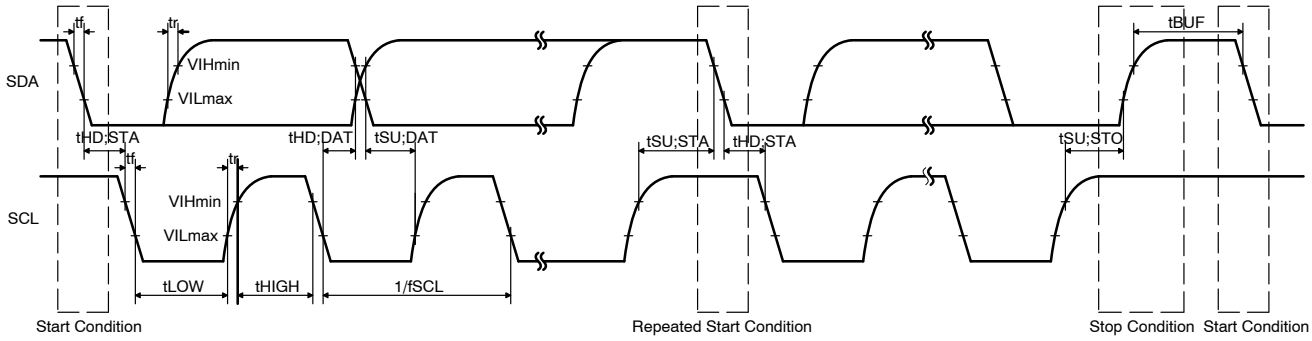


Figure 5.

Table 9.

Item	Symbol	Standard−mode		Fast−mode		Fast−mode Plus		Units
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	fSCL	−	100	−	400	−	1000	kHz
START condition hold time	tHD;STA	4.0	−	0.6	−	0.26	−	μs
SCL clock Low period	tLOW	4.7	−	1.3	−	0.5	−	μs
SCL clock High period	tHIGH	4.0	−	0.6	−	0.26	−	μs
Setup time for repetition START condition	tSU;STA	4.7	−	0.6	−	0.26	−	μs
Data hold time	tHD;DAT	0 (Note 3)	3.45	0 (Note 3)	0.9	0 (Note 3)	0.45	μs
Data setup time	tSU;DAT	250	−	100	−	50	−	ns
SDA, SCL rising time	tr	−	1000	−	300	−	120	ns
SDA, SCL falling time	tf	−	300	−	300	−	120	ns
STOP condition setup time	tSU;STO	4.0	−	0.6	−	0.26	−	μs
Bus free time between STOP and START	tBUF	4.7	−	1.3	−	0.5	−	μs

3. Although the I^{2}C specification defines a condition that 300 ns of hold time is required internally, this LSI is designed for a condition with typ. 25 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resister.

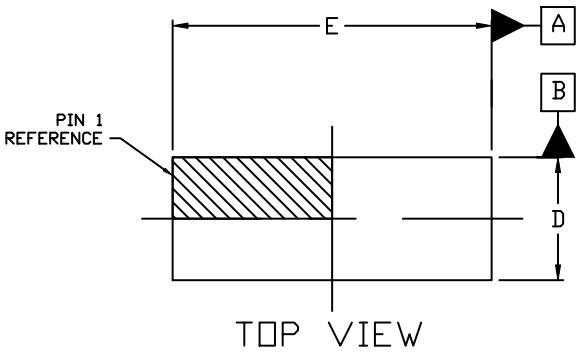
ORDERING INFORMATION

Part Number	Package	Shipping†
LC898129DP1XHTBG	WLCSP40 (Pb−Free, Halogen−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

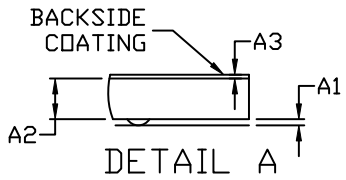
WLCSP40 1.60x4.15x0.33
CASE 567XS
ISSUE O

DATE 12 APR 2019

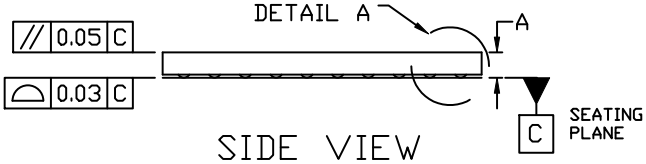


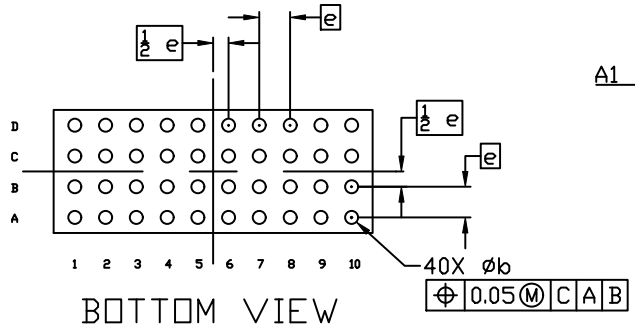
NOTES:

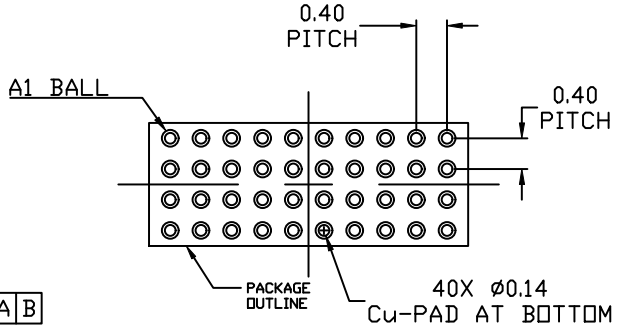
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.31	0.33	0.35
A1	0.034	0.040	0.046
A2	0.2525	0.2650	0.2775
A3	0.020	0.025	0.030
b	0.15	0.17	0.19
D	1.575	1.600	1.625
E	4.125	4.150	4.175
e	0.40 BSC		

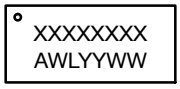






* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON05909H	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	WLCSP40 1.60x4.15x0.33	PAGE 1 OF 1

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