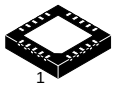
Programmable USB Type-C® and Power Delivery 3.1 Source Controller with PPS Support

FUSB15101



QFN20 4x4, 0.5P
CASE 485BH−01

The FUSB15101 is a highly integrated USB Power Delivery (PD) power source controller that can control the opto−coupler in the secondary side of an AC−DC adapter or a DC−DC port power regulator.

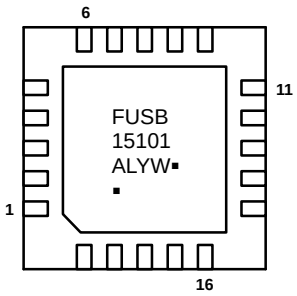
The FUSB15101 enables a complete solution for USB power sources through optimized hardware peripherals and complete open−source embedded firmware all in a compact solution.

It integrates a highly efficient Arm® Cortex®−M0+ processor with custom designed peripherals to seamlessly support USB PD 3.1 source applications. The FUSB15101 supports the PPS specification in USB PD, with a minimum of 3.3 V and a maximum of 21 V output voltage control. It includes Constant Voltage (CV) and Constant Current Limit (CL) control blocks, various protection mechanisms and high voltage tolerance on connector pins.

Key Features

- 32−bit Arm Cortex−M0+ Processor
- 32 KB OTP (One Time Programmable) Program Memory
- USB PD 3.1 with PPS Support
  - Power Management Unit with VIN Support from 3.3 V to 24 V
  - Integrated VCONN Supply for Interrogating E−Marked Cables
- Idle and Sleep Modes to Meet CoC and DoE Requirements
- Peripherals
  - USB Type−C / PD Detection and Communication Layer
  - VBUS NMOS Gate Driver for Load Switch Control
  - VBUS Discharge Functionality
  - Programmable Constant Voltage & Constant Current Control
  - Two 10−bit DAC's for Precise Voltage and Current Control
  - Two NTC Temperature Measurements
  - 10−bit ADC for Voltage, Current and Temperature Reporting
  - Two General Purpose 32−bit Timers
  - Watchdog Timer (WDT)
  - I^2C Master/Slave Peripheral
  - UART on D+/− Pins
- Output Fault Protection
  - Over−Voltage
  - Under−Voltage
  - Over−Current
  - Over−Temperature
- 20−pin QFN Package (4 mm x 4 mm, 0.5 P)

MARKING DIAGRAM



FUSB	= Specific Device Code
15101	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
FUSB15101MNTWG	QFN20 (Pb−Free)	4,000 / Tape & Reel

Typical Applications

- Wall Chargers for Mobile Phones and Tablets and Computing Devices
- AC−DC USB PD Compliant Adapters
- Power Banks
- Cigarette Lighter Adapters

Introduction

The FUSB15101 supports USB Type−C 2.1 and USB PD 3.1 specifications for power source applications with VBUS voltages ranging from 3.3 V to 21 V.

A highly flexible and open firmware environment allows hardware peripherals to be customized to meet a variety application needs.

Key integrated functions and peripherals are highlighted below:

- *Arm Cortex−M0+*: A 32−bit core with flexible clocking up to 12 MHz.
- *Memories*: A total of 32 kB of One Time Programmable Memory (OTP) is available to store program code; 2 KB of SRAM program memory.
- *USB Type−C and PD*: Integrated USB PD PHY and Type−C termination/comparators supporting latest USB−IF specification. Open and customizable USB PD firmware stack allows for tailored vendor specific functions.
- *Integrated VCONN Switch*: Provides power to cable eMarkers to interrogate current capabilities.
- *CC/CV Control*: Firmware controlled feedback voltage and current loop operation with programmable voltage and current DACs, Cable Drop Compensation, OVP, UVP and OCP.
- *Current Sense Amplifier*: Programmable for use with 5 mΩ or 10 mΩ sense resistors.
- *High Voltage Protection*: 26 V DC tolerant BLD, CC and D+/−.
- *ADC*: 10−bit ADC for accurate monitoring of VBUS voltage and current, external temperatures or voltages.
- *I^2C*: Serial communication port capable of acting as a host or device.
- *UART*: UART peripheral available via HVDP/DM.
- *GPIOs*: Fully programmable I/Os with internal terminations. Configurable as input or output (CMOS or open−drain).
- *Multiple Timers*: Three independent 32−bit timers are available: 1 General Purpose, 1 Watchdog, and 1 Wake−up / General Purpose.
- *Dual External NTC*: Integrated current sources are used in conjunction with the ADC to monitor a variety of NTC resistors.
- *Low Power Operation Modes*: Programmable Sleep Modes allowing the device to minimize power usage as needed. Automatic USB−C detection and weak−up functionality from sleep modes.
- *Temperature Range*: Extended operating temperature range of −40°C to 105°C.

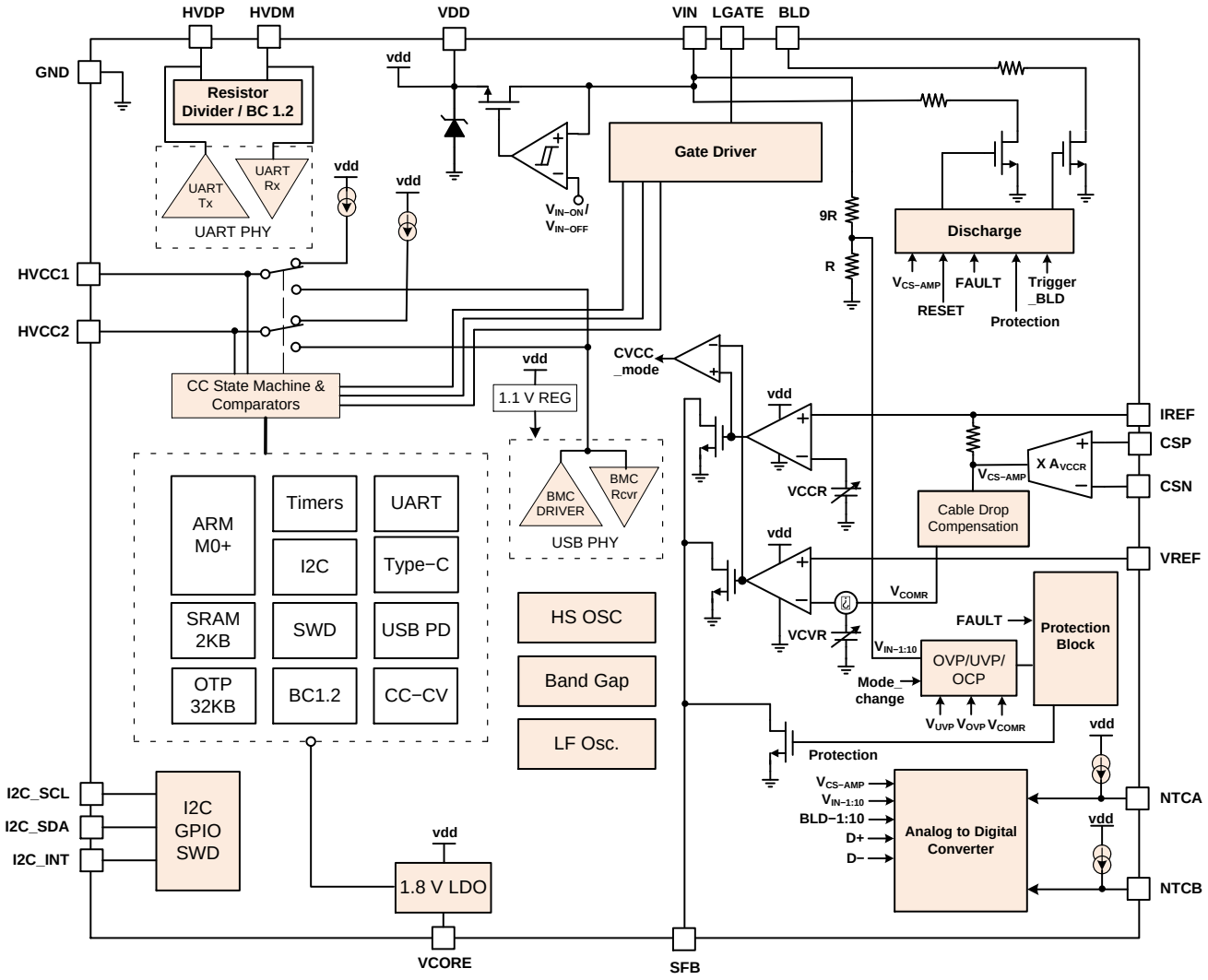


Figure 1. Simplified Block Diagram

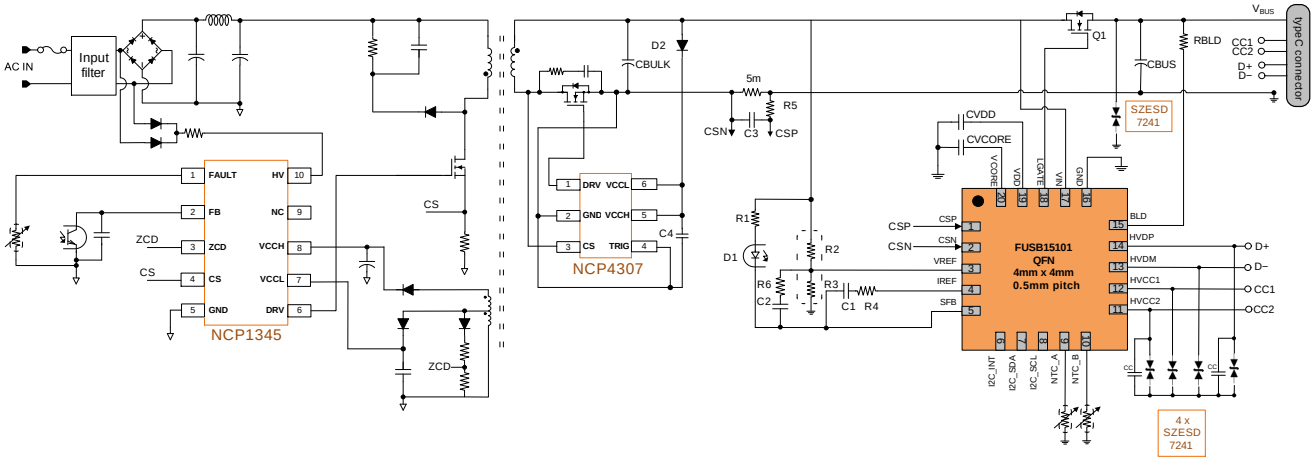


Figure 2. AC/DC Application Schematic

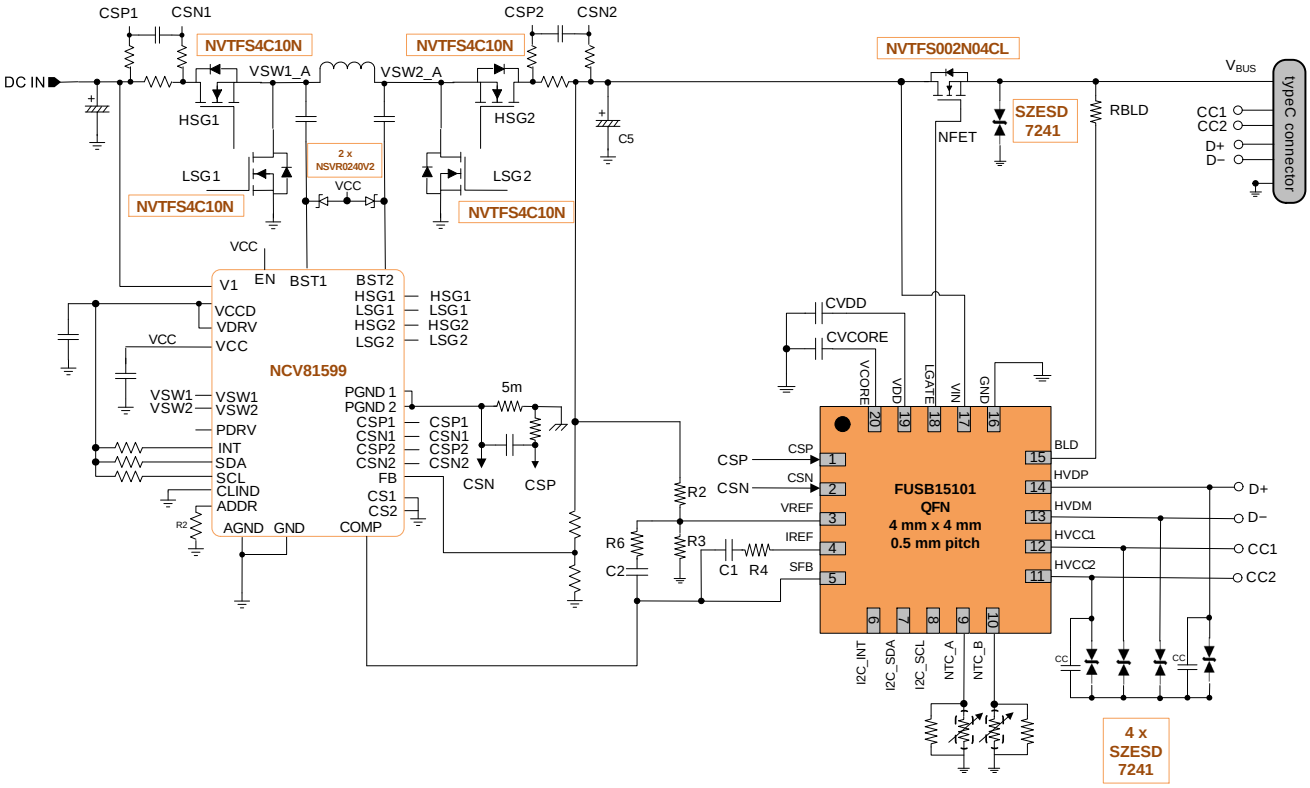


Figure 3. DC/DC Application Schematic

PIN CONNECTIONS

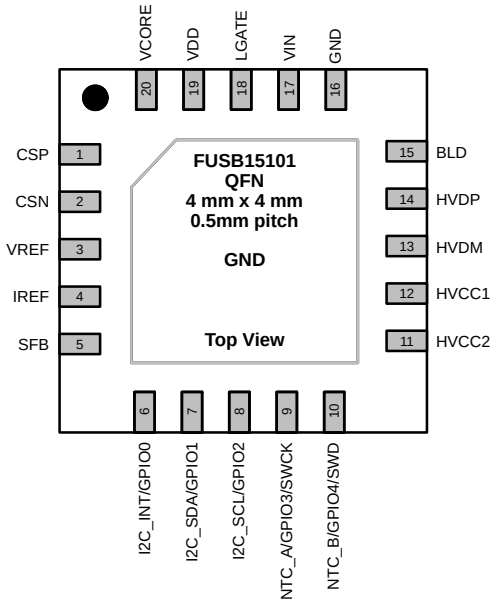


Figure 4. QFN20 Top−View

PIN FUNCTION DESCRIPTION

Pin #	Name	Description
1	CSP	Current Sensing Amplifier Positive Terminal. Connect this pin directly to the positive end of the current sense resistor with a short PCB trace.
2	CSN	Current Sensing Amplifier Negative Terminal . Connect this pin directly to the negative end of the current sense resistor with a short PCB trace.
3	VREF	Output Voltage Sensing Voltage. This pin is used for CV regulation, and it is tied to the internal CV loop amplifier non−inverting input terminal. It is tied to the output voltage resistor divider.
4	IREF	Constant Current Amplifying Signal. The voltage level on this point is the amplified current sense signal. This pin is tied to the internal CC loop amplifier's non−inverting input terminal.
5	SFB	Secondary Feedback. Common output of the dual OTA open drain operational amplifiers. Typically, an opto−coupler is connected to this pin to provide feedback to the primary side PWM controller.
6	I2C_INT/GPIO0	I^2C Interrupt Signal / General Purpose I/O
7	I2C_SDA/GPIO1	I^2C Data Signal / General Purpose I/O
8	I2C_SCL/GPIO2	I^2C Clock Signal / General Purpose I/O
9	NTC_A/GPIO3/SWCK	An external NTC can be connected to this pin / General purpose I/O/SWCK.
10	NTC_B/GPIO4/SWD	An external NTC can be connected to this pin / General purpose I/O/SWCK.
11	HVCC2	Configuration Channel 2. This pin is used to detect USB Type−C devices and communicate over USB PD when applicable.
12	HVCC1	Configuration Channel 1. This pin is used to detect USB Type−C devices and communicate over USB PD when applicable.
13	HVDM	USB Communication Interface. This pin is tied to the USB D− data line input.
14	HVDP	USB Communication Interface. This pin is tied to the USB D+ data line input.
15	BLD	Bleeder pin. This pin is tied to VBUS after the load switch to discharge VBUS.
16	GND	Ground reference for IC
17	VIN	Output voltage (Input voltage to the FUSB15101). This pin is tied to the output of the adapter to monitor its output voltage and supply internal bias.
18	LGATE	Load switch gate drive signal. This pin is tied to the gate of the load switch.
19	VDD	Internal 5 V supply voltage.
20	VCORE	Internal 1.8 V supply voltage for the MCU core.
DAP	GND	Connect to GND Plane for thermal dissipation.

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS (Notes 1, 2)

Symbol	Parameter	Min	Typ	Max	Unit
V_{USB}	D+/− and CC Connector Pins	−0.3	−	26	V
V_{IO}	I/O Voltage	−0.5	−	6.0	V
V_{NTC}	NTC_A and NTC_B Pin Voltage	−0.5	−	6.0	V
V_{VREF}	VREF Pin Input Voltage	−0.5	−	6.0	V
V_{IREF}	IREF Pin Input Voltage	−0.5	−	6.0	V
V_{CSx}	CSP and CSN Pins Input Voltages	−0.5	−	6.0	V
V_{DC}	VDD Pin Input Voltage	−0.5	−	6.0	V
V_{CORE}	VCORE Pin Input Voltage	−0.5	−	2.0	V
V_{LGATE}	LGATE Pin Input Voltage	−0.3	−	31	V
V_{SFB}	SFB Pin Input Voltage	−0.3	−	26	V
V_{IN}	VIN Pin Input Voltage	−0.3	−	26	V
V_{BLD}	BLD Pin Input Voltage	−0.3	−	26	V
ESD_{HBM}	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012 (Note 2)	4	−	−	kV
ESD_{CDM}	Charged Device Model, JESD22−C101 (Note 2)	2	−	−	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. Meets JEDEC standards JS−001−2012 and JESD 22−C101.

OPERATING RATINGS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Functional Range for Supply Input	3.135	5.0	24	V
V_{HVCC}	Communication Channel Pins	0	−	5.5	V
$V_{HVDP/DM}$	D+/− USB Voltage	0	−	3.6	V
V_{IO}	GPIO, I2C, RESET	0	−	5.5	V
T_J	Junction Temperature	−40	−	+125	°C
T_A	Operating Ambient Temperature	−40	−	+105	°C
V_{CORE}	VCORE Pin Voltage	0	−	1.9	V
V_{VDD}	VDD Pin Voltage	4.75	−	5.5	V
V_{NTC_X}	NTC_/B Pin Voltage	0	−	1.28	V
V_{REF}	VREF Pin Voltage	0	−	2.2	V
I_{REF}	IREF Pin Voltage	0	−	1.8	V
V_{CSP}	CSP Voltage	0	−	0.063	V
V_{CSN}	CSN Pin Voltage	−	0	−	V
V_{SFB}	SFB Pin Voltage	0	−	22.5	V
V_{LGATE}	LGATE Pin Voltage	0	−	25	V
V_{BLD}	BLD Pin Voltage	0	−	22.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL CHARACTERISTICS (Note 3)

Symbol	Characteristic	Value	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance	38.6	°C/W
θ_{JC}	Junction−to−Case Thermal Resistance	4.2	°C/W

3. Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with two−layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature T_J(max) at a given ambient temperature T_A.

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.135 V to 22.5 V, TA = −40°C to +105°C unless otherwise noted. Typical values are at TA = 25°C, VIN = 5.0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INTERNAL POWER SUPPLY						
VIN						
$I_{IN-OP-5V}$	Operating Supply Current at 5 V	Attached, PD Communication in progress, ADCs enabled, NTCs enabled, CC & CV enabled, Gate Driver Enabled. VIN = 5 V, VCS = −25 mV, RCS = 5 mΩ	−	3.5	−	mA
$I_{IN-OP-20V}$	Operating Supply Current at 20 V	Attached, PD Communication in progress, ADCs enabled, NTCs enabled, CC & CV enabled, Gate Driver Enabled. VIN = 20 V, VCS = −25 mV, RCS = 5 mΩ	−	4.4	−	mA
$I_{IN-Sleep}$	Operating Supply Current at Sleep Mode	No Device Attached, Type−C enabled & Gate Driver OFF or BC1.2 Detection enabled & Gate Driver ON; VIN = 5 V, VCS = 0 V excluding IP−CC1 and IP−CC2 Supply Current and ISFB Current	−	−	0.75	mA
V_{IN-ON}	IC Turn−On Threshold Voltage	Increase VIN	2.9	3.2	3.4	V
V_{IN-OFF}	IC Turn−Off Threshold Voltage	VIN > VIN−ON then decrease VIN	2.75	2.875	3.0	V
$t_{VIN-off-Debounce}$	IC Turn−Off Debounce Time	VIN > VIN−ON then decrease VIN	−	−	200	μs
$t_{VIN-OCP-Debounce}$	Hardware OCP Debouce on Both Edges	Entering and exiting OCP Mode	−	50	100	μs
$V_{LATCH-OFF}$	Output Voltage Release Latch Mode	VIN Falling	−	−	1.55	V
$t_{VIN-OVP-Debounce}$	VIN OVP Debounce Time		35	75	110	μs
$V_{IN-OVP-MAX}$	VIN Maximum Overvoltage Protection		24	−	26	V
$V_{IN-UVP-PPS}$	Turn−Off Threshold Voltage when in a PPS Contract	VIN Falling in a PPS contract	2.805	2.97	3.135	V
VIN UVP SECTION						
$K_{IN-UVP-60}$	Ratio VIN Under−Voltage−Protection (UVP) to VIN	VCS = 0 mV	57.5	60	62.5	%
$K_{IN-UVP-65}$		VCS = 0 mV	60	65	70	
$K_{IN-UVP-70}$		VCS = 0 mV	67.5	70	72.5	
$K_{IN-UVP-80}$		VCS = 0 mV	77	80	83	
$K_{IN-UVP-90}$		VCS = 0 mV	87	90	93	
$K_{IN-UVP-95}$		VCS = 0 mV	92	95	98	

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.135 V to 22.5 V, TA = −40°C to +105°C unless otherwise noted. Typical values are at TA = 25°C, VIN = 5.0 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIN OVP SECTION						
$K_{IN-OVP-105}$	Ratio VIN Over−Voltage−Protection (OVP) to VIN	VCS = 0 mV	102	105	108	%
$K_{IN-OVP-110}$		VCS = 0 mV	107	110	113	
$K_{IN-OVP-115}$		VCS = 0 mV	112	115	118	
$K_{IN-OVP-120}$		VCS = 0 mV	117	120	123	
$K_{IN-OVP-125}$		VCS = 0 mV	122	125	128	
$K_{IN-OVP-130}$		VCS = 0 mV	127	130	133	
$K_{IN-OVP-135}$		VCS = 0 mV	132	135	138	
VDD						
V_{DD}	VDD Source Voltage > 6 V	VIN = 6 V to 22.5 V, IVDD = 10 mA	4.75	5.125	5.5	V
I_{DD}	VDD Source Current Capability	VIN = 3.3 V, VDD = 2.9 V	10	−	−	mA
TYPE−C AND PD						
USB PD PHY						
TRANSMITTER						
UI	Unit Interval		3.03	3.33	3.7	μs
$p_{BitRate}$	Maximum Difference between the bit−rate During the Payload and Last 32 Bits of Preamble		−	−	0.25	%
$t_{EndDriveBMC}$	Time to Cease Driving the Line after the End of the Last Bit of the Frame		−	−	23	μs
$t_{HoldLowBMC}$	Time to Cease Driving the Line after the Final High−to−low Transition		1	−	−	μs
$t_{InterFrameGap}$	Any PD Transmission Cannot be Sent out before a Dead Time of at Least tInterFrameGap from Receiving or Sending a Packet		25	−	−	μs
$t_{Fall-CC}$	Fall Time	10 % and 90 % amplitude points, minimum is under an unloaded condition.	300	−	−	ns
$t_{Rise-CC}$	Rise Time	10 % and 90 % amplitude points, minimum is under an unloaded condition.	300	−	−	ns
$t_{StartDrive}$	Time before the Start of the First Bit of the Preamble when the Transmitter Shall Start Driving the Line		−1	−	1	μs
V_{Swing}	BMC Voltage Swing		1.05	1.125	1.2	V
Z_{Driver}	TX Output Impedance at 750 kHz with an External 220 pF or Equivalent Load		33	−	75	Ω
RECEIVER						
$C_{Receiver}$	Receiver Capacitance when Driver isn't Turned On	Vrms = 0.371; Vdc = 0.5 V; Freq. = 1 MHz	−	75	−	pF
$t_{RxFilter}$	Rx Bandwidth Limiting Filter		100	−	−	ns
$t_{TransitionWindow}$	Time Window for Detecting Non−idle		12	−	20	μs
Z_{BmcRx} (Note 5)	Receiver Input Impedance		1	−	−	MΩ

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.135 V to 22.5 V, TA = −40°C to +105°C unless otherwise noted. Typical values are at TA = 25°C, VIN = 5.0 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TYPE−C FRONT END						
$R_{BLD-LEAK}$	BLD Pin Impedance to GND when VBUS is not Sourced	BLD = 0 V to 5.75 V; LGATE = OFF	72.4	−	−	kΩ
I_{180_CCX}	SRC 180 μA CC Current (1.5 A)		166	180	194	μA
I_{330_CCX}	SRC 330 μA CC Current (3 A)		304	330	356	μA
R_{DEVICE}	Device Pull−down Resistance		4.6	5.1	5.6	kΩ
R_A	Ra		800	−	1200	Ω
Z_{OPEN}	CC Resistance for Disabled State, when VDD is Valid		126	−	−	kΩ
I_{VCONN}	Maximum Current for VCONN Source	VIN = 4.75 V	34	−	−	mA
$V_{RdSRC3.0}$	Source Attach Threshold for CC Pin at 3 A Current		2.45	2.6	2.75	V
$V_{RaSRC3.0}$	Source Ra Threshold for CC Pin at 3 A Current		0.75	0.8	0.85	V
V_{OVP_CC}	CCx OVP Threshold		5.6	−	6.0	V
$t_{VCONN-OCP}$	VCONN OCP Debounce Time		2.5	3.5	4.5	ms
$t_{CC-OVP-Debounce}$	CC1/CC2 OVP Debounce Time		−	100	125	μs
$t_{CC-OVP-Debounce-Recover}$	Debounce Time after CC OVP Event		−	15	−	ms
I_{VCONN_OCP}	Over Current Protection (OCP) Limit at which VCONN Switch Shuts Off		50	−	−	mA
V_{VCONN}	Voltage Range for VCONN Source		3.0	−	5.5	V
VBUS CONTROL						
LOAD SWITCH						
$V_{LGATE-3.3V}$	Gate High Voltage at 3.3 V	VIN = 3.3 V	8.1	−	−	V
$V_{LGATE-20V}$	Gate High Voltage at 20 V	VIN = 20 V	23.5	−	−	V
$V_{LGATE-OVP-Max}$	Gate High Voltage at VIN−OVP−Max	VIN = VIN−OVP−Max	−	−	31.5	V
BLEEDER						
$I_{VIN-Sink}$	VIN Sinking Current During tBLD	Bleeding current on VIN at VIN = 20 V	60	−	−	mA
$I_{BLD-Sink}$	BLD Sinking Current During tBLD	Bleeding current on BLD at BLD = 20 V	250	−	−	mA
VBUS MEASUREMENT						
$V_{Safe0V-THR}$	Safe Operating Voltage at “Zero Volts”.		0.6	−	0.8	V
CLOCKS						
f_{LS_CLK}	Low Speed Clock for Idle, Type−C and ADC		232.8	240	247.2	kHz
f_{HS_CLK}	Internal Clock for PD, I^2C and MCU Core		11.4	12	12.6	MHz
TEMPERATURE PROTECTION						
T_{SHUT}	Temperature Threshold for Internal Circuit Protection		−	145	−	°C
T_{HYS}	Over Temperature Hysteresis		−	10	−	°C

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.135 V to 22.5 V, TA = −40°C to +105°C unless otherwise noted. Typical values are at TA = 25°C, VIN = 5.0 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BC1.2						
R_{DCP}	DCP Emulation Resistance	V_{HVDP} or V_{HVDM} = 0 V, 1.0 V, ION = 2 mA	−	75	140	Ω
R_{Dx-DWN}	DP/DM Pull Down Resistance	V_{HVDP} or V_{HVDM} = 0 V − 3.6 V	16	19.5	23	kΩ
I_{DX-SNK}	Sink Current to Dx	VDD = 3.0 V to 5.5 V	25	100	175	μA
$R_{DAT-LKG}$	Resistor Weak Pull−Down on D+ and D−	V_{HVDP} or V_{HVDM} = 0 V to 3.6 V	300	700	1100	kΩ
V_{Dx-SRC}	Source Voltage	VDD = 3.0 V to 5.5 V	0.5	0.6	0.7	V
USB2.0 PORT CHARACTERISTICS						
$I_{OFF-USB}$	Power−Off Leakage Current	All data ports, V_{HVDP} or V_{HVDM} = 3.6 V, VDD = 0 V	−	−	18	μA
C_{USB2}	HVDP/HVDM Capacitance	f=240 MHz; V_{HVDP} or V_{HVDM} = 400 mV Vpk−pk	−	2.4	−	pF
$V_{OVP-VIH-USB}$	HVDP/DM Rising over Voltage Threshold		4.4	4.55	4.7	V
$V_{OVP-VIL-USB}$	HVDP/DM Falling over Voltage Threshold		−	4.35	−	
$t_{OVP-USB}$	USB OVP Event Recovery Time	HVDP/HVDM Over Voltage debounce	−	100	125	μs
$t_{OVP-USB-Recover}$	USB OVP Event Recovery Time	USB OVP event removed	−	15	−	ms
MOISTURE DETECTION (HVDM PIN)						
$V_{SRC-MOIS}$	Voltage Source for Moisture Detection		.9	1.0	1.1	V
$R_{PU-MOIS}$	High Pull up Resistor for Moisture Detection		250	300	352	kΩ
$R_{PU-MOS-LO}$	Low Pull Up Resistor for Moisture Detection		2.25	2.5	2.75	kΩ
SERIAL WIRE DEBUG INTERFACE						
$f_{SWD-CLK}$	Serial Wire Debug Input Clock Frequency		−	−	4	MHz
$t_{SWDI-SET}$	Serial Wire Debug Data Setup Timing		0.25 x (1/ SWD_CLK)	−	−	ns
$t_{SWDI-HOLD}$	Serial Wire Debug Data Hold Timing		0.25 x (1/ SWD_CLK)	−	−	ns
$V_{SWD-VIH}$	Serial Wire Debug Input Voltage Threshold	VIN = 3.1 V to 22.5 V	0.7 x VDD	−	−	V
$V_{SWD-VIL}$		VIN = 3.1 V to 22.5 V	−	−	0.3 x VDD	
$V_{SWD-HYS}$	Serial Wire Debug Input Voltage Hysteresis	VIN = 3.1 V to 22.5 V	−	300	−	mV
$I_{SWD-LKG}$	Serial Wire Debug Input Leakage	VIN = 3.1 V to 22.5 V Input Voltage 0 V to 5.5 V	−10	−	+10	μA
$V_{SWD-VOH}$	Serial Wire Debug Output Voltage High	VIN = 3.1 V to 22.5 V, Iout = −2 mA	VDD − 0.5	−	−	V
$V_{SWD-VOL}$	Serial Wire Debug Output Voltage Low	VIN = 3.1 V to 22.5 V, Iout = +4 mA	−	−	0.4	V

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.135 V to 22.5 V, TA = −40°C to +105°C unless otherwise noted. Typical values are at TA = 25°C, VIN = 5.0 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I/OS						
GPIO						
$V_{GPIO-VIH}$	High Level Input Voltage	VIN = 3.1 V to 22.5 V	0.7 x VDD	−	−	V
$V_{GPIO-IL}$	Low Level Input Voltage	VIN = 3.1 V to 22.5 V	−	−	0.3 x VDD	V
$V_{GPIO-VOH}$	Output High Voltage	VIN = 3.1 V to 22.5 V, Iout = −2 mA	VDD − 0.5	−	−	V
$V_{GPIO-VOL}$	Ouptut Low Voltage	VIN = 3.1 V to 22.5 V, Iout = +4 mA	−	−	0.4	V
$V_{GPIO-HYS}$	Input Hysteresis	VIN = 3.1 V to 22.5 V, 5.0 V Typ	−	300	−	mV
$I_{IN-GPIO}$	Input Leakage	VIN = 3.1 V to 22.5 V, Input Voltage 0 V to 5.5 V	−10	−	5	μA
$I_{OFF-GPIO}$	Off Input Leakage	VIN = 0 V, Input Voltage 0 V to 5.5 V	−5	−	5	μA
$R_{PD-GPIO}$	Pull−Down Resistance	PORT_PDx = 1	−	100	−	kΩ
$R_{PU-GPIO}$	Pull−Up Resistance	PORT_PUx = 1	−	100	−	kΩ
C_{GPIO}	Pin Capacitance		−	5	−	pF
NTC						
I_{NTCA}	Current Source on NTCA		55	60	65	μA
I_{NTCB}	Current Source on NTCB		55	60	65	μA
I²C						
IO						
I_{CCTI2C}	VDD Current when SDA or SCL is HIGH	VIN = 3.1 V to 22.5 V, VSDA/VSCL = 1.8 V	−10	−	10	μA
I_{I2C}	Input Current of SDA and SCL Pins	VIN = 3.1 V to 22.5 V, VI = 0 V to 5.5V	−10	−	10	μA
V_{IH-I2C}	High−Level Input Voltage	VIN = 3.1 V to 22.5 V	1.2	−	−	V
V_{IL-I2C}	Low−Level Input Voltage	VIN = 3.1 V to 22.5 V	−	−	0.4	V
$V_{OL1-I2C}$	Low−Level Output Voltage at 3 mA Sink Current (Open−Drain)	VIN = 3.1 V to 22.5 V	−	−	0.3	V
$V_{hys-I2C}$	Hysteresis of Schmitt Trigger Inputs	VIN = 3.1 V to 22.5 V	−	0.2	−	V
I_{OL-SDA}	Low−Level Output Current (Open−Drain)	VIN = 3.1 V to 22.5 V, V_OL = 0.4 V (Note 4)	20	−	−	mA
V_{OL-INT}	INT_N Output Low Voltage	VIN = 3.1 V to 22.5 V, I_OL = 4 mA	−	−	0.4	V
C_{I2C}	Capacitance for Each I/O Pin	VIN = 3.1 V to 22.5 V	−	5	−	pF
$V_{OL2-I2C}$	Low−Level Output Voltage at 2 mA Sink Current (Open−Drain)	VIN = 3.1 V to 22.5 V	−	−	0.3	V
t_{SP-I2C}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter		−	−	50	ns
V_{IH_INT}	High−Level Input Voltage	VIN = 3.1 V to 22.5 V	1.2	−	−	V
V_{IL_INT}	Low−Level Input Voltage	VIN = 3.1 V to 22.5 V	−	−	0.4	V
CV/CC CONTROL						
CONSTANT CURRENT SENSE SECTION						
$A_{V-CCR-40}$	Current Sense Amplifier Gain	RCS = 5 mΩ	−	40	−	V/V
$A_{V-CCR-20}$		RCS = 10 mΩ	−	20	−	
I_{CS-1A}	Current Threshold on Sensing Resistor between CSP and CSN at IOUT = 1.00 A	Constant Current Limit mode and VCC = 5 V, 20 V	0.85	1.00	1.15	A

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.135 V to 22.5 V, TA = −40°C to +105°C unless otherwise noted. Typical values are at TA = 25°C, VIN = 5.0 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CONSTANT CURRENT SENSE SECTION						
I_{CS-2A}	Current Threshold on Sensing Resistor between CSP and CSN at IOUT = 2.00 A	Constant Current Limit mode and VCC = 5 V, 20 V	1.85	2.00	2.15	A
I_{CS-3A}	Current Threshold on Sensing Resistor between CSP and CSN at IOUT = 3.00 A	Constant Current Limit mode and VCC = 5 V, 20 V	2.85	3.00	3.15	A
I_{CS-4A}	Current Threshold on Sensing Resistor between CSP and CSN at IOUT = 4.00 A	Constant Current Limit mode and VCC = 5 V, 20 V	3.80	4.00	4.20	A
I_{CS-5A}	Current Threshold on Sensing Resistor between CSP and CSN at IOUT = 5.00 A	Constant Current Limit mode and VCC = 5 V, 20 V	4.75	5.00	5.25	A
$I_{CS-STEP}$	Current Threshold on Sensing Resistor between CSP and CSN at ΔIOUT = 50 mA	Constant Current Limit mode and VCC = 5 V	48	50	52	mA
$I_{CS-EN-BLD}$	Real Current Threshold to Enable Bleeder	VBUS_BLD_EN = 1	200	450	700	mA
$t_{CS-EN-BLD}$	Enable Bleeder Debounce Time	VBUS_BLD_EN = 1	−	0.6	1	ms
OVER CURRENT PROTECTION SENSING SECTION						
$V_{CS-3.6A}$	Voltage Difference between CSP and CSN at Nominal 3.6 A	Rcs = 5 mΩ; ccdac_refp = 10b (120%); csa_multiplier =1 (40x)	16.92	18	19.08	mV
V_{CS-6A}	Voltage Difference between CSP and CSN at Nominal 6.0 A	Rcs = 5 mΩ; ccdac_refp = 10b (120%); csa_multiplier =1 (40x)	28.5	30	31.5	mV
CONSTANT VOLTAGE SENSE SECTION						
$V_{CVR-3.3V}$	CV Reference Voltage at 3.3 V	VIN = 3.3 V, VCS = 0 V	0.32	0.33	0.34	V
$V_{CVR-5.0V}$	CV Reference Voltage at 5.0 V	VIN = 5.0 V, VCS = 0 V	0.485	0.5	0.515	V
$V_{CVR-9.0V}$	CV Reference Voltage at 9.0 V	VIN = 9.0 V, VCS = 0 V	0.873	0.9	0.927	V
$V_{CVR-12V}$	CV Reference Voltage at 12 V	VIN = 12 V, VCS = 0 V	1.164	1.200	1.236	V
$V_{CVR-15V}$	CV Reference Voltage at 15 V	VIN = 15 V, VCS = 0 V	1.455	1.500	1.545	V
$V_{CVR-20V}$	CV Reference Voltage at 20 V	VIN = 20 V, VCS = 0 V	1.940	2.000	2.060	V
$V_{CVR-STEP-20mV}$	CV Reference Voltage of 20 mV Step	delta VIN = 20 mV, VCS = 0 V	1.940	2.000	2.060	mV
CABLE DROP COMPENSATION						
$V_{COMR-CDC-0}$	Cable Compensation Voltage on VCVR for VOUT = 0 mV/A	RCS = 5 mΩ, VCS = −5 mV	−	0	−	mV
$V_{COMR-CDC-50}$	Cable Compensation Voltage on VCVR for VOUT = 50 mV/A	RCS = 5 mΩ, VCS = −5 mV	−	5	−	mV
$V_{COMR-CDC-100}$	Cable Compensation Voltage on VCVR for VOUT = 100 mV/A	RCS = 5 mΩ, VCS = −5 mV	−	10	−	mV
$V_{COMR-CDC-150}$	Cable Compensation Voltage on VCVR for VOUT = 150 mV/A	RCS = 5 mΩ, VCS = −5 mV	−	15	−	mV
$V_{COMR-CDC-200}$	Cable Compensation Voltage on VCVR for VOUT = 200 mV/A	RCS = 5 mΩ, VCS = −5 mV	−	20	−	mV
$V_{COMR-CDC-250}$	Cable Compensation Voltage on VCVR for VOUT = 250 mV/A	RCS = 5 mΩ, VCS = −5 mV	−	25	−	mV
FEEDBACK SECTION						
$I_{SFB-Sink-MAX}$	SFB Maximum Sinking Current During Regulation	Minimum guaranteed sink current expected from SFB pin	2	−	−	mA

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.135 V to 22.5 V, TA = −40°C to +105°C unless otherwise noted. Typical values are at TA = 25°C, VIN = 5.0 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UART						
$V_{UART-VIH}$	High−Level Input Voltage	VIN = 3.5 V − 22.5 V	2	−	−	V
$V_{UART-VIL}$	Low−Level Input Voltage	VIN = 3.5 V − 22.5 V	−	−	0.8	V
$V_{UART-HYS}$	Input Hysteresis	VIN = 3.5 V − 22.5 V	−	200	−	mV
$V_{UART-VOL}$	Output Low Voltage	VIN = 3.5 V − 22.5 V, Iout = 2 mA	−	−	0.4	V
$V_{UART-VOH}$	UART High Output Voltage	VIN = 3.5 V − 22.5V, Iout = −2 mA	2.9	−	−	V
$t_{UART-tR}$	Rise Time of UART Tx	10%−90%, VIN = 3.5 V − 22.5 V, Cl = 20 pF	−	250	−	ns
$t_{UART-tFall}$	Fall Time of UART Tx	90% to 10%, VIN = 3.5 V − 22.5 V, Cload = 20 pF	−	250	−	ns
UART−BAUD (Note 5)	UART BAUD Rate Range Supported	Transmit and receive fall within 10% of BAUD Rate set, including min and max	9600	−	230400	bps

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Note (20 mA guaranteed over −40°C to 85°C)
5. Guaranteed by Design

Arm Cortex−M0+ Processor

The FUSB15101 integrates an Arm Cortex−M0+ processor with Nested Vector Interrupt Controller (NVIC), Wake−up Interrupt Controller (WIC), and Debug Access Port (DAP). The processor uses the Thumb instruction set and is optimized for high performance with reduced code size and low power operation. The Arm Cortex−M0+ efficiently handles multiple parallel peripherals and has integrated sleep modes. Test and debug capability are enhanced with the Arm Serial Wire Debug Port.

The Arm implementation in the FUSB15101 includes a 32 kB OTP and 2 kB of SRAM. The MCU, Memory and DAP are interconnected using the AMBA (Advanced Microcontroller Bus Architecture) AHB−Lite interface and peripherals are connected to the AHB via APB interface (Advanced Peripheral Bus).

In addition to the base Arm Cortex−M0+ processor interrupts, the FUSB15101 implements multiple external source interrupts for peripheral devices. A powerful nested, pre−emptive and priority−based interrupt handling system assures timely and flexible response to external events.

Low power features on FUSB15101 include the WIC, adjustable clock rates, and different software−controlled power modes to maximize opportunities to save power in the final application.

Reset Sources

The FUSB15101 has various sources of reset including:

- *Internal Power−On Reset* − The Internal Power−On Reset asserts when VIN supply is below threshold levels for proper operation. It resets the entire chip including core, debug port, peripherals, wakeup timer, and watchdog.
- *Software Issued Reset* − The software reset can be called by writing to a given register in the Cortex address space. It is typically called on exit from a processor exception. Software reset resets the entire chip including core, peripherals, wakeup timer, and watchdog.
- *Watchdog Timer Reset* − The watchdog timer reset is caused by the watchdog timeout and is used to prevent errant software from locking up the device. The watchdog reset resets the entire chip including core, debug port, peripherals, and watchdog. The watchdog timer is disabled upon power up and must be enabled by software. The watchdog is not paused when the debugger halts the processor.

Power and Sleep Behavior

The FUSB15101 has been optimized to conserve power by utilizing peripheral interrupts and hardware autonomy. The device can be configured via firmware to enter low power states, disable unneeded peripherals and scale clock frequencies based on different application needs.

The Type−C block is designed to function at the lowest power states and will automatically wake when a Type−C attach is detected. This minimizes total power consumption when no device is attached.

Clock Sources

FUSB15101 implements a dual oscillator architecture to minimize power consumption.

- A 12 MHz internal RC oscillator to enable full functionality.
- A 240 kHz internal RC oscillator that can be used for very low power sleep modes

Timers

- *32−bit General Purpose Timer* − FUSB15101 has a 32−bit down−counter that can generate an interrupt request signal, status, when the counter reaches 0. The timing resolution depends on the programmable clock source and pre−scale ratios/
- *32−bit Wake−up Timer (WUT)* − The main purpose of the wakeup timer is to facilitate scheduled exit from low power modes. It can also be used for general purpose event timing.
- *32−bit Watchdog Timer (WDT)* − The watchdog timer applies a reset to the system in the event of a software failure, providing a way to recover from software crashes. The watchdog timer is disabled by default and must be enabled through software. The watchdog is protected with a lock mechanism to prevent rogue software from disabling the watchdog functionality. A special value has to be written to the lock register to access watchdog control. The watchdog timer is clocked from the same oscillator as the core, which can be LS_CLK or HS_CLK.

Serial Wire Debug Interface (SWD)

The Arm M0+ implementation includes a Debug Access Port (DAP). The debug mode implementation includes 4 hardware breakpoints and 2 hardware watch points. The Debug Access Port interface implementation is the Arm Serial Wire Debug Port (SW−DAP) connected to Pins SWCLK and SWDIO. The Serial Wire Debug Port Interface uses a single bi−directional data connection. Each operation consists of three phases: Packet request, Acknowledge response, and Data transfer phase. Use any Serial Wire Debug (SWD) compliant hardware debugger interface to interact with the internals of the FUSB15101.

USB Type−C & PD Peripheral Overview

The USB Type−C and PD peripheral is a fully compliant USB solution. This peripheral consists of an analog front end and a digital state machine. Firmware implements the higher−level protocol and policy layers whereas the analog and digital components can perform lower−level PD protocol and PHY layer functions.

The Type−C block includes all terminations and comparators required for Source/Sink/DRP operation: plug orientation detection, power capability advertisement and power role detection.

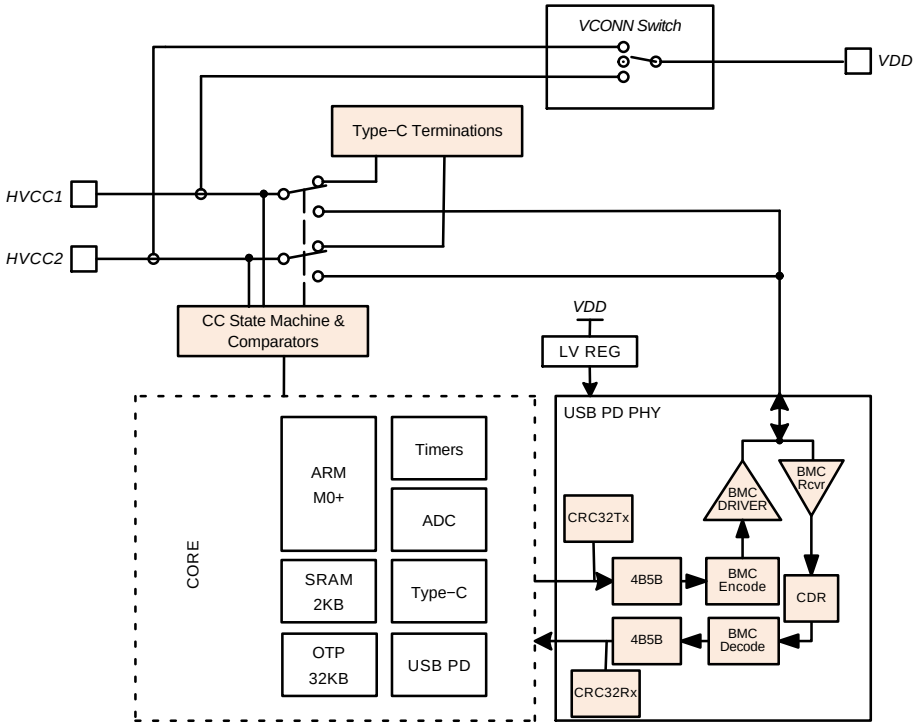


Figure 5. USB Type−C and PD

VCONN Switch

Some applications require that a VCONN voltage be sourced in order to provide additional source capabilities when sourcing greater than 3 A on VBUS. The level of over−current protection on VCONN is fixed at 50 mA.

USB PD PHY State Machine Logic

The FUSB15101 PD module includes the following digital functions to enable USB PD messaging:

- Serialization and de−serialization
- Clock and data recovery (CDR)
- 4B5B coding
- BMC coding
- Packet CRC generation and checking
- Coding and detection of Power Delivery K−Codes
- Automatic GoodCRC packet response

BC1.2 Support

The FUSB15101 has the circuitry to enable emulation BC1.2, QC2.0 and 2.4A Divider Mode via firmware.

VBUS Operation

Gate Driver

VBUS from the USB−C connector is typically connected to a load switch NFET (Q1 in Figure 6) source terminal whose gate terminal is driven by the FUSB15101 gate driver via the LGATE pin. **onsemi** recommends NFETs with low I_{GSS} leakages (<1 μA) for optimal gate drive.

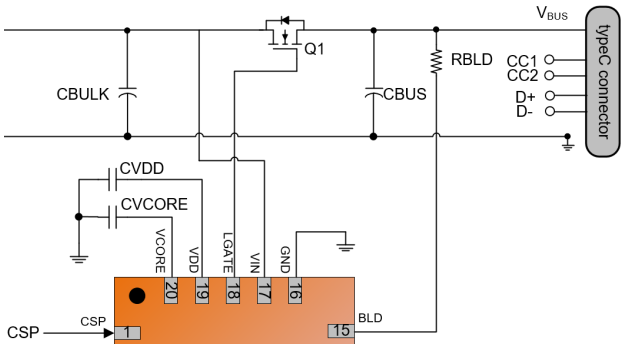


Figure 6. VBUS Discharge via BLD Pin

VBUS Discharge

VBUS is discharged through a resistor (RBLD) via the BLD pin of the FUSB15101 as shown in the highlighted section in Figure 6. The external resistor RBLD value is dependent on the total bulk capacitance (CBULK) of the power source so that VBUS is discharged within the time limits dictated by USB PD. A typical value for RBLD is 30 Ω, 1 W and in addition, there is internal resistance that limits the discharge current within the FUSB15101 ($I_{BLD−SINK}$ in the electrical tables above).

When the load current to the Sink is sufficient (exceeds $I_{CS−EN−BLD}$ for $t_{CS−EN−BLD}$ debounce time) such that the internal discharge is not needed, then the FUSB15101 will automatically disable internal discharge.

Upon power up, firmware in the FUSB15101 may discharge VBUS in case there is a voltage on VBUS since the only way a Sink can be attached per Type C specification is if VBUS is discharged to ground (below VSafe0V) upon attach.

The discharge resistance limits are governed by the Type C specification when not sourcing power on VBUS ($R_{BLD−LEAK}$ in the electrical tables above). It is preferred that no external load/discharge resistor is connected to VBUS other than RBLD to the FUSB15101 discharge BLD pin. A TVS diode connected from VBUS to ground ([SZ]ESD7241) allow operating voltages up to 24 V covering the entire VBUS range of 3.3 V to 21 V for a USB PD PPS contract. This can be replaced by a TVS that covers the VBUS range for the use case of this design if needed.

Voltage and Current Sensing Operation

The resistor ratio from VIN to ground formed by resistors R2 and R3 in Figure 7 (typically 1:10 ratio) is sensed via FUSB15101 VREF pin to set the output voltage.

For the offline design in Figure 2, this will be done via the FUSB15101 SFB pin, the opto−coupler, resistor R1 and the primary side PWM controller operation.

For DC−DC design in Figure 3, this will be done via the FUSB15101 SFB pin controlling the buck−boost PWM via its COMP pin.

The FUSB15101 will automatically control the SFB pin based on the desired voltage as determine by the USB PD contract and the existing VIN voltage sensed by VREF.

The external compensation network formed by C2/R2 and R4/C1 need to be selected to achieve stable operation over the range of VBUS voltage and current transitions as shown in Figure 7.

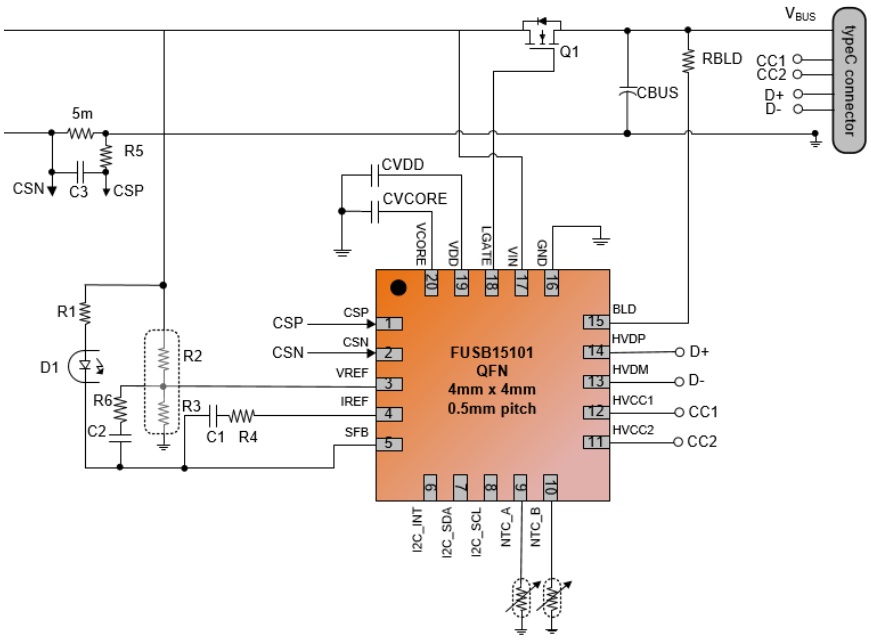


Figure 7. Compensation Network for AC/DC Constant Voltage / Constant Current (CC/CV) Feedback

For the DC−DC design in Figure 3, there may be a need for additional compensation networks from COMP pin to ground or from COMP to the DC−DC's supply.

The current is sensed via a small resistor (5 mΩ typically) connected between the USB−C connector ground and the main ground plane of the power source (secondary side ground for offline design) as shown in Figure 7. The gain of the current sense amplifier can be adjusted to work with 10 mΩ resistors if desired.

A low pass filter formed by R5/C3 provides a stable signal for CSP and CSN pins of the FUSB15101 to sense this current for over−current protection for fixed voltage PD contracts, constant current operation for PPS contracts and cable compensation (Table 1).

Table 1. CABLE DROP COMPENSATION

Symbol	Cable Drop Compensation
$V_{COMR-CDC-0}$	0 mV/A
$V_{COMR-CDC-0}$	50 mV/A
$V_{COMR-CDC-100}$	100 mV/A
$V_{COMR-CDC15-0}$	150 mV/A
$V_{COMR-CDC-200}$	200 mV/A
$V_{COMR-CDC-250}$	250 mV/A

It is expected that the USB−C connector ground is connected only to the current sense network resistors and the connector TVS ground connections and not to the main ground plane of the DC/DC design or secondary side power ground for the offline design (FUSB15101 ground connection). However, the FUSB15101 consumes very little current and so it should have a negligible impact on this current sensing if the FUSB15101 ground connection is on the USC−C connector ground if it is more convenient in the Printed Circuit Board (PCB) layout.

When in a PPS contract, if a PPS_Status message is requested, the firmware in the FUSB15101 will measure the current with an internal 10−bit Analog to Digital Converter (ADC) based on the above description and report it back to the Sink on the PPS_Status message. The voltage is also reported back but it is measured off VIN with the ADC not VREF pin since the VREF pin is only used for voltage feedback. Thus, if the voltage feedback resistor divider connected to VREF is modified to be slightly different from the 1:10 ratio expected, the voltage sensing for this PPS_Status message will not be affected. BLD pin voltage can also be monitored by the ADC and it will be accurate as long as the discharge function is not enabled.

Protection Operation

FUSB15101 has several ways it protects itself as shown in Table 2.

OVP and UVP are sensed via an internal resistor divider that divides VIN by 10 to determine the voltage from the power source. HVCC1, HVCC2, HVDP and HVDM are directly sensed for over voltage. For external temperature monitoring (E_OTP), two NTC pins are available that are connected to NTC resistors to ground usually in parallel with another resistor to ground for linearity. An internal temperature monitor (I_OTP) is also used for protecting the devince under extreme die temperatures. For all faults capable of automatic hardware protection (when enabled), the FUSB15101 will disable the Type C connection with the Sink (no pull−up on CC), shut off VBUS load switch and discharge VIN to vSafe5V.

Table 2. PROTECTION FEATURES

Symbol	Description	Pin(s) Used	Automatic Hardware Protection Capable?
OVP	Output Over Voltage Protection	VIN	Yes
UVP	Output Under Voltage Protection	VIN	Firmware Controlled
OCP	Over Current Protection	CSP & CSN	Yes
I_OTP	Internal Temperature Protection	N/A	Yes
E_OTP	External Temperature Protection	NTCA / NTCB	Firmware Controlled
CC_OVP	HVCC1 or HVCC2 Over Voltage Protection	HVCC1 / HVCC2	Yes
USB_OVP	HVDP or HVDM Over Voltage Protection	HVDP / HVDM	Yes
VCONN_OCP	VCONN Over Current Protection	CC1 / CC2	Yes
Cable Fault	VBUS or HVDM Pollution Detection	BLD / HVDM	Firmware Controlled

Output Over−Voltage Protection (OVP)

FUSB15101 has built−in OVP based on firmware programmable values. Whenever VIN, as sensed by an internal 1:10 resistor divider, exceeds by K_{IN-OVP} (Table 3) of the requested VIN from the power source for a debounce time of $t_{VIN-OVP-Debounce}$, then the OVP fault would be triggered. If hardware auto−protection is enabled, the FUSB15101 will disable the Type C connection with the Sink (no pull−up on CC), shut off VBUS load switch and discharge VIN to vSafe5V.

During transitions between VIN voltages, the OVP circuitry can be blanked or disabled via firmware to ensure that false triggering of OVP doesn't occur. To ensure safe operation over all voltages of VIN, the maximum VIN voltage is limited to VIN−OVP−MAX.

Table 3. PROGRAMMABLE OVP SETTINGS

Symbol	VIN / VIN Requested
$K_{IN-OVP-105}$	105%
$K_{IN-OVP-110}$	110%
$K_{IN-OVP-115}$	115%
$K_{IN-OVP-120}$	120%
$K_{IN-OVP-125}$	125%
$K_{IN-OVP-130}$	130%
$K_{IN-OVP-135}$	135%

Output Under−Voltage Protection (UVP)

FUSB15101 has a built−in firmware programmable UVP. Whenever VIN, as sensed internally, is below K_{IN-UVP} (Table 4) of the requested output voltage from the power source, then the UVP fault would be triggered. During transitions between VIN voltages, the UVP circuitry can be blanked or disabled via firmware to ensure that false triggering of UVP doesn't occur. For PPS contracts, if current limiting causes the voltage to decrease, the UVP fault will not trigger at a percentage of VIN since all voltages from the requested voltage to VIN−OFF, the lowest voltage, are valid.

For compliance with the USB PD specification, the FUSB15101 will trigger UVP whenever VIN is below VIN−OFF. This allows protection for a direct short of VBUS to ground separately or in conjunction with the OCP fault described below. If VIN < VIN−OFF fault is triggered, then to resume normal operation, VIN has to go below VLATCH−OFF to reset the FUSB15101 to exit this fault condition.

Table 4. PROGRAMMABLE UVP SETTINGS

Symbol	VIN / VIN Requested
$K_{IN-OVP-105}$	105%
$K_{IN-UVP-60}$	60%
$K_{IN-UVP-65}$	65%
$K_{IN-UVP-70}$	70%
$K_{IN-UVP-80}$	80%
$K_{IN-UVP-90}$	90%
$K_{IN-UVP-95}$	95%

Over−Current Protection (OCP) and Constant Current Limit (CL)

If VBUS is shorted to ground, either the UVP fault described above could trigger or the OCP fault, or both. FUSB15101 senses the current via a small sense resistor (5 mΩ typical) as described in the Voltage and Current Sensing section above. The OCP fault is triggered at firmware programmed ratio of the maximum current for the requested Power Data Object (PDO). Once this OCP fault occurs, the FUSB15101 protects the system as described in the Protection Operation section above. For PPS APDO's (Augmented Power Data Objects), Constant Current Limiting (CL) is used as specified in the USB PD specification where the voltage will drop to a low value based on keeping the current constant and equal to the requested PPS current. In this case UVP described above will trigger if VIN drops below VIN−OFF since any voltage from the lowest 3.3 V − 5% to the PPS requested voltage could occur with current limiting. If the PPS current limit is

changed with a new PD Request message, the VIN voltage may change accordingly to a new value based on the current limiting function.

Over−Temperature Protection (Internal and External)

FUSB15101 has two different over temperature faults, External and Internal. For External OTP, there are two NTC pins that may be connected to NTC resistors in parallel with a regular resistor for linearity. The FUSB15101 provides separate INTC current sources (typically 60 μA) on the NTC pins to bias these NTC resistors so that an internal A/D converter measures the external temperature as shown in Figure 8. The firmware can be customized to trigger a fault on the desired application specific temperature limits. If the second NTC pin is not used for measuring temperature, it can be used as a general−purpose ADC channel.

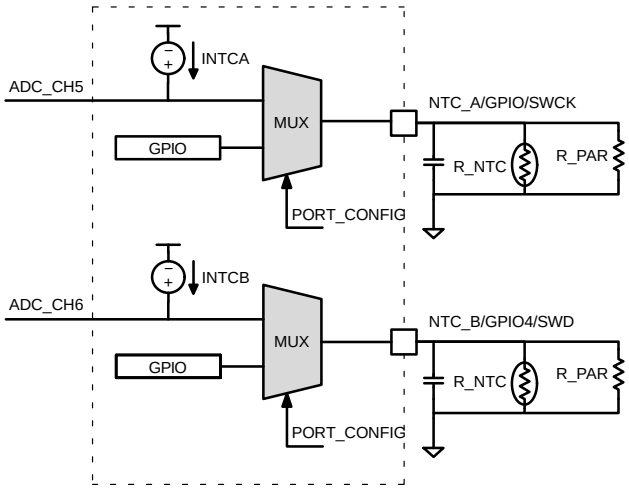


Figure 8. External Temperature Monitoring

This NTC measured temperature is useful for dynamic monitoring by the Sink via FUSB15101 provided PD Status messages.

Internal OTP monitors the internal die temperature. When the die temperature exceeds Tshut threshold for tOTP−Debounce time, an interrupt is set to alert the core and take action.

Cable Fault

The FUSB15101 allows for foreign substance monitoring of the Type−C receptacle via the HVDM pin.

Pollution detection on HVDM is done by applying a small voltage and resistance to the DM pin and measuring its voltage potential via the on−board ADC.

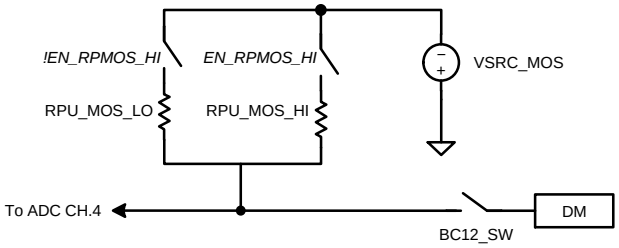


Figure 9. HVDM Pollution Detection

There are two pull up resistors that are selectable:

1. EN_RPMOS_HI = 1 (RPU_MOS_HI = 300 kΩ) Moisture or pollutants on the Type−C connector have been characterized as resistance to ground smaller than ~300 kΩ when nothing is attached.
2. EN_RPMOS_HI = 0 (RPU_MOS_LO = 2.5 kΩ) Certain applications prefer to detect pollution resistance in the 200 Ω to ~400 Ω range. For that a second pull−up resistor is included.

I^2C

The FUSB15101's serial interface is compatible with Standard, Fast, and Fast Mode Plus I^2C bus specifications. The I^2C peripheral can be configured for either host or device modes. The analog circuitry is firmware configurable for the function required by the application and follows the final BC1.2 specification.

Bus Timing

As shown in Figure 10 below[6], for data bits, SDA must be stable while SCL is HIGH. SDA may only transition when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

6. Bus timing referenced from I^2C−bus specification Rev. 6−4 April 2014

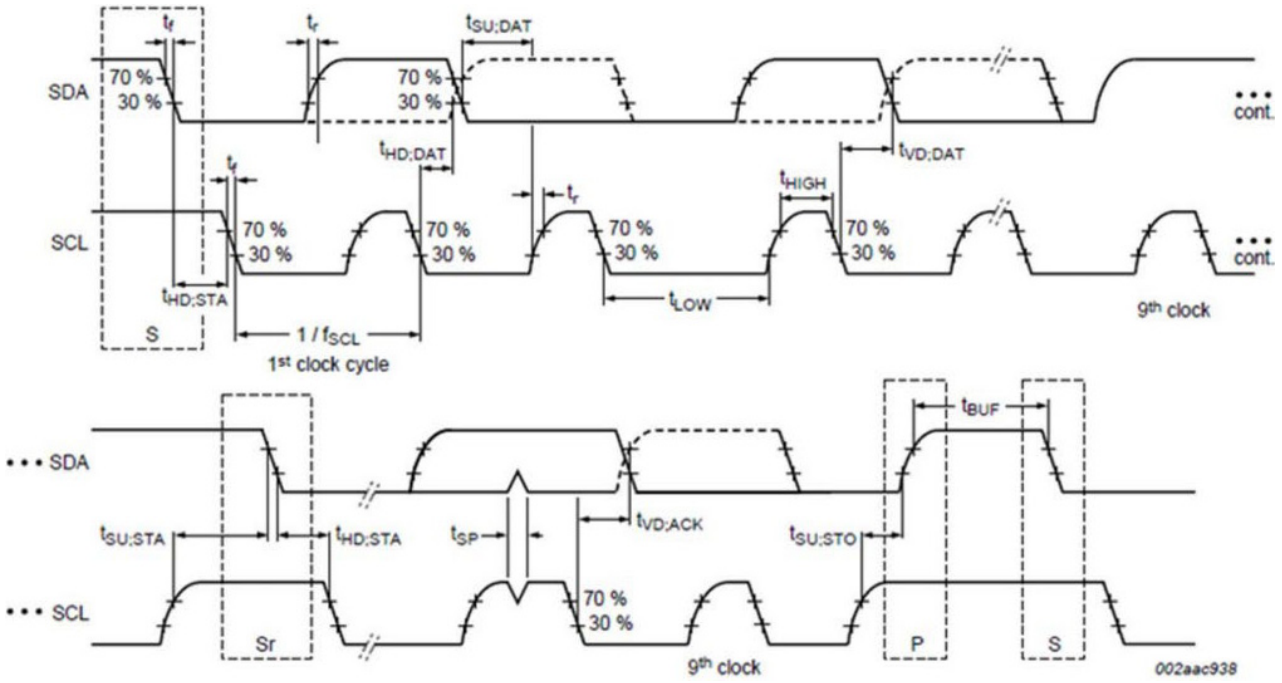


Figure 10. I²C Bus Timing Definition

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH. A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH. During a read from the FUSB15101, the host issues a Repeated Start after sending a data command and before resending the device address. The Repeated Start is a 1−to−0 transition on SDA while SCL is HIGH.

UART

The FUSB15101 implements a UART transceiver that communicates via D+/− when enabled.

When this peripheral is disabled, it should not interfere with D+/− charging protocols such as BC1.2− where the ADC is sensitive to loads.

Clock Requirements and BAUD Rates

The max BAUD rate support is dependent on the CLK_HS speed setting. BAUD rates are supported from 9,600 to 230,400.

Automatic BAUD Rate Detection

The FUSB15101 implements automatic BAUD Rate detection based on the first character received in a message.

The supported characters for automatic BAUD rate detection are 0xAA or 0x55.

Automatic BAUD detection rate works up to 230,400 bps. BAUD Rates detected outside of this range will be flagged as errors to the core.

Port Control and GPIOs

The FUSB15101 includes a number of pins that can be configured to be used as standard GPIO or for use with a dedicated peripheral such as I²C. A subset of these Pins can also be connected as an input to the ADC. Internal pull−up/down resistors are programmable. Pull−up resistors are always connected to VDD.

When the PORT is configured as GPIOs it will have the following capabilities:

- Bi−directional capability
- Push pull or open drain configuration
- Individually configurable interrupt lines
- Rising or Falling edge interrupt
- High− or Low−level interrupt

Table 5. PIN−PORT CONFIGURATION

Pin #	Name	Port
6	GPIO0	PA0
	I2C_INT	
7	GPIO1	PA1
	I2C_SDA	
8	GPIO2	PA2
	I2C_SCL	
9	GPIO3	PA3
	ADC_CH5	
	SWCK	
10	GPIO4	PA4
	ADC_CH6	
	SWD	

ADC

The FUSB15101 allows for up to 7 signals to be measured and converted using the internal 10−bit ADC. For most applications, this will consist of VBUS and VIN voltages, Output Current, two NTC temperature channels and two D+/D− BC1.2 ports. Table 6 below shows the typical FUSB15101 configuration along with the expected settings for the ADC module.

Table 6. ADC CONFIGURATION

ADC Channel	Pin Measurement	Resolution	Range	Full Scale Voltage
0	VIN	10 mV	0 V to 10.23 V	1.024 V
		20 mV	0 V to 20.46 V	2.048 V
		40 mV	0 V to 40.92 V	4.096 V
1	BLD	10 mV	0 V to 10.23 V	1.024 V
		20 mV	0 V to 20.46 V	2.048 V
		40 mV	0 V to 40.92 V	4.096 V
2	Output Current	10 mA	0 A to 10.23 A	2.048 V
3	HVDP	4 mV	0 V to 4.096 V	4.096 V
4	HVDM	4 mV	0 V to 4.096 V	4.096 V
5	NTCA Temperature	1°C	0°C to 160°C	1.28 V
6	NTCB Temperature	1°C	0°C to 160°C	1.28 V

Development Tools

FUSB15101 is supported by a full suite of comprehensive tools including:

- An easy−to−use development board
- Software Development Kit (SDK) including: USB PD protocol stacks, sample code, libraries, and documentation

Specifications References

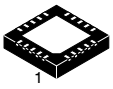
- Universal Serial Bus Power Delivery specification revision 3.1 Version 1.0, dated May 2021
- Universal Serial Bus Type C Cable and Connection Specification release 2.1, dated May, 2021
- USB Battery Charging Specification, revision 1.2, dated December 7, 2010
- I^2C−bus specification Rev. 6 − 4 April 2014

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

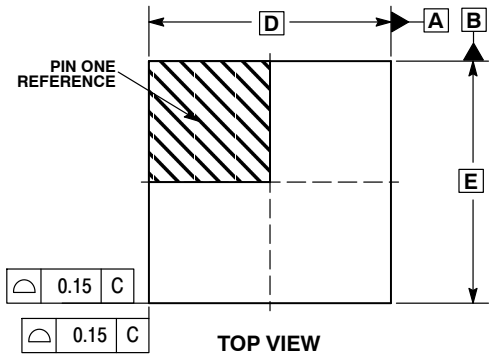
ON Semiconductor®

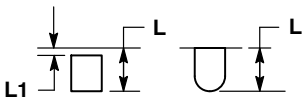
QFN20 4x4, 0.5P
CASE 485BH−01
ISSUE O

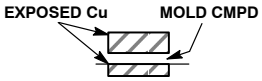
DATE 19 FEB 2010

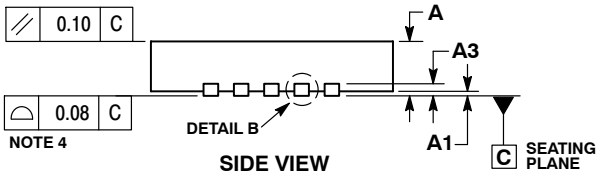


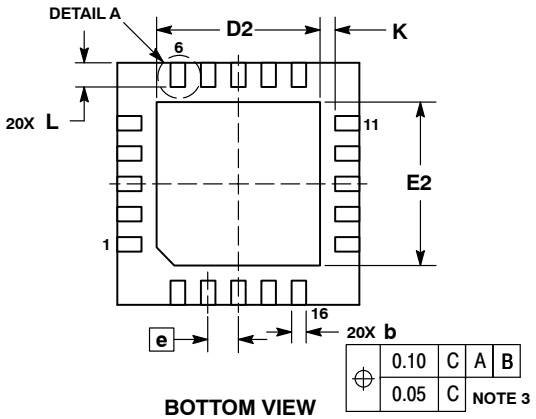
SCALE 2:1











NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.80
E	4.00 BSC	
E2	2.60	2.80
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	0.00	0.15

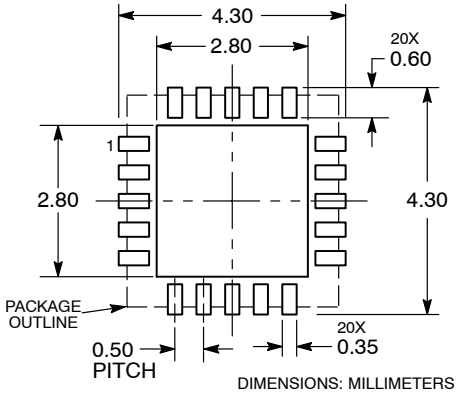
GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

MOUNTING FOOTPRINT



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