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USB Type-C Analog Audio Switch with Over Voltage Protection

FSA4485

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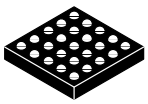


WLCSP25
CASE 567YL

PRODUCT SUMMARY

General Description

The FSA4485 is a high performance USB Type−C port multimedia switch to supports analog audio headsets. The FSA4485 allows sharing of the USB Type−C port to pass USB2.0 signals, analog audio, sideband use signals, and analog microphone signal. For enhanced audio performance the FSA4485 incorporates MOSFET gate drivers to support low resistance external analog ground switches. The FSA4485 features Over Voltage Protection on all connector facing pins as well as Over Current Protection for the analog ground switch.

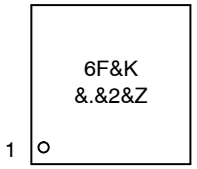
Features

- VCC Range from 2.7 V to 5.5 V (Primary)
- OVP Function on Common Node Pins
- Over Current Protection for Analog Ground Switch
- Analog Audio Device Unplug Detection
- 16 V DC Tolerance on Connector Side Pins: DP_R, DN_L, GBSUx, SBUx
- 20 V DC Tolerance on CC_IN
- High Performance Audio/USB SW:
  - Audio SW, THD+N < −109 dB; 1 VRMS, 32 Ω Load;
  - USB SW, BW: 1 GHz
- 225 mΩ (Typical) Sense to GSBUx on Resistance
- 78 mΩ (Typical) SBUx to AGND on Resistance
- Programmable Gate Drive for Optional External SBUx to AGND Switch
- 1.2 V Capable I^2C Interface
- Two I^2C Addresses
- Optional Normally Closed Configuration for SBU Data Switch to Support Factory Test
- Moisture/Resistance Detection on DP_R, DN_L and SBUx

Applications

- Mobile Phone
- Tablet
- Notebook PC
- Media Player

MARKING DIAGRAM



6F	= Alphanumeric Device Marking
&K	= Lot Run Code
&2	= Alphabetical Year Code
&Z	= Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

PRODUCT BLOCK DIAGRAM

Block Diagram

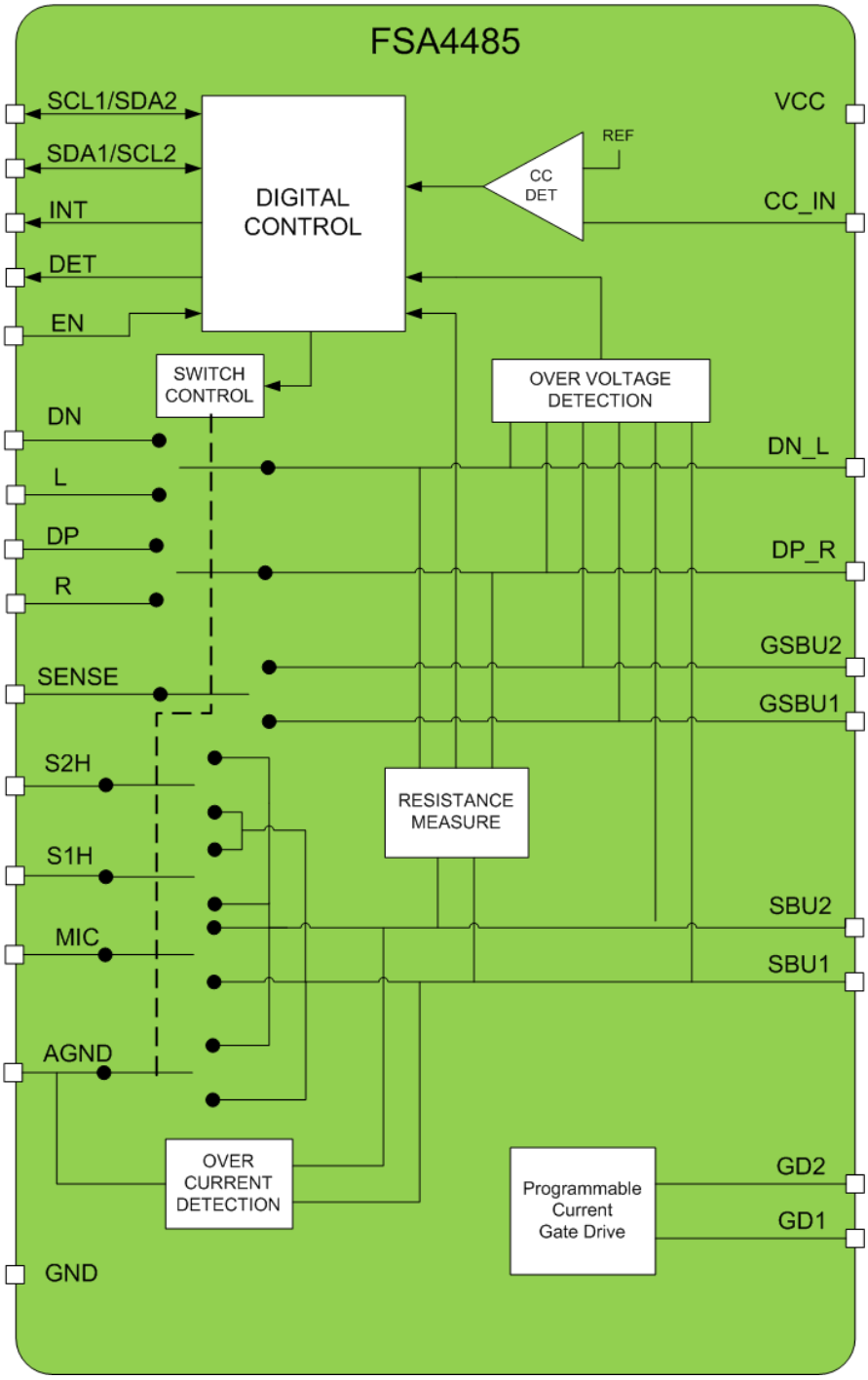


Figure 1. Block Diagram

PART NUMBERING

Ordering Information

Table 1. ORDERING INFORMATION

Part Number	Operating Temperature	Package	Top Marking
FSA4485UCX	−40 to +85°C	25−Ball WLCSP, Non−JEDEC 2.16 × 2.16 mm, 0.4 mm Pitch (Pb−Free)	6F

PRODUCT PIN ASSIGNMENTS

Pin Configuration

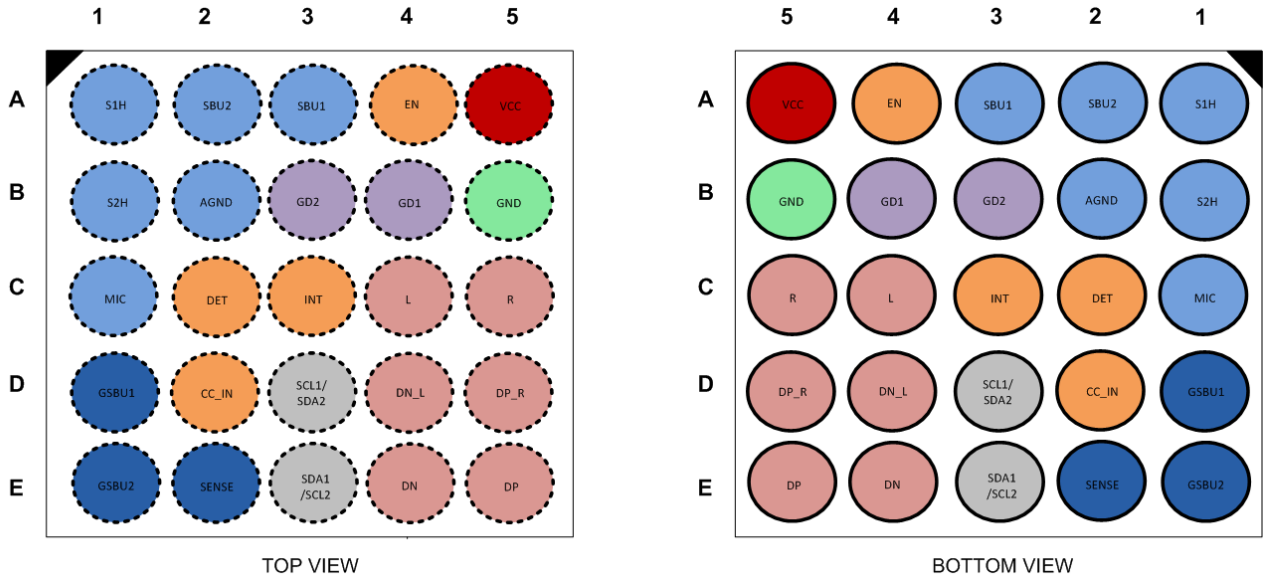


Figure 2. Pin Configuration

Pin Descriptions

PIN DESCRIPTIONS

Pin	Name	Description
A5	VCC	Power Supply (2.7 to 5.5 V)
B5	GND	Device Ground
D5	DN_R	USB/Audio Common Connector
D4	DN_L	USB/Audio Common Connector
E5	DP	USB Data (Differential +)
E4	DN	USB Data (Differential −)
C5	R	Audio − Right Channel
C4	L	Audio − Left Channel
A3	SBU1	Sideband Use 1
A2	SBU2	Sideband Use 2
C1	MIC	Microphone Signal
B2	AGND	Audio Ground
B4	GD1	External Gate Driver
B3	GD2	External Gate Driver
E2	SENSE	Audio Ground Sense Output
C3	INT	I^2C Interrupt Output, Active Low (Open Drain)
D2	CC_IN	Audio Accessory Attach Detection Input
D1	GSBU1	Audio Sense Path 1 to Headset Jack GND
E1	GSBU2	Audio Sense Path 2 to Headset Jack GND
C2	DET	Attach Detect Output, Active Low (Open Drain)
D3	SCL1/SDA2	I^2C Clock/Data
E3	SDA1/SCL2	I^2C Data/Clock
B1	S2H	Host Side Sideband use
A1	S1H	Host Side Sideband use
A4	EN	Device Enable and Precondition, 3−state Input with internal pull−up/pull−down

MAXIMUM RATINGS

MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC	Supply Voltage		−0.5	–	6.5	V
VCC_IN	CC Voltage	CC_IN to GND	−0.5	–	20	V
VSW_USB	USB Switch Voltage	(DP_R, DN_L) to GND	−3.5	–	16	V
VSW_SBU	SBU Switch Voltage	(SBUx, GSBUx) to GND	−0.5	–	16	V
VSW_HOST	Host Side Switch Voltage	(DP, DN, S1H, S2H, SENSE, MIC) to GND	−0.5	–	6.5	V
VSW_Audio	Host Side Audio Switch Voltage	(L, R) to GND	−3.5	–	6.5	V
VCNTRL	Control Pin Voltage	(SDA, SCL, EN, DET, INT) to GND	−0.5	–	6.5	V
IIK	DC Input Diode Current		−50	–	–	mA
ISW_USB	USB Switch Current	Between DP_R and DP or DN_L and DN		–	100	mA
ISW_SBU	SBU Switch Current	(S1H, S2H, MIC) to SBUx		–	50	mA
ISW_SENSE	Sense Switch Current	GSBUx to SENSE		–	100	mA
ISW_AGND	Analog Ground Current	SBUx to AGND		–	500	mA
ISW_Audio	Audio Switch Current	DP_R to R or DN_L to L	−250	–	250	mA
ESDHBM	Human Body Model, JEDEC: JS−001−2017	All Pins	2	–	–	kV
ESDHBM_Con		Connector Side Pins and Power Pins	3.5	–	–	kV
ESDCDM	Charged Device Model, JEDEC: JS−002−2018		1	–		kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL PROPERTIES

THERMAL PROPERTIES

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{STG}	Storage Temperature		−65		150	°C
T_A	Operating Temperature		−40	25	85	°C

1. Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with two−layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.

OPERATING CONDITIONS

OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC	Supply Voltage		2.7	–	5.5	V
VCC_IN	CC Voltage	CC_IN to GND	0	–	5.5	V
VSW_USB	USB Switch Voltage	(DP_R, DN_L, DP, DN) to GND	0	–	3.6	V
VSW_SBU	SBU Switch Voltage	(SBUx, GSBUx) to GND	0	–	3.6	V
VSW_HOST	Host Side Switch Voltage	(DP, DN, S1H, S2H, SENSE, MIC) to GND	0	–	3.6	V
VSW_Audio	Host Side Audio Switch Voltage	(DN_L, DP_R, L, R) to GND	−3	–	3	V
VCNTRL	Control Input Voltage (EN, SCL1/SDA2, SDA1/SCL2)				VCC	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL SPECIFICATION TABLE

ELECTRICAL SPECIFICATIONS

(Minimum and maximum values are at VCC = 2.7 V to 5.5 V and T_A = −40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C, VCC = 3.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CURRENT						
ICC	Supply Current	USB switches on, SBUx to SBUx_H switches on			65	μA
ICC_AUDIO	Audio Supply Current	Audio switches closed, MIC switch closed and Audio GND switch closed			65	μA
ICCZ	Quiescent Current, Software Disabled	04H'b7 = 0, EN = Low or Float			5	μA
ICCZ_H	Quiescent Current, Hardware Disable	EN = High			10	μA
USB/AUDIO COMMON PINS						
IOZ	USB Connector Side Off Leakage Current	DP_R, DN_L = 0 V to 3.6 V	−3		3	μA
IOFF	USB Connector Side Power Off Leakage Current	DP_R, DN_L = 0 V to 3.6 V, VCC = 0 V	−3		3	μA
VOV_TRIP	Input OVP Lockout	Rising Edge of DP_R, DN_L, SBUx, GSBUx	4.7	5	5.2	V
VOV_HYS	Input OVP Hysteresis	DP_R, DN_L, SBUx, GSBUx	–	0.3	–	V
USB SWITCH						
ION_USB	USB Switch ON Leakage Current	DN_L, DP_R = 0 V to 3.6 V, DP, DN, R, L = Float	−3		3	μA
IOZ_USB	USB Host Side Off Leakage Current	DN, DP = 0 V to 3.6 V	−3		3	μA
IOFF_USB	USB Host Side Power Off Leakage Current	DN, DP = 0 V to 3.6 V, VCC = 0 V	−3		3	μA
RON_USB	USB Switch On Resistance	ISW = 8 mA, VSW = 0.4 V		3		Ω
AUDIO SWITCH						
ION_AUDIO	ON Leakage Current of Audio Switch	DN_L, DP_R = −3 V to 3.0 V, DP, DN, R, L = Float	−6		6	μA
IOFF_AUDIO	Power Off Leakage Current of Audio Switch L, R	L, R = 0 V to 3 V; DP_R, DN_L = Float, VCC = 0 V	−1		1	μA
RON_AUDIO	Audio Switch On Resistance	ISW = 100 mA, VSW = −3 V to 3 V		1		Ω
RON_FLAT	Audio Switch On Resistance Flatness †	VSW = −3.0 V to +3.0 V		10		mΩ
RSHUNT	Pull Down Resistor on R/L Pin when Audio Switch is Off	L = R = 3 V	6	10	14	kΩ
SBU COMMON PINS						
IOZ_SBU	Off Leakage Current (SBU1, SBU2)	SBUx = 0 V to 3.6 V	−3		3	μA
IOFF_SBU	Power Off Leakage Current (SBU1, SBU2)	SBUx = 0 V to 3.6 V, VCC = 0 V	−3		3	μA
SBU DATA SWITCH						
ION_SxH	ON Leakage Current of SBU Switch	SBUx = 0 V to 3.6 V, SxH = Float	−3		3	μA
IOZ_SxH	Off Leakage Current (S1H, S2H)	SxH =0 V to 3.6 V	−1		1	μA
IOFF_SxH	Power Off Leakage Current (S1H, S2H)	SxH =0 V to 3.6 V, VCC = 0 V	−1		1	μA
RON_SxH	SBU Switch On Resistance to (S1H, S2H)	VSW = 0 V to 3.6 V, ISW = 20 mA		3		Ω
MIC SWITCH						
ION_MIC	ON Leakage Current of MIC Switch	SBUx = 0 V to 3.6 V, MIC = Float	−3		3	μA
IOZ_MIC	Off Leakage Current (MIC)	MIC = 0 V to 3.6 V	−1		1	μA

ELECTRICAL SPECIFICATIONS (continued)
(Minimum and maximum values are at VCC = 2.7 V to 5.5 V and T_A = −40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C, VCC = 3.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MIC SWITCH						
IOFF_MIC	Power Off Leakage Current (MIC)	MIC = 0 V to 3.6 V, VCC = 0 V	−1		1	μA
RON_MIC	SBU Switch On Resistance to (MIC)	VSW = 0 V to 3.6 V, ISW = 20 mA		3		Ω
AGND SWITCH						
RON_AGND	SBUx Switch On Resistance to AGND	ISW = 100 mA on SBUx		78	125	mΩ
IOC_TRIP	Input OCP Lockout SBUx to AGND	04h'b0 = 1, 07h = xx010xxxb or xxxxx010b	0.75	1.5	3.0	A
SENSE SWITCH						
ION_SENSE	ON Leakage Current of SENSE switch	On GSBUx = 0 V to 1.0 V, Off GSBUx = 2 V, Sense = Float	−2		2	μA
IOZ_SENSE	Off Leakage Current of SENSE	Sense = 0 V to 1.0 V	−3		3	μA
IOZ_GSBU	Off Leakage Current of GSBUx	GSBUx = 0 V to 3.6 V	−3		3	μA
IOFF_SENSE	Power Off Leakage Current of SENSE	Sense = 0 V to 1.0 V, VCC = 0 V	−3		3	μA
IOFF_GSBU	Power Off Leakage Current of GSBUx	GSBUx = 0 V to 3.6 V, VCC = 0 V	−3		3	μA
RON_SENSE	Sense Switch On Resistance	IOUT = 100 mA, VSW =1 V		250	400	mΩ
CC_IN PIN						
VTH_L_CC	Input Low Threshold			1.2		V
VTH_H_CC	Input High Threshold			1.5		V
IIN_CC	CC_IN Input Leakage Current	CC_IN = 0 V to 5.5 V			1	μA
EN PIN						
VIH_EN	EN Input Voltage High		1.1			V
VIL_EN	EN Input Voltage Low				0.5	V
RFLOAT_EN	Resistance from EN to GND			900		KΩ
IIN_EN	EN Input Leakage Current	EN = 0 V to 5.5 V			10	μA
DET & INT PIN						
VOL	Output Low Voltage	IOUT = 2 mA			0.4	V
I²C PINS						
VIL_I2C	Low Level Input Voltage				0.36	V
VIH_I2C	High Level Input Voltage		0.84			V
IIN_I2C	Input Current	SCL1/SDA2, SDA1/SCL2 = 0 V to 3.6 V	−2		2	μA
VOL_I2C	Low Level Output Voltage	IOL = 2 mA			0.3	V
VOH_I2C	Low Level Output Current	VOL_I2C = 0.2 V	10			mA
GATE DRIVE						
I_GATE	Gate Drive Current (GD1, GD2) †	V_GATE = 3 V		2		μA
V_GATE	Gate Drive Voltage (GD1, GD2) †	ILoad = 200 nA		6		V
R_GATE	Gate Drive Discharge Resistance †			1.0		MΩ
AUDIO SWITCH						
tDELAY_Audio	Audio Switch Turn On Delay Time †	DP_R = DN_L = 1 V, RL = 32 Ω, SLOW_TURN_ON = 0b		100		μs
tDELAY_Audio_Slow	Audio Switch Turn On Delay with Slow Turn On †	DP_R = DN_L = 1 V, RL = 32 Ω, SLOW_TURN_ON = 1b		150		μs

ELECTRICAL SPECIFICATIONS (continued)
(Minimum and maximum values are at VCC = 2.7 V to 5.5 V and T_A = −40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C, VCC = 3.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AUDIO SWITCH						
tRISE_Audio	Audio Switch Turn On Rise Time †	DP_R = DN_L = 1 V, RL = 32 Ω, SLOW_TURN_ON = 0b		26		μs
tRISE_Audio_Slow	Audio Switch Turn On Rise Time with Slow Turn On †	DP_R = DN_L = 1 V, RL = 32 Ω, SLOW_TURN_ON = 1b		180		μs
tOFF_Audio	Audio Switch Turn Off Time †	DP_R = DN_L = 1 V, RL = 32 Ω		15		μs
XTALK_Audio	Crosstalk between Left and Right †	f = 1 kHz, RL = 50 Ω to GND, VSW = 1 VRMS		−100		dB
BW_Audio	−3dB Bandwidth †	VSW = 200 mV, RL = 50 Ω		550		MHz
OIRR_Audio	Off Isolation †	F = 1 kHz, RL = 50 Ω, CL = 0 pF, VSW = 1 VRMS		−100		dB
THD+N_600	Total Harmonic Distortion + Noise Performance with A−weighting Filter †	RL = 600 Ω, f = 20 Hz~20 kHz, VSW = 2 VRMS		−100		dB
THD+N_32	Total Harmonic Distortion + Noise Performance with A−weighting Filter †	RL = 32 Ω, f = 20 Hz~20 kHz, VSW = 1 VRMS		−109		dB
THD+N_16	Total Harmonic Distortion + Noise Performance with A−weighting Filter †	RL = 16 Ω, f = 20 Hz~20 kHz, VSW = 0.5 VRMS		−108		dB
PSRR_Audio	Power Supply Rejection Ratio to Audio †	Supply Noise = 300mVpp, f = 217 Hz, RL = 50 Ω, Audio Switch Closed		−70		dB
USB SWITCH						
tON_USB	USB Switch Turn−on Time †	DP_R = DN_L = 1.5 V, RL = 50 Ω		33		μs
tOFF_USB	USB Switch Turn −off Time †	DP_R = DN_L = 1.5 V, RL = 50 Ω		15		μs
BW_USB	−3 dB Differential Bandwidth †	RL = 50 Ω		1		GHz
IL_USB	Insetrion Loss †	RL = 50 Ω, f = 720 MHz		−2.2		dB
OIRR_USB	Off Isolation between DP, DN and Common Node Pins †	f = 1 kHz, RL = 50 Ω, CL = 0 pF, VSW = 1 VRMS		-100		dB
tOVP_USB	DP_R and DN_L pins OVP Response Time †	Rising edge of DP_R or DN_L ≥ 4.8 V to falling edge of DP or DN or L or R ≤ 4.8 V, RL on DP or DN = 1 kΩ		600		ns
MIC/AUDIO GROUND SWITCH						
tDELAY_MIC	MIC Switch Turn On Delay Time with Slow Turn On Disabled †	SBUx = 1 V, RL = 50 Ω, SLOW_TURN_ON = 0b		90		μs
tDELAY_MIC_Slow	MIC Switch Turn On Delay with Slow Turn On Enabled †	SBUx = 1 V, RL = 50 Ω, SLOW_TURN_ON = 1b		200		μs
tRISE_MIC	MIC Switch Turn On Rising Time with Slow Turn On Disabled †	SBUx = 1 V, RL = 50 Ω, SLOW_TURN_ON = 0b		40		μs
tRISE_MIC_Slow	MIC Switch Turn On Rising Time with Slow Turn On Enabled †	SBUx = 1 V, RL = 50 Ω, SLOW_TURN_ON = 1b		300		μs
tDELAY_AGND	AGND Switch Turn On Time with Slow Turn On Disabled †	SBUx pulled up to 0.5 V by 16 Ω, AGND connect to GND, SLOW_TURN_ON = 0b		660		μs
tDELAY_AGND_Slow	AGND Switch Turn On Time with Slow Turn On Enabled †	SBUx pulled up to 0.5 V by 16 Ω, AGND connect to GND, SLOW_TURN_ON = 1b		1100		μs
tRISE_AGND	AGND Switch Turn On Rise Time with Slow Turn On Disabled †	SBUx pulled up to 0.5 V by 16 Ω, AGND connect to GND, SLOW−TURN_ON = 0b		270		μs

ELECTRICAL SPECIFICATIONS (continued)
(Minimum and maximum values are at VCC = 2.7 V to 5.5 V and T_A = −40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C, VCC = 3.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MIC/AUDIO GROUND SWITCH						
tRISE_AGND_Slow	AGND Switch Turn On Rise Time with Slow Turn On Enabled †	SBUx pulled up to 0.5 V by 16 Ω, AGND connect to GND, SLOW−TURN_ON = 1b		720		μs
tOFF_MIC	MIC Switch Turn Off Time †	SBUx = 2.5 V, RL = 50 Ω		15		μs
tOFF_AGND	AGND Switch Turn Off Time †	SBUx: Vsource = 2.5 V, clamp to 10 mA		15		μs
BW	MIC Switch Bandwidth †	RL = 50 Ω		35		MHz
tOC_DEB	SBUx to AGND Over Current Debounce Time †			500		μs
SBU SWITCH						
tON_SBU	SBUx_H Switch Turn On Time †	SBUx = 2.5 V, RL = 50 Ω		75		μs
tOFF_SBU	SBUx_H Switch Turn Off Time †	SBUx = 2.5 V, RL = 50 Ω		15		μs
BW_SBU	Bandwidth †	RL = 50 Ω		35		MHz
tOVP_SBU	SBUx Pins OVP Response Time †	Rising edge of SBUx ≥ 4.8 V to falling edge of SxH ≤ 4.8 V, RL on SxH = 1 kΩ		250		ns
SENSE SWITCH						
tDELAY_SENSE	Sense Switch Turn On Delay with Slow Turn On Disabled †	GSBUx = 1 V, RL = 50 Ω, SLOW_TURN_ON = 0b		150		μs
tDELAY_SENSE_Slow	Sense Switch Turn On Delay with Slow Turn On Enabled †	GSBUx = 1 V, RL = 50 Ω, SLOW_TURN_ON = 1b		110		μs
tRISE_SENSE	Sense Switch Turn On Rise Time with Slow Turn On Disabled †	GSBUx = 1 V, RL = 50 Ω, SLOW_TURN_ON = 0b		110		μs
tRISE_SENSE_Slow	Sense Switch Turn On Rise Time with Slow Turn On Enabled †	GSBUx = 1 V, RL = 50 Ω, SLOW_TURN_ON = 1b		110		μs
tOFF_SENSE	Sense Switch Turn Off Time †	GSBUx = 1 V, RL = 50 Ω		15		μs
tOVP_SENSE	GSBUx Pins OVP Response Time †	Rising edge of GSBUx ≥ 4.8 V to falling edge of SENSE ≤ 4.8 V, RL on SENSE = 1 kΩ		250		ns
BW_SENSE	Bandwidth †	RL = 50 Ω		108		MHz
DET DELAY						
tDELAY_DET	DET Response Delay †	Transition from High−Z to 0 V		2.5		μs
I²C SPECIFICATIONS						
fSCL	I2C_SCL Clock Frequency				400	kHz
tHD; STA	Hold Time (Repeated) START Condition †		0.6			μs
tLOW	Low Period of I2C_SCL Clock †		1.3			μs
tHIGH	High Period of I2C_SCL Clock †		0.6			μs
tSU; STA	Set−up Time for Repeated START Condition †		0.6			μs
tHD; DAT	Data Hold Time †		0		0.9	μs
tSU; DAT	Data Set−up Time †		100			ns
tr	Rise Time of I2C_SDA and I2C_SCL Signals †		20 + 0.1Cb		300	ns
tf	Fall Time of I2C_SDA and I2C_SCL Signals †		20 + 0.1Cb		300	sn
tSU; STO	Set−up Time for STOP Condition †		0.6			μs

ELECTRICAL SPECIFICATIONS (continued)
(Minimum and maximum values are at VCC = 2.7 V to 5.5 V and T_A = −40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C, VCC = 3.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C SPECIFICATIONS						
tBUF	Bus−Free Time between STOP and START Conditions †		1.3			μs
tSP	Pulse Width of Spikes that Must Be Suppressed by the Input Filter †		0		50	ns
CAPACITANCE						
CON_USB	On Capacitance of USB Common Pins †	f = 1 MHz, 100 mVPK−PK, 100 mV DC		8.5		pF
COFF_ USB	Off Capacitance of USB Common Pins †	f = 1 MHz, 100 mVPK−PK, 100 mV DC		9.5		pF
COFF_USBHost	Off Capacitance of USB Host Pins †	f = 1 MHz, 100 mVPK−PK, 100 mV DC		3.0		pF
CON_SENSE	On Capacitance of GSBUx †	f = 1 MHz, 100 mVPK−PK, 100 mV DC		34		pF
COFF_SENSE	Off Capacitance of GSBUx †	f = 1 MHz, 100 mVPK−PK, 100 mV DC		44		pF
CON_MIC	On Capacitance of SBUx to MIC Switch †	f = 1 MHz, 100 mVPK−PK, 100 mV DC		115		pF
COFF_MIC	Off Capacitance of MIC †	f = 1 MHz, 100 mVPK−PK, 100 mV DC		8.5		pF
CON_AGND	On Capacitance of SBUx to AGND Switch †	f = 1 MHz, 100 mVPK−PK, 100 mV DC		94.5		pF
CON_SBU	On Capacitance of SBUx to SxH Switch †	f = 1 MHz, 100 mVPK−PK, 100 mV DC		114		pF
COFF_SBU	Off Capacitance of SBUx †	f = 1 MHz, 100 mVPK−PK, 100 mV DC		108		pF
COFF_SBUHost	On Capacitance of SBUx to SxH Switch †	f = 1 MHz, 100 mVPK−PK, 100 mV DC		9.0		pF
CCNTRL	Control Input Pin Capacitance †	f = 1 MHz, 100 mVPK−PK, 100 mV DC		5.0		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
Guarantee Levels:
†Guaranteed by Design. Characterized on the ATE or Bench.

FUNCTIONAL SPECIFICATIONS

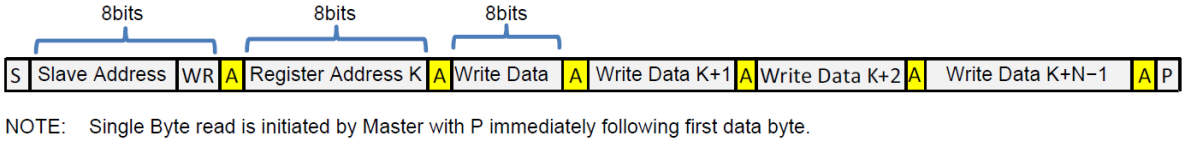
I²C Interface

The FSA4485 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 2.1 requirements. This block is designed for fast mode, 400 kHz, signals. Examples of an I²C write and read sequence are shown in below figures respectively.

The I²C Address can be selected by routing the SDA/SCL signals per the Table 2 below. The FSA4485 will detect the clock and automatically configure the I/O and address. The I²C interface will operate with VDDIO pull up from 1.2 V to 1.8 V.

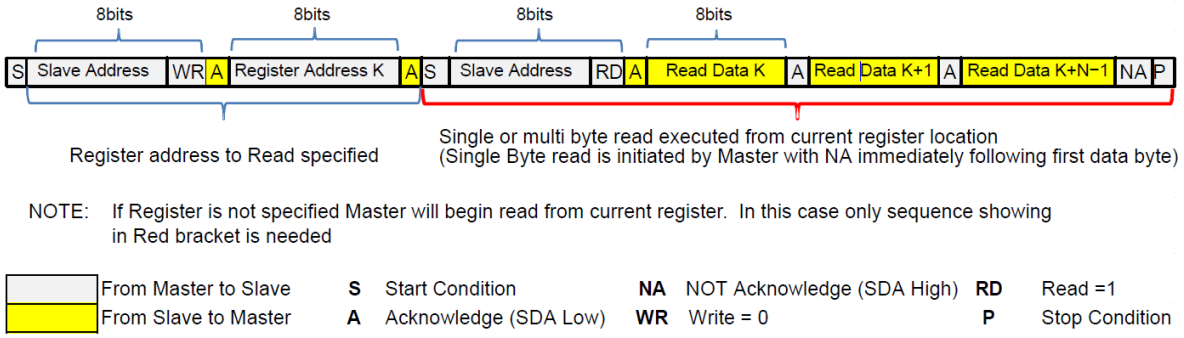
Table 2. I²C SLAVE ADDRESS

SDA	SCL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDA1	SCL1	1	0	0	0	0	1	0	R/W
SDA2	SCL2	1	0	0	0	0	1	1	R/W



NOTE: Single Byte read is initiated by Master with P immediately following first data byte.

Figure 3. I²C Write Example



NOTE: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed

Figure 4. I²C Read Example

Over Voltage Protection

FSA4485 features over voltage protection (OVP) on the receptacle side pins. This will automatically switch open the internal signal routing path if the input voltage exceeds the OVP threshold. If OVP has occurred an interrupt signal will be send using the INT signal. The OVP_INTERRUPT register will indicate which pin had the OVP event. If the over voltage is no longer present, indicated by the OVP_STAT register, the signal path can be restored manually from the SWITCH_SEL register.

Over Current Protection

When the EN_OCP register is set to Enable and the SBUx switch is closed to AGND Over Current Protection (OCP) will be enabled. OCP monitors the voltage drop from SBUx to AGND across the closed switch to limit the current to 1.5 A for 500 μs. This will prevent a short from VBUS to AGND through SBUx. OCP will not automatically reset. When an OCP event occurs an interrupt will be sent to the processor. The interrupt is cleared by reading the I_OCP_AGND register. The SBUx to AGND switch can be closed after an OCP event by setting AGND_EN = 1b.

MIC Switch Auto−Off

MIC switch auto−off is controlled by the MIC_AUTO_OFF register (12h, Bit 2). If enabled, when the port is configured for audio (L, R, MIC, AGND switches are closed) and a detach is detected (CC_IN > 1.5 V) the receptacle side of the MIC switch will connect to ground for 50 μs prior to becoming high impedance.

Headset Detection

Headset detection is performed by the CC_IN input and indicated by the CC_IN_STAT register (11h, Bit 2). Headset detection can also be indicated by the DET output. DET is an Open Drain user configurable attach/detach detection output. It can be configured or disabled from the I²C register DET_FUNCT. The DET output once triggered can be cleared by reading the Detection Interrupt Register I_DET_FUNCT. When configured for Type−C or Audio

Accessory attach detection DET will clear automatically when the Type−C device or audio accessory is detached.

Value	DET_FUNCT	Description
00b	00b: Type-C Attach Detection, DET = LOW if CC_IN_STAT = 0b	Type-C Attach Detect
01b	01b: Audio Accessory Attach Detection, DET = LOW if NO_AUDIO_ACC = 0b	Audio Accessory Attach Detect
10b	10b: Audio Accessory Detach Detection, DET = LOW if CC_IN_STAT transitions from 0b to 1b	Audio Accessory Detach Detect
11b	Disabled, DET = Hi-Z (DEFAULT)	Disabled

Figure 5. Detect Pin Function

Gate Drive

The FSA4485 includes two gate drive outputs GD1 and GD2 to allow a low resistance external switch to be used for AGND. The gate drives are enabled from the I^2C register GATE_DRIVE_EN and will follow automatic orientation detection. When enabled, if SBU1 = AGND then GD1 = High, If SBU2 = AGND then GD2 = High.

The gate to source voltage (Vgs) will be held at V_GATE to ensure low on resistance. The maximum gate drive current can be selected from the I^2C register GATE_DRIVE_CURR to control switch turn on time.

GATE DRIVE CURRENT

Register Value	GATE_DRIVE_CURR
00b	1 μA
01b	1.5 μA
10b	2.0 μA (default)
11b	3.0 μA

EN and Factory Mode

The enable input (EN) is a 3 state input which sets the USB and SBU data switch initial conditions during device power up. It has a weak internal pull down which will set the default condition to High−Z if no input level is present. For applications using the SBU signals for data the EN input can be floated or connected to a GPIO in High−Z state at power up. For typical conditions EN can be tied to GND. EN is tied to GND using a 10 kΩ resistor if also using the EN input to disable the device. It is not recommended that the EN = High−Z condition be used if the system uses SBU for the DisplayPort Aux channel.

EN	Initial Condition			Operating Condition		
	USB 2.0	SBUx	Device	USB 2.0	SBUx	Device
LOW	DP/DN	OPEN	Enabled	Set from I2C Register		Enabled
High-Z	DP/DN	S1H/S2H	Enabled	Set from I2C Register		Enabled
HIGH	OPEN	OPEN	Disabled	OPEN	OPEN	Disabled

Figure 6. EN Input Truth Table

Moisture Detection

The moisture detection function is controlled the RES_DETECT register (12h, Bit 1). It will detect moisture or any foreign object that creates resistance between the receptacle side pins and ground. During resistance detection, the switch associated with the pin will be open. The detection result will be saved in the RES_VALUE register (14h). The measurement range is from 1 kΩ to 2.56 MΩ and is controlled by the RES_DET_RANGE register (12h, Bit 5). Detection can be performed manually or an automatic detection interval can be set to 100 ms, 1 s or 10 s by the RED_DET_INTV register (16h).

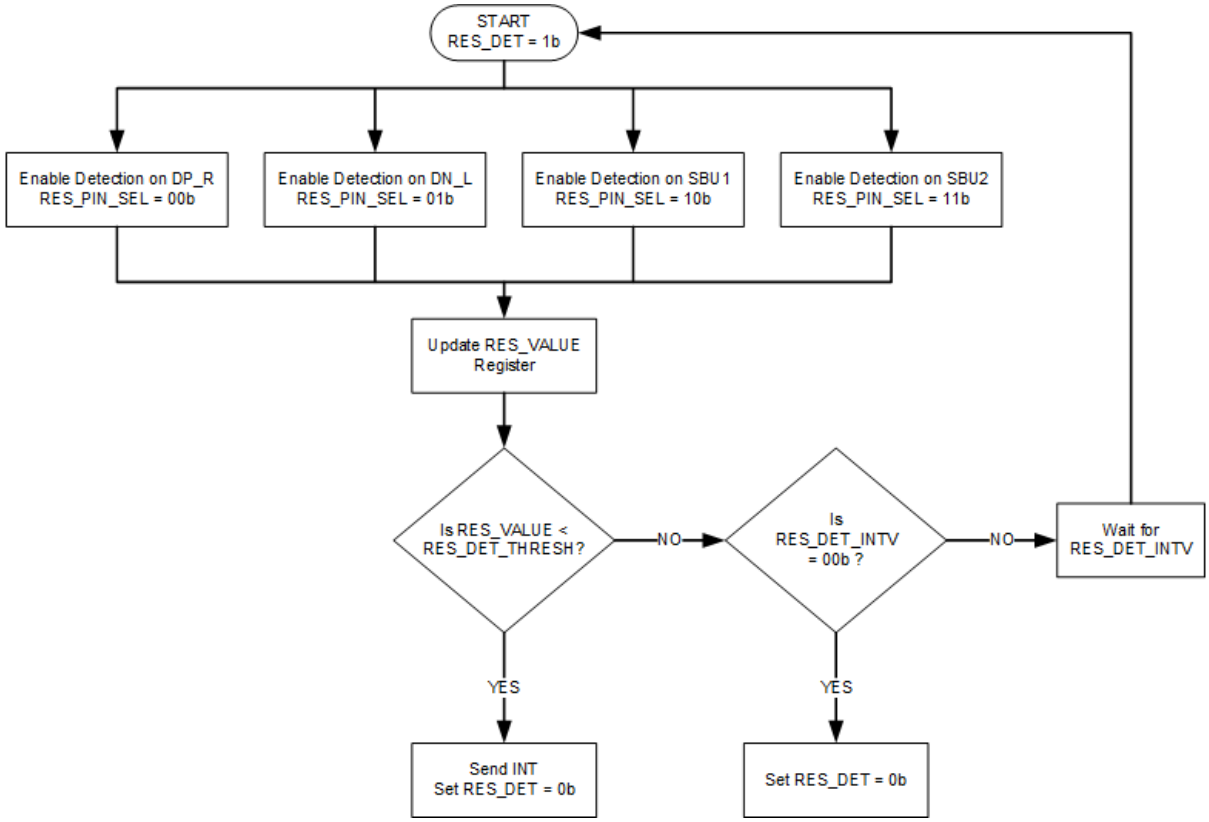


Figure 7. Moisture Detection Procedure

Test Diagrams

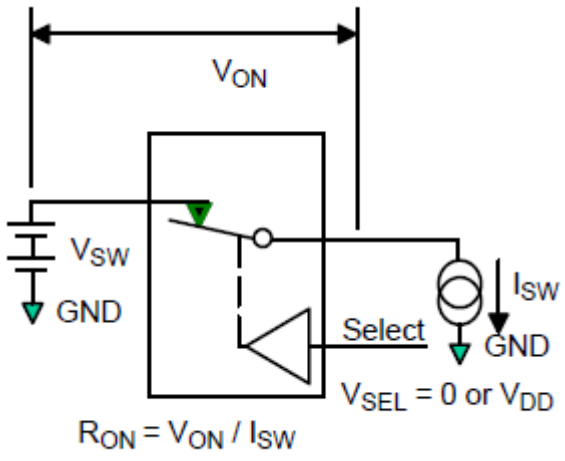


Figure 9. On Resistance

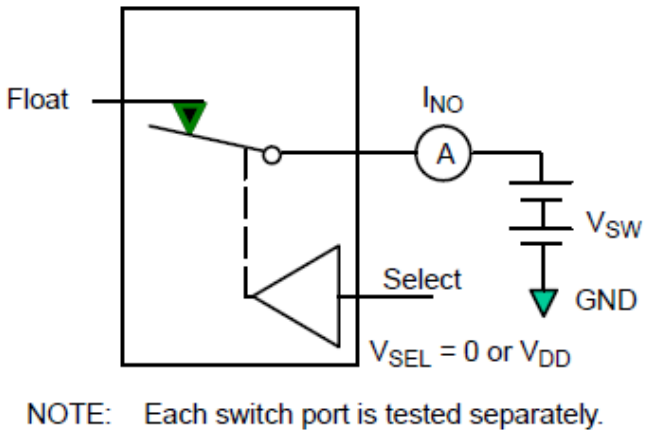


Figure 8. Off Leakage (IOZ)

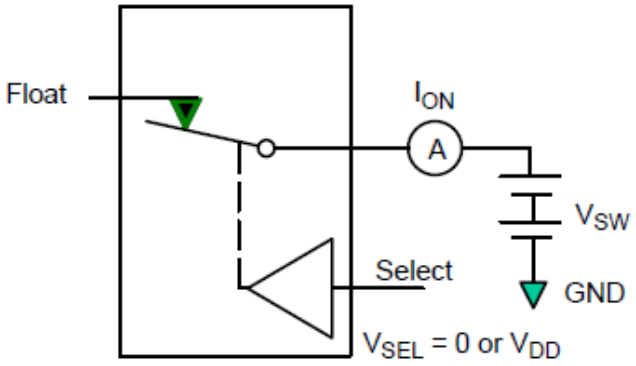


Figure 10. On Leakage

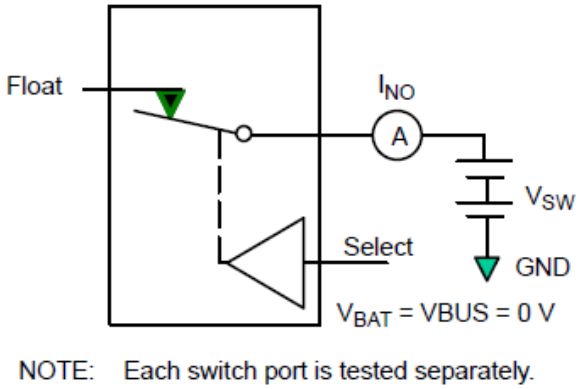


Figure 11. Power Off Leakage (IOFF)

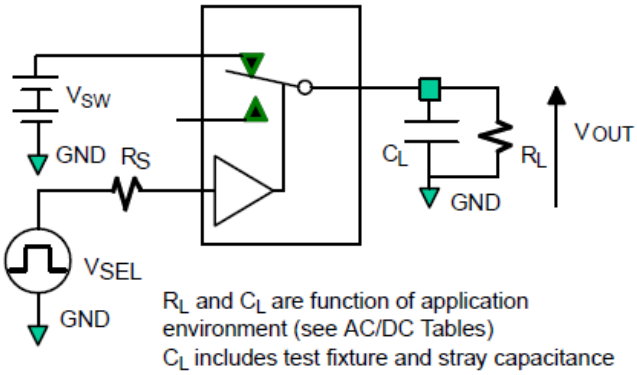


Figure 12. Test Circuit Load

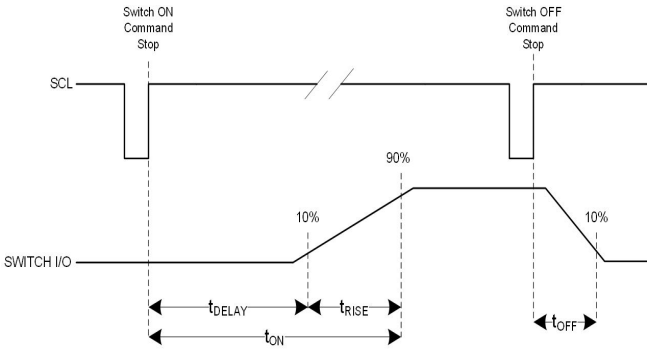


Figure 13. Manual Mode Turn On/Off Waveform

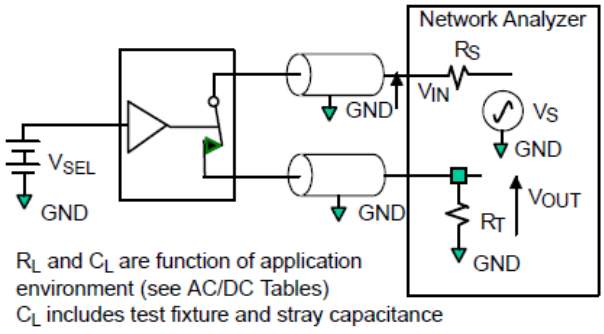


Figure 14. Bandwidth

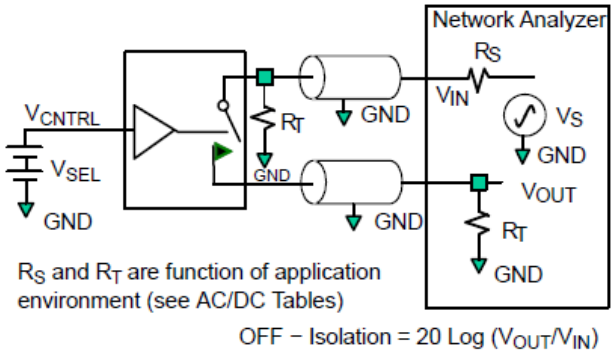


Figure 15. Channel Off Isolation

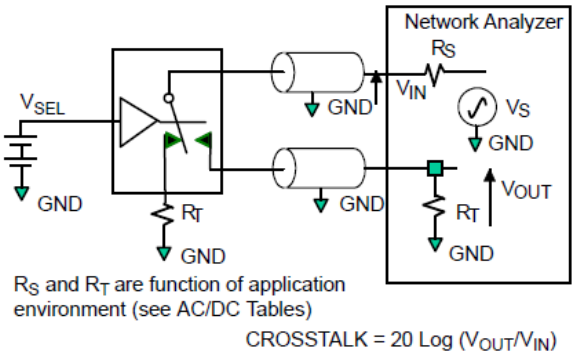


Figure 16. Adjacent Channel Crosstalk

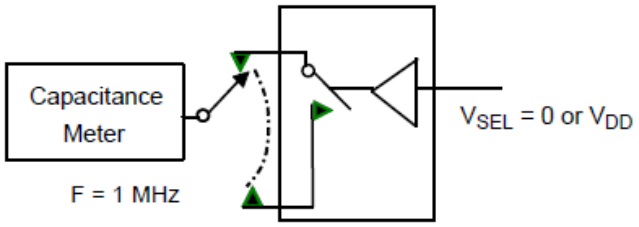


Figure 17. Channel Off Capacitance

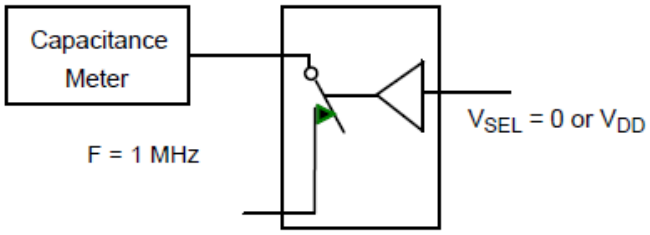


Figure 18. Channel Off Capacitance

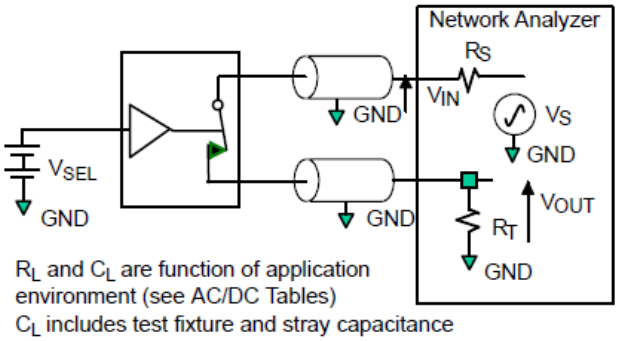


Figure 19. Total Harmonic Distortion (THD + N)

REGISTER MAPPING TABLE

REGISTER MAPPING

					Read Only	Write Only	Read / Write	Read / Clear	Write / Clear
Address	**Name**	**Bit[7]**	**Bit[6]**	**Bit[5]**	**Bit[4]**	**Bit[3]**	**Bit[2]**	**Bit[1]**	**Bit[0]**
0x00	DEVID	VENID		VERID			REVID		
0x01	OVP_MASK	M_OCP_AGND	M_OVP_ALL	M_OVP_DP_R	M_OVP_DN_L	M_OVP_SBU1	M_OVP_SBU2	M_OVP_GSBU1	M_OVP_GSBU2
0x02	OVP_INTERRUPT	I_OCP_AGND	I_OVP_ALL	I_OVP_DP_R	I_OVP_DN_L	I_OVP_SBU1	I_OVP_SBU2	I_OVP_GSBU1	I_OVP_GSBU2
0x03	OVP_STAT	Reserved	OCP_STAT _AGND	OVP_STAT _DP_R	OVP_STAT _DN_L	OVP_STAT _SBU1	OVP_STAT _SBU2	OVP_STAT _GSBU1	OVP_STAT _GSBU2
0x04	SWITCH_EN	DEVICE_EN	S1H_EN	S2H_EN	DN_L_EN	DP_R_EN	SENSE_EN	MIC_EN	AGND_EN
0x05	SWITCH_SEL	Reserved	S1H_SEL	S2H_SEL	DN_L_SEL	DP_R_SEL	SENSE_SEL	MIC_SEL	AGND_SEL
0x06	SWITCH_STAT_1	Reserved		SENSE_STAT		DP_R_STAT		DN_L_STAT	
0x07	SWITCH_STAT_2	Reserved		SBU2_STAT			SBU1_STAT		
0x08	AUDIO_SLO W_LEFT	AUDIO_SLOW_LEFT							
0x09	AUDIO_SLO W_RIGHT	AUDIO_SLOW_RIGHT							
0x0A	MIC_SLOW	MIC_SLOW							
0x0B	SENSE_SLOW	SENSE_SLOW							
0x0C	AGND_SLOW	AGND_SLOW							
0x0D	L2R_EN_DELAY	L2R_EN_DELAY							
0x0E	MIC2L_EN_ DELAY	MIC2L_EN _DELAY							
0x0F	SENSE2L_EN_DELAY	SENSE2L_EN_DELAY							
0x10	AGND2L_EN_DELAY	AGND2L_EN_DELAY							
0x11	AUDIO_ACC_STAT	Reserved						CC_IN_STAT	DET_STAT
0x12	FUNCTION_ EN	DET_FUNCT		RES_DET _RANGE	HIZ_ACC_DET	SLOW_TURN _ON	MIC_AUT_OFF	RES_DETECT	AUDIO_JACK _DET
0x13	RES_PIN_SEL	Reserved					RES_PIN_SEL		
0x14	RES_VALUE	RES_VALUE							
0x15	RES_DET_THRESH	RES_DET_THRESH							
0x16	RES_DET_INTV	Reserved						RES_DET_INTV	
0x17	AUDIO_JACK_STAT	Reserved			UNKNOWN _AUDIO_ACC	4POLE_A	4POLE_B	3POLE	NO_AUDIO_ACC
0x18	DET_INTERRUPT	Reserved			I_DISABLE	I_DET_FUNCT	I_AUDIO_JACK _DET	I_LOW_RES	I_RES_DET _COMP
0x19	DET_MASK	Reserved			M_DISABLE	M_DET	M_AUDIO _JACK_DET	M_LOW_RES	M_RES
0x1A	AUDIO_JACK_DET1	AUDIO_JACK_DET1							
0x1B	AUDIO_JACK_DET2	AUDIO_JACK_DET2							
0x1C	MIC_DET_TH_LOW	MIC_DET_TH_LOW							
0x1D	MIC_DET_TH_UP	MIC_DET_TH_UP							
0x1E	I2C_RESET	Reserved							I2C_RESET
0x1F	CURR_SOURCE_SET	Reserved						CURR_SOURCE_SET	
0x20	CURR_SOURCE_STAT	Reserved						CURR_SOURCE_STAT	
0x21	GATE_DRIVE	Reserved					GATE_DRIVE _EN	GATE_DRIVE_CURR	
0x22	PROTECTION_EN	Reserved						EN_OVP	EN_OCP
0x23	PROTECTION_STAT	Reserved		USB_OVP	GSBU_OVP	SBU1_OVP	SBU2_OVP	OCP1	OCP2

REGISTER DETAILS

Table 3. DEVICE ID

0x00 DEVID				Default = 00001001
Bit	**Name**	**Default**	**Type**	**Description**
7:6	VENID	00	Read	Vendor ID
5:3	VERID	001	Read	Revision ID Low: 001h A_[Revision ID]: 0x001 (e.g. A_revA) B_[Revision ID]: 0x010 (e.g. B_revA) C_[Revision ID]: 0x011 (e.g. C_revA) etc
2:0	REVID	001	Read	Revision ID Low: 001h A_[Revision ID]: 0x001 (e.g. A_revA) B_[Revision ID]: 0x010 (e.g. A_revB) C_[Revision ID]: 0x011 (e.g. A_revC) etc

Table 4. OVP/OCP INTERRUPT MASK

0x01 OVP_MASK				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7	M_OCP_AGND	0	R/W	0b: Do not mask OCP interrupt 1b: Mask OCP interrupt on SBUx to AGND
6	M_OVP_ALL	0	R/W	0b: OCP Mask is controled by bit 7, OVP Mask is controled by bit [5:0] 1b: Mask OVP/OCP interrupt on all connector side pins
5	M_OVP_DP_R	0	R/W	0b: Do not mask OVP interrupt 1b: Mask OVP interrupt on DP_R
4	M_OVP_DN_L	0	R/W	0b: Do not mask OVP interrupt 1b: Mask OVP interrupt on DN_L
3	M_OVP_SBU1	0	R/W	0b: Do not mask OVP interrupt 1b: Mask OVP interrupt on SBU1
2	M_OVP_SBU2	0	R/W	0b: Do not mask OVP interrupt 1b: Mask OVP interrupt on SBU2
1	M_OVP_GSBU1	0	R/W	0b: Do not mask OVP interrupt 1b: Mask OVP interrupt on GSBU1
0	M_OVP_GSBU2	0	R/W	0b: Do not mask OVP interrupt 1b: Mask OVP interrupt on GSBU2

Table 5. OVP/OCP INTERRUPT FLAG

0x02 OVP_INTERRUPT				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7	I_OCP_AGND	0	R/CLR	0b: OCP has not occured 1b: OCP event has occured on SBUx to AGND
6	I_OVP_ALL	0	R/CLR	0b: OVP or OCP event has not occurred 1b: OVP or OCP event has occurred
5	I_OVP_DP_R	0	R/CLR	0b: OVP event has not occured 1b: OVP event has occurred on DP_R
4	I_OVP_DN_L	0	R/CLR	0b: OVP event has not occured 1b: OVP event has occurred on DN_L
3	I_OVP_SBU1	0	R/CLR	0b: OVP event has not occured 1b: OVP event has occurred on SBU1
2	I_OVP_SBU2	0	R/CLR	0b: OVP event has not occured 1b: OVP event has occurred on SBU2
1	I_OVP_GSBU1	0	R/CLR	0b: OVP event has not occured 1b: OVP event has occurred on GSBU1
0	I_OVP_GSBU2	0	R/CLR	0b: OVP event has not occured 1b: OVP event has occurred on GSBU2

Table 6. OVP/OCP STATUS

0x03 OVP_STAT				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7	Reserved	0	Read	Do Not Use
6	OCP_STAT_AGND	0	Read	0b: OCP event has not occured 1b: OCP event has occurred on SBUx to AGND
5	OVP_STAT_DP_R	0	Read	0b: OVP event has not occured 1b: OVP event has occurred on DP R
4	OVP_STAT_DN_L	0	Read	0b: OVP event has not occured 1b: OVP event has occurred on DN L
3	OVP_STAT_SBU1	0	Read	0b: OVP event has not occured 1b: OVP event has occurred on SBU1
2	OVP_STAT_SBU2	0	Read	0b: OVP event has not occured 1b: OVP event has occurred on SBU2
1	OVP_STAT_GSBU1	0	Read	0b: OVP event has not occured 1b: OVP event has occurred on GSBU1
0	OVP_STAT_GSBU2	0	Read	0b: OVP event has not occured 1b: OVP event has occurred on GSBU2

Table 7. SWITCH ENABLE

0x04 SWITCH_EN				Default = 10011000
Bit	**Name**	**Default**	**Type**	**Description**
7	DEVICE_EN	1	R/W	0b: Device Disabled, L and R = 10 kΩ Pull Down, All Other Switches = High−Z, this overrides EN = Low 1b: Device Enabled, All Switches are Enabled, this can be overridden by EN = High
6	S1H_EN	0	R/W	0b: Switch Disabled, S1H = High−Z 1b: SBUx to S1H Switch Enabled
5	S2H_EN	0	R/W	0b: Switch Disabled, S2H = High−Z 1b: SBUx to S2H Switch Enabled
4	DN_L_EN	1	R/W	0b: Switch Disabled, DN = High−Z, L = 10 kΩ Pull Down 1b: DN L Switch Enabled
3	DP_R_EN	1	R/W	0b: Switch Disabled, DP = High−Z, R = 10 kΩ Pull Down 1b: DP R Switch Enabled
2	SENSE_EN	0	R/W	0b: Switch Disabled, SENSE, GSBU1 and GSBU2 = High−Z 1b: SENSE Switch Enabled
1	MIC_EN	0	R/W	0b: Switch Disabled, MIC = High−Z 1b: MIC to SBUx Switch Enabled If S1H EN and/or S2H EN = 1b then MIC will = High−Z when MIC EN = 1b
0	AGND_EN	0	R/W	0b: Switch Disabled, AGND = High−Z 1b: AGND to SBUx Switch Enabled If S1H EN and/or S2H EN = 1b then AGND will = High−Z when AGND EN = 1b

Table 8. SWITCH SELECT

0x05 SWITCH_SEL				Default = 00011000
Bit	**Name**	**Default**	**Type**	**Description**
7	Reserved	0	R/W	Do Not Use
6	S1H_SEL	0	R/W	0b: S1H to SBU1 switch is CLOSED 1b: S1H to SBU2 switch is CLOSED
5	S2H_SEL	0	R/W	0b: S2H to SBU2 switch is CLOSED 1b: S2H to SBU1 switch is CLOSED
4	DN_L_SEL	1	R/W	0b: DN_L to L switch is CLOSED 1b: DN L to DN switch is CLOSED
3	DP_R_SEL	1	R/W	0b: DP_R to R switch is CLOSED 1b: DP R to DP switch is CLOSED
2	SENSE_SEL	0	R/W	0b: SENSE to GSBU1 switch is CLOSED 1b: SENSE to GSBU2 switch is CLOSED
1	MIC_SEL	0	R/W	0b: MIC to SBU2 switch is CLOSED 1b: MIC to SBU1 switch is CLOSED If AGND_SEL = 0b and MIC_SEL = 1b when AGND_EN and MIC_EN = 1b then MIC = High−Z If AGND SEL = 1b and MIC SEL = 0b when AGND EN and MIC EN = 1b then MIC = High−Z
0	AGND_SEL	0	R/W	0b: AGND to SBU1 switch is CLOSED 1b: AGND to SBU2 switch is CLOSED

Table 9. SWITCH STATUS 1

0x06 SWITCH_STAT_1				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:6	Reserved	00	Read	Do Not Use
5:4	SENSE_STAT	00	Read	00b: SENSE switch is OPEN 01b: SENSE switch is CLOSED to GSBU1 10b: SENSE Switch is CLOSED to GSBU2 11b: Not Valid
3:2	DP_R_STAT	00	Read	00b: DP_R switch is OPEN 01b: DP_R switch is CLOSED to DP 10b: DP_R Switch is CLOSED to R 11b: Not Valid
1:0	DN_L_STAT	00	Read	00b: DN_L switch is OPEN 01b: DN_L switch is CLOSED to DN 10b: DN_L Switch is CLOSED to L 11b: Not Valid

Table 10. SWITCH STATUS 2

0x07 SWITCH_STAT_2				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:6	Reserved	00	Read	Do Not Use
5:3	SBU2_STAT	000	Read	000b: SBU2 switch is OPEN 001b: SBU2 switch is CLOSED to MIC 010b: SBU2 Switch is CLOSED to AGND 011b: SBU2 Switch is CLOSED to S1H 100b: SBU2 Switch is CLOSED to S2H 101b: SBU2 Switch is CLOSED to both S1H and S2H 110b: Not Valid 111b: Not Valid
2:0	SBU1_STAT	000	Read	000b: SBU1 switch is OPEN 001b: SBU1 switch is CLOSED to MIC 010b: SBU1 Switch is CLOSED to AGND 011b: SBU1 Switch is CLOSED to S1H 100b: SBU1 Switch is CLOSED to S2H 101b: SBU1 Switch is CLOSED to both S1H and S2H 110b: Not Valid 111b: Not Valid

Table 11. AUDIO SWITCH LEFT CHANNEL SLOW TURN ON TIME

0x08 AUDIO_SLOW_LEFT				Default = 00000001
Bit	**Name**	**Default**	**Type**	**Description**
7:0	AUDIO_SLOW_LEFT	00000001	R/W	00000000b: = 180 μs 00000001b: = 330 μs (DEFAULT) Typical turn on time (tON) is incremented approximately 150 μs per bit

Table 12. AUDIO SWITCH RIGHT CHANNEL SLOW TURN ON TIME

0x09 AUDIO_SLOW_RIGHT				Default = 00000001
Bit	**Name**	**Default**	**Type**	**Description**
7:0	AUDIO_SLOW_RIGHT	00000001	R/W	00000000b: = 180 μs 00000001b: = 330 μs (DEFAULT) Typical turn on time (tON) is incremented approximately 150 μs per bit

Table 13. MIC SWITCH SLOW TURN ON TIME

0x0A MIC_SLOW				Default = 00000010
Bit	**Name**	**Default**	**Type**	**Description**
7:0	MIC_SLOW	00000010	R/W	00000000b: = Do Not Use 00000001b: = 370 μs 00000010b: = 520 μs (DEFAULT) Typical turn on time (tON) is incremented approximately 150 μs per bit

Table 14. SENSE SWITCH SLOW TURN ON TIME

0x0B SENSE_SLOW				Default = 00000001
Bit	**Name**	**Default**	**Type**	**Description**
7:0	SENSE_SLOW	00000001	R/W	00000000b: = 160 μs 00000001b: = 220 μs (DEFAULT) Typical turn on time (tON) is incremented approximately 60 μs per bit

Table 15. AGND SWITCH SLOW TURN ON TIME

0x0C AGND_SLOW				Default = 00000001
Bit	**Name**	**Default**	**Type**	**Description**
7:0	AGND_SLOW	00000001	R/W	00000000b: = 900 μs 00000001b: = 1750 μs (DEFAULT) Typical turn on time (tON) is incremented approximately 850 μs per bit

Table 16. TIMING DELAY BETWEEN AUDIO L AND AUDIO R SWITCH ENABLE

0x0D L2R_EN_DELAY				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:0	L2R_EN_DELAY	00000000	R/W	00000000b: = 0 μs (DEFAULT) 00000001b: = 100 μs …….. 11111111b: = 25500 μs Increment size is 100 μs per bit

Table 17. TIMING DELAY BETWEEN AUDIO MIC AND AUDIO L SWITCH ENABLE

0x0E MIC2L_EN_DELAY				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:0	MIC2L_EN_DELAY	00000000	R/W	00000000b: = 0 μs (DEFAULT) 00000001b: = 100 μs …….. 11111111b: = 25500 μs Increment size is 100 us per bit

Table 18. TIMING DELAY BETWEEN SENSE SWITCH AND AUDIO L SWITCH ENABLE

0x0F SENSE2L_EN_DELAY				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:0	SENSE2L_EN_DELAY	00000000	R/W	00000000b: = 0 μs (DEFAULT) 00000001b: = 100 μs …….. 11111111b: = 25500 μs Increment size is 100 μs per bit

Table 19. TIMING DELAY BETWEEN AGND SWITCH AND AUDIO L SWITCH ENABLE

0x10 AGND2L_EN_DELAY				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:0	AGND2L_EN_DELAY	00000000	R/W	00000000b: = 0 μs (DEFAULT) 00000001b: = 100 μs …….. 11111111b: = 25500 μs Increment size is 100 μs per bit

Table 20. AUDIO ACCESSORY STATUS

0x11 AUDIO_ACC_STAT				Default = 00000011
Bit	**Name**	**Default**	**Type**	**Description**
7:2	Reserved	000000	Read	Reserved
1	CC_IN_STAT	1	Read	0b: CC_IN < V_TH_L_CC 1b: CC_IN > V_TH_H_CC
0	DET_STAT	1	Read	0b: DET output is LOW 1b: DET output is High−Z

Table 21. AUTOMATIC FUNCTION ENABLE

0x12 FUNCTION_EN				Default = 11001000
Bit	**Name**	**Default**	**Type**	**Description**
7:6	DET_FUNCT	11	R/W	DET Output Configuration 00b: Type−C Attach Detection, DET = LOW if CC_IN_STAT = 0b 01b: Audio Accessory Attach Detection, DET = LOW if NO_AUDIO_ACC = 0b 10b: Audio Accessory Detach Detection, DET = LOW if CC_IN_STAT transitions from 0b to 1b 11b: Disabled, DET = High−Z (DEFAULT)
5	RES_DET_RANGE	0	R/W	Resistor Detection Range Setting 0b: 1 kΩ to 256 kΩ 1b: 10 kΩ to 2560 kΩ
4	HIZ_ACC_DET	0	R/W	High Impedance Audio Accessory Detection 0b: Automatic Hi−Z Accessory Detection is disabled 1b: Automatic Hi−Z Accessory Detection is enabled
3	SLOW_TURN_ON	1	R/W	Switch Slow Turn On Control Enable 0b: Disabled 1b: Enabled
2	MIC_AUTO_OFF	0	R/W	0b: MIC Switch Auto Off Function is Disabled 1b: MIC Switch Auto Off Function is Enabled
1	RES_DETECT	0	R/W	Resistance Detection Enabled 0b: Resistance Detection is Disabled 1b: Resistance Detection is Enabled Automatically reset to 0b by I LOW RES = 1b
0	AUDIO_JACK_DET	0	R/W	Audio Jack Detection and Configuration Enabled 0b: Audio Jack Detection is Disabled 1b: Audio Jack Detection and Configuration is Enabled Automatically reset to 0b by I AUDIO JACK DET = 1b

Table 22. RESISTOR DETECTION PIN SELECTION

0x13 RES_PIN_SEL				Default = 00000001
Bit	**Name**	**Default**	**Type**	**Description**
7:3	Reserved	00000	R/W	Do Not Use
2:0	RES_PIN_SEL	001	R/W	000b: Not Valid 001b: DP_R (DEFAULT) 010b: DN_L 011b: SBU1 100b: SBU2 101b to 111b: Not Valid RES PIN SEL must be set prior to setting RES DETECT to Enabled

Table 23. DETECTED RESISTOR VALUE

0x14 RES_VALUE				Default = 11111111
Bit	**Name**	**Default**	**Type**	**Description**
7:0	RES_VALUE	11111111	Read	00000000b: R <= 1 kΩ / 10 kΩ 11111111b: R >= 256 kΩ / 2.56 MΩ Increment = 10 kΩ per bit if RES_DET_RANGE = 0b Increment = 1 kΩ per bit if RES DET RANGE = 1b

Table 24. RESISTOR DETECTION THRESHOLD

0x15 RES_DET_THRESH				Default = 00010110
Bit	**Name**	**Default**	**Type**	**Description**
7:0	RES_DET_THRESH	00010110	R/W	00000000b: 1 kΩ / 10 kΩ ..... 00010110b: 23 kΩ / 230 kΩ (DEFAULT) ..... 11111111b: 256 kΩ / 2560 kΩ Increment = 10 kΩ per bit if RES_DET_RANGE = 0b Increment = 1 kΩ per bit if RES DET RANGE = 1b

Table 25. AUTOMATIC RESISTANCE DETECTION TIME INTERVAL

0x16 RES_DET_INTV				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:2	Reserved	000000	R/W	Do Not Use
1:0	RES_DET_INTV	00	R/W	00b: One Time Detection 01b: Detection is performed every 100 ms 10b: Detection is performed every 1 s 11b: Detection is performed every 10 s

Table 26. AUDIO JACK STATUS

0x17 AUDIO_JACK_STAT				Default = 00000001
Bit	**Name**	**Default**	**Type**	**Description**
7:5	Reserved	000	Read	Do Not Use
4	UNKNOWN_AUDIO_ACC	0	Read	0b: OTHER 1b: Unknown Audio Accessory
3	4POLE_A	0	Read	0b: OTHER 1b: 4 Pole Audio, SBU2 to MIC, SBU1 to AGND
2	4POLE_B	0	Read	0b: OTHER 1b: 4 Pole Audio, SBU1 to MIC, SBU2 to AGND
1	3POLE	0	Read	0b: OTHER 1b: 3 Pole Audio
0	NO_AUDIO_ACC	1	Read	0b: Audio Accessory Attached 1b: No Audio Accessory

Table 27. RESISTANCE AND AUDIO JACK DETECTION INTERRUPT

0x18 DET_INTERRUPT				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:5	Reserved	000	R/CLR	Do Not Use
4	I_DISABLE	0	R/CLR	A hardware disable has occurred due to EN = High 0b: The device has not been disabled 1b: The device was disabled
3	I_DET_FUNCT	0	R/CLR	Audio Accessory Detach has occurred 0b: DET_FUNCT = 00b, 01b, 11b, or DET_FUNCT = 10b and DET_STAT= 1b 1b: DET_FUNCT = 10b and DET_STAT = 0b Clearing I DET FUNCT will return the DET output to High−Z
2	I_AUDIO_JACK_DET	0	R/CLR	0b: Audio Jack Detection and Configuration has not occurred 1b: Audio Jack Detection and Configuration has occurred
1	I_LOW_RES	0	R/CLR	0b: A Resistance < RES_DET_THRESH has not been detected 1b: A Resistance < RES DET THRESH has been detected
0	I_RES_DET_COMP	0	R/CLR	0b: Resistance Detection has not been completed 1b: Resistance Detection has been completed

Table 28. RESISTANCE AND AUDIO JACK DETECTION INTERRUPT MASK

0x19 DET_MASK				Default = 00001000
Bit	**Name**	**Default**	**Type**	**Description**
7:5	Reserved	000	R/W	Do Not Use
4	M_DISABLE	0	R/W	0b: Do not mask Device Disable interrupt 1b: Mask Device Disable interrupt
3	M_DET_FUNCT	1	R/W	0b: Do not mask Audio Accessory Detach interrupt 1b: Mask Audio Accessory Detach interrupt
2	M_AUDIO_JACK_DET	0	R/W	0b: Do not mask Audio Jack Detection and Configuration interrupt 1b: Mask Audio Jack Detection and Configuration interrupt
1	M_LOW_RES	0	R/W	0b: Do not mask Low Resistance Detection interrupt 1b: Mask Low Resistance Detection interrupt
0	M_RES_DET_COMP	0	R/W	0b: Do not mask Resistance Detection completed interrupt 1b: Mask Resistance Detection completed interrupt

Table 29. AUDIO JACK MIC/AGND ORIENTATION DETECTION 1

0x1A AUDIO_JACK_DET1				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:0	AUDIO_JACK_DET1	00000000	Read	Voltage from resistance between SBU1 and SBU2 (SBU2 = ground) 00000000b: = 0 V …….. 11111111b: = 2.4 V Increment is 9.375 mV per bit Resistance is calculated as AUDIO_JACK_DET1 / CURR_SOURCE_SET

Table 30. AUDIO JACK MIC/AGND ORIENTATION DETECTION 2

0x1B AUDIO_JACK_DET2				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:0	AUDIO_JACK_DET2	00000000	Read	Voltage from resistance between SBU2 and SBU1 (SBU1 = ground) 00000000b: = 0 V …….. 11111111b: = 2.4 V Increment is 9.375 mV per bit Resistance is calculated as AUDIO_JACK_DET2 / CURR_SOURCE_SET

Table 31. LOWER MIC DETECTION THRESHOLD VOLTAGE

0x1C MIC_DET_TH_LOW				Default = 00100000
Bit	**Name**	**Default**	**Type**	**Description**
7:0	MIC_DET_TH_LOW	00100000	R/W	00000000b: = 0 mV …….. 00100000b: = 300 mV (DEFAULT) …….. 11111111b: = 2.4 V Increment = 9.375 mV per bit

Table 32. UPPER MIC DETECTION THRESHOLD VOLTAGE

0x1D MIC_DET_TH_UP				Default = 11111111
Bit	**Name**	**Default**	**Type**	**Description**
7:0	MIC_DET_TH_UP	11111111	R/W	00000000b: = 0 mV …….. 00100000b: = 300 mV …….. 11111111b: = 2.4 V (DEFAULT) Increment = 9.375 mV per bit

Table 33. I^2C REGISTER RESET

0x1E I2C_RESET				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:1	Reserved	0000000	W1CLR	Do Not Use
0	I2C_RESET	0	W1CLR	0b: DEFAULT 1b: Reset all I^2C Register Values to Default

Table 34. RESISTANCE DETECTION CURRENT SOURCE

0x1F CURR_SOURCE_SET				Default = 00000010
Bit	**Name**	**Default**	**Type**	**Description**
7:2	Reserved	000000	Write	Do Not Use
1:0	CURR_SOURCE_SET	10	Write	00b: 20 μA 01b: 100 μA 10b: 700 μA (DEFAULT) 11b: 1500 μA

Table 35. DETECTION CURRENT STATUS

0x20 CURR_SOURCE_STAT				Default = 00000010
Bit	**Name**	**Default**	**Type**	**Description**
7:2	Reserved	000000	Read	Do Not Use
1:0	CURR_SOURCE_STAT	10	Read	00b: 20 μA 01b: 100 μA 10b: 700 μA (DEFAULT) 11b: 1500 μA

Table 36. EXTERNAL GATE DRIVE OUTPUT CONTROL

0x21 GATE_DRIVE				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:3	Reserved	00000	R/W	Do Not Use
2	GATE_DRIVE_EN	0	R/W	0b: External Gate Drive GD1 and GD2 are Disabled (DEFAULT) 1b: External Gate Drive GD1 and GS2 are Enabled
1:0	GATE_DRIVE_CURR	00	R/W	00b: 1 μA (DEFAULT) 01b: 1.5 μA 10b: 2 μA 11b: 3 μA

Table 37. OVER VOLTAGE AND OVER CURRENT PROTECTION ENABLE

0x22 PROTECTION_EN				Default =00000011
Bit	**Name**	**Default**	**Type**	**Description**
7:2	Reserved	000000	R/W	Do Not Use
1	EN_OVP	1	R/W	0b: Over Voltage Protection is Disabled 1b: Over Voltage Protection is Enabled (DEFAULT)
0	EN_OCP	1	R/W	0b: Over Current Protection is Disabled 1b: Over Current Protection is Enabled (DEFAULT)

Table 38. OVER VOLTAGE AND OVER CURRENT PROTECTION STATUS

0x23 PROTECTION_STAT				Default = 00100000
Bit	**Name**	**Default**	**Type**	**Description**
7:6	Reserved	00	Read	Do Not Use
5	USB_OVP	1	Read	0b: Over Voltage Protection on DP_R and DN_L is Disabled 1b: Over Voltage Protection on DP_R and DN_L is Enabled (DEFAULT)
4	GSBU_OVP	0	Read	0b: Over Voltage Protection on GSBUx is Disabled (DEFAULT) 1b: Over Voltage Protection on GSBUx is Enabled
3	SBU1_OVP	0	Read	0b: Over Voltage Protection on SBU1 is Disabled (DEFAULT) 1b: Over Voltage Protection on SBU1 is Enabled
2	SBU2_OVP	0	Read	0b: Over Voltage Protection on SBU2 is Disabled (DEFAULT) 1b: Over Voltage Protection on SBU2 is Enabled
1	OCP1	0	Read	0b: Over Current Protection from SBU1 to AGND is Disabled (DEFAULT) 1b: SBU1 STAT = 010b, Over Current Protection from SBU1 to AGND is Enabled
0	OCP2	0	Read	0b: Over Current Protection from SBU2 to AGND is Disabled (DEFAULT) 1b: SBU2_STAT = 010b, Over Current Protection from SBU2 to AGND is Enabled

APPLICATION CIRCUIT

Application Circuit Diagram

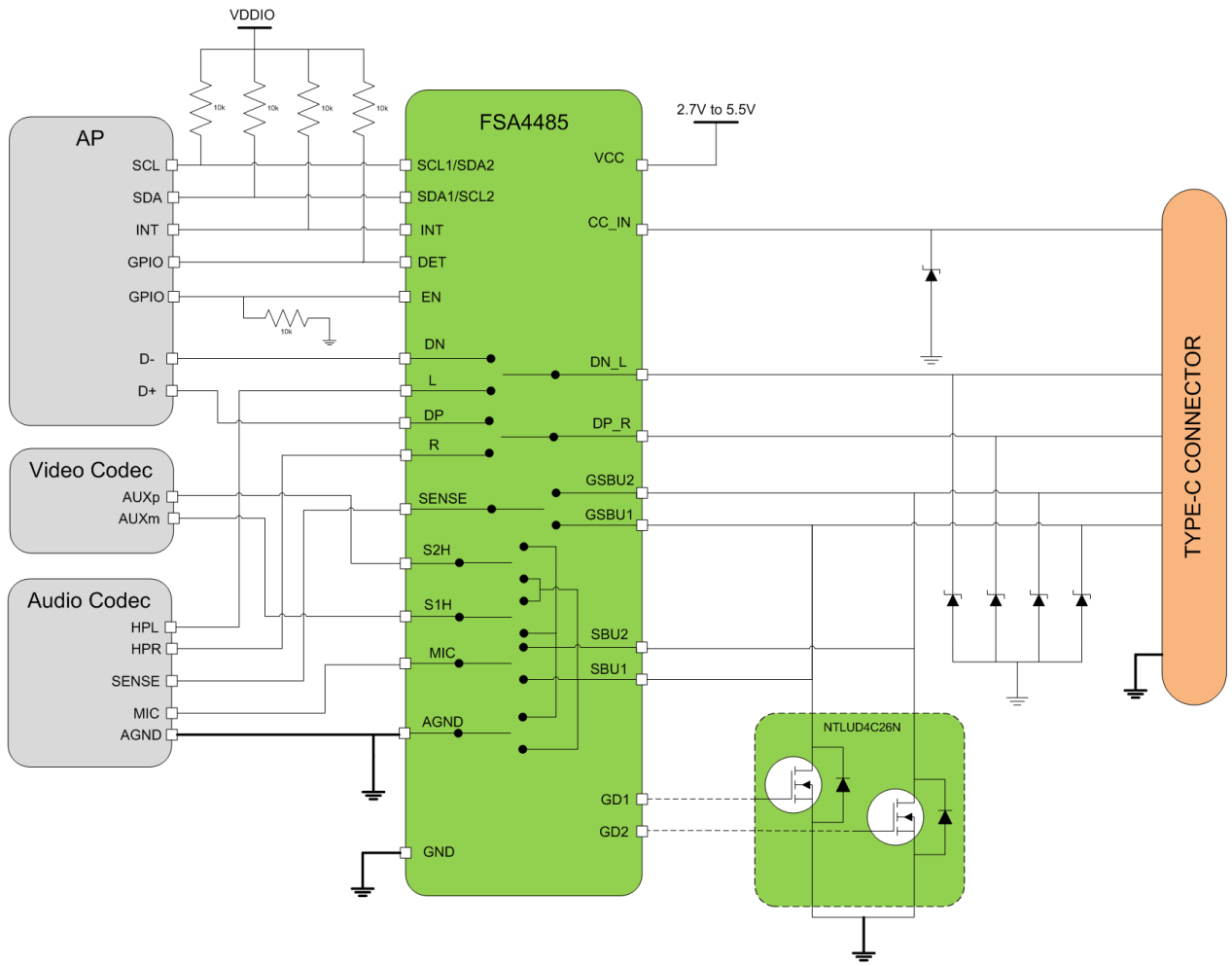


Figure 20. Application Example with Factory Test Mode

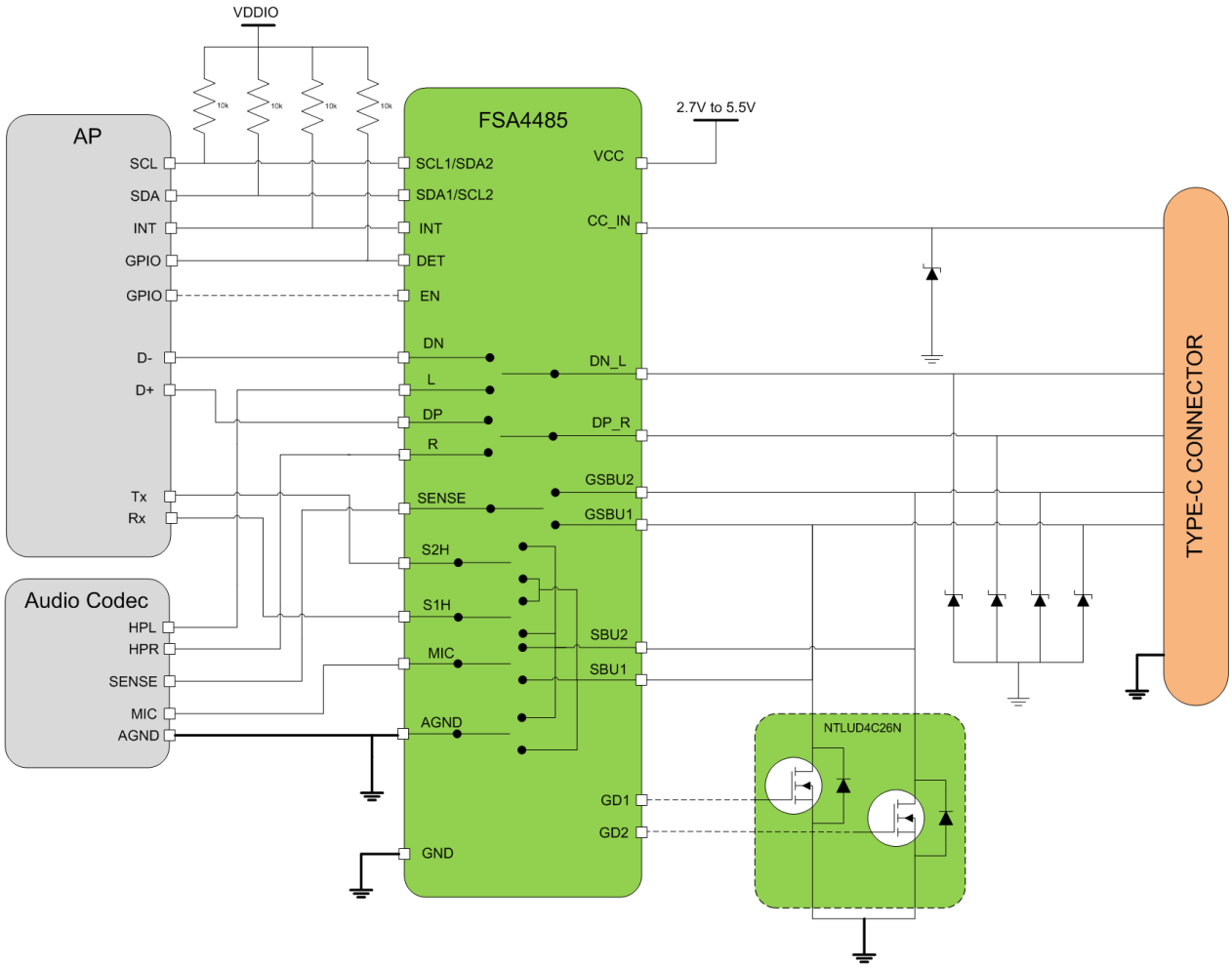


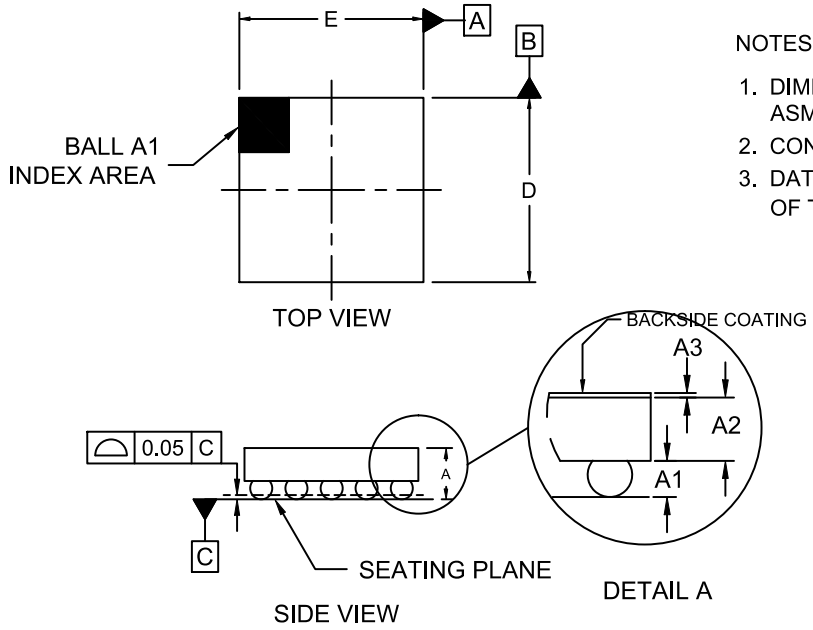
Figure 21. Application Example with Factory Test Mode

ON Semiconductor is licensed by the Philips Corporation to carry the I^2C bus protocol.

FSA4485

PACKAGE DIMENSIONS

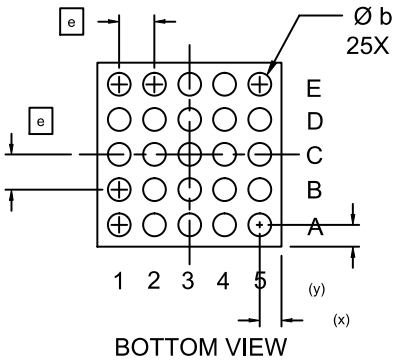
WLCSP25 2.16x2.16x0.574
CASE 567YL
ISSUE O

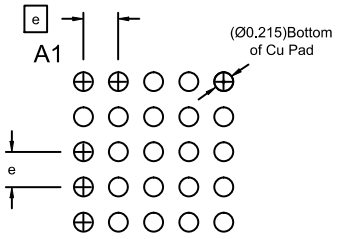


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.536	0.574	0.612
A1	0.176	0.196	0.216
A2	0.338	0.353	0.368
A3	0.022	0.025	0.028
b	0.24	0.26	0.28
D	2.13	2.16	2.19
E	2.13	2.16	2.19
e	0.40 BASIC		
x	0.265	0.280	0.295
y	0.265	0.280	0.295





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