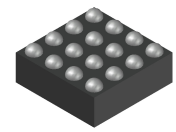
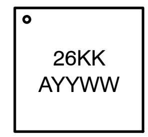
Protection Switch, with OVP/OTP/OCP Function, 24 V, 4.5 A

FPF2266UCX



WLCSP16
CASE 567UX

MARKING DIAGRAM



26	= Device Part Number
KK	= Lot Run Code
A	= Assembly Location
YY	= Year of Production
WW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 18 of this data sheet.

General Description

The FPF2266 features 4.5 A continuous current for USB charging port application, which offers Over−Voltage Protection (OVP), over current protection (OCP), also NTC block to monitor system temperature. It has low On−resistance of typical 15 mohms that can operate over an input voltage range of 3.6 V to 24 V and up to 28 V absolute maximum.

The FPF2266 also provides an open−drain output (BATT_SHDN) for system battery disconnect and a bi−directional interface (ALERT/KILL) with SOC, MCU, or other external source (provides temperature fault condition to external source or it can receive system KILL signal to turn OFF internal switch and disconnect battery).

The FPF2266 is available in a 4x4 balls 0.4 mm pitch WLCSP package which can operate over −40°C to +125°C junction temperature range.

Features

- 24 V/4.5 A OTP/OVP/OCP Power Switch
- 2 Channels NTC Detection for System Thermal Monitoring
- Input voltage Range:
  - V_{IN}: 3.6 V ~ 24 V
  - V_{BAT}: 2.7 V − 5.5 V
- Ultra−Low On−Resistance
  - Typical 15 mΩ
- Up to 28 V Input/Output Voltage AMR
- Active Discharge
- Integrated Inrush Control
- Thermal Shutdown
- BO Detection to Check VIN Drop Off, Battery Disconnect Control Pin BATT_SHDN, Bi−direction I/O ALERT/KILL Pins
- WLCSP 4x4 Balls 0.4 mm Pitch Package
- This is a Pb−Free Device

Applications

- Tablet

APPLICATION DIAGRAM

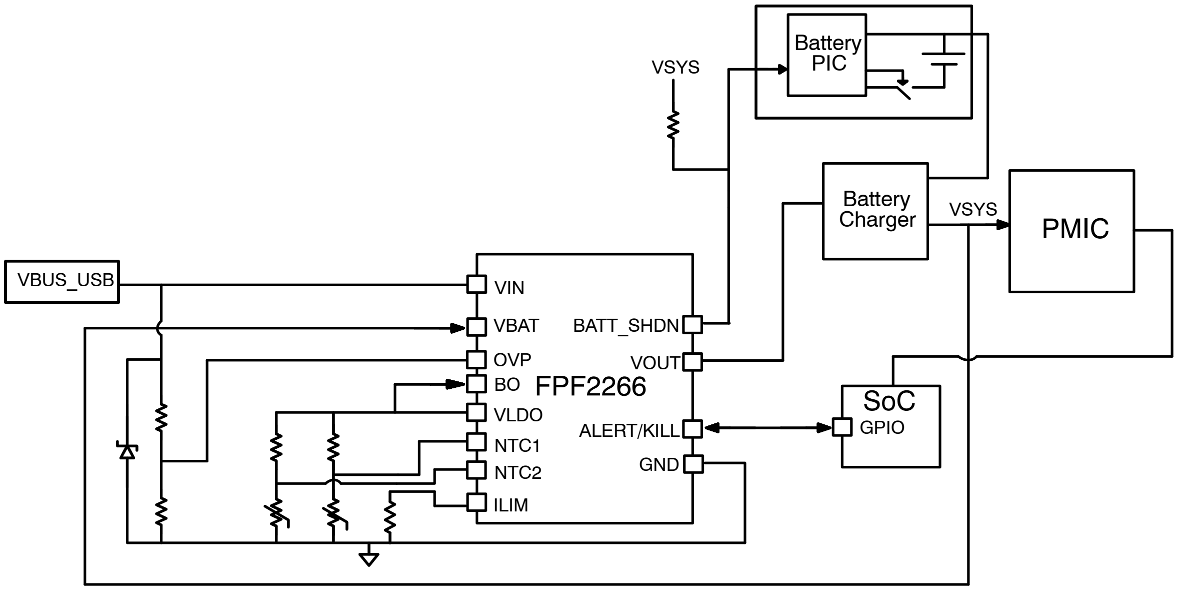


Figure 1. Typical Application 1

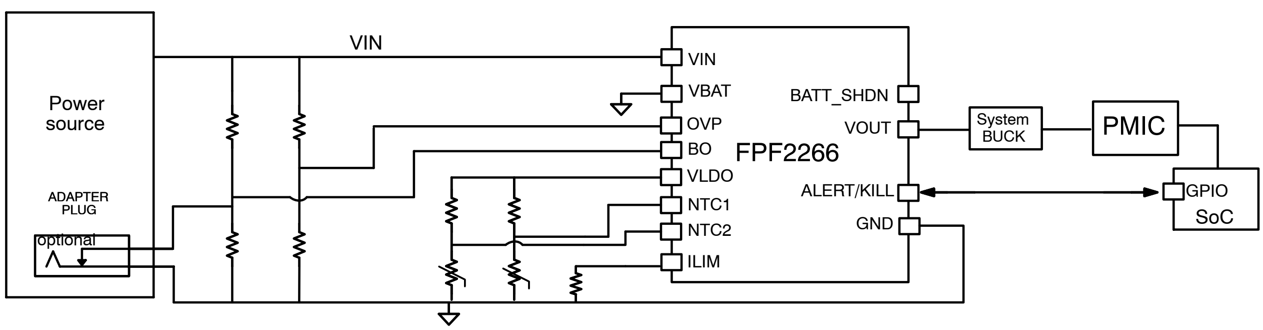


Figure 2. Typical Application 2

BLOCK DIAGRAM

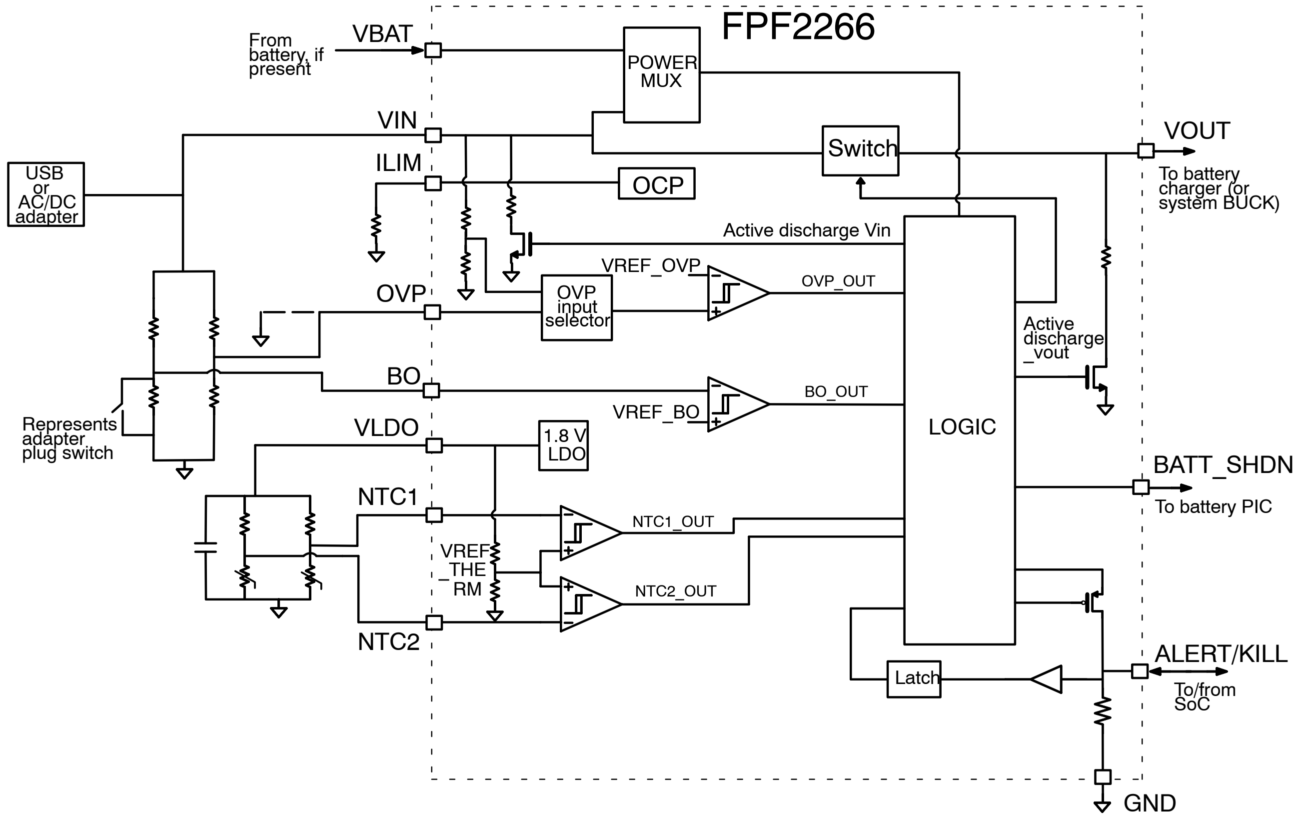


Figure 3. Functional Block Diagram

PIN CONFIGURATION

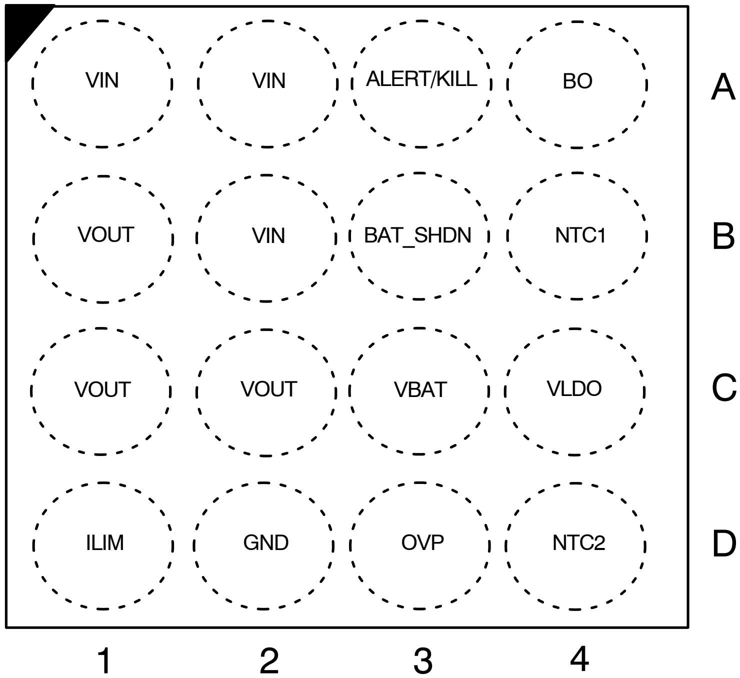


Figure 4. Pin Configuration (Top View)

PIN DESCRIPTION

Pin #	Pin Name	Type	Description
D3	OVP	Input	Input to over−voltage protection circuit, when this pin tied to ground, internal OVP threshold is used.
B4	NTC1	Input	Input to NTC sensing comparator 1
D4	NTC2	Input	Input to NTC sensing comparator 2
C4	VLDO	Output (power)	Voltage rail for NTC thermistor sensing
A3	ALERT/KILL	Input/Output	ALERT (output): provides temp fault status to SoC KILL (input): kill signal from SoC to shut off system power
B3	BATT_SHDN	Output	Open−drain output to disconnect battery pack from charger
A1/A2/B2	VIN	Input (power)	Dedicated power to protection IC. Input to internal switch.
A4	BO	Input	Input to brownout detection
D2	GND		IC ground
B1/C1/C2	VOUT	Output (power)	Output of internal switch
C3	VBAT	Input (power)	Input from battery
D1	ILIM	Input	Pin to set OCP limit threshold using an external resistor, once tie it to GND, then OCP limitation will be removed.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{IN}	VIN to GND & VIN to VOUT = GND or Float		−0.3	28	V
V_{OUT}	VOUT to GND & VOUT to VIN = GND or Float		−0.3	28	V
VIO/VBAT	OVP, ALERT/KILL, BATT_SHDN, BO, OVP, NTC1/2, VBAT to GND		−0.3	6	V
$I_{IN\_VIN\_VOUT}$	Continuous VIN to VOUT Current		–	5	A
T_{PD}	Total Power Dissipation at T_A = 25°C		–	1	W
T_{STG}	Storage Junction Temperature		−65	+150	°C
T_J	Junction Temperature		–	+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)		–	+260	°C
Θ_{JA}	Thermal Resistance, Junction−to−Ambient (2S2P.1in. (Note 1) pad of 2 oz. Copper)		–	100	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI/ESDA/JEDEC JS−001	2	–	kV
		Charged Device Model, JESD22−C101	1	–	
	IEC61000−4−2 System Level	Air Discharge at VIN and VOUT (Note 2)	15	–	
		Contact Discharge at VIN and VOUT (Note 2)	8	–	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Measured using 2S2P JEDEC std. PCB.
2. External TVS is required to guarantee.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}/V_{OUT}	VIN/VOUT Operating Voltage	3.6	–	24	V
V_{IO}	ALERT/KILL, BATT_SHDN, OVP, BO, ILIM	0	–	5.5	V
V_{BAT}	VBAT to GND	2.7	–	5.5	V
I_{SW}	DC Switch Current (ISW)	0	4.5	5	A
T_A	Ambient Operating Temperature, T_A	−40	–	85	°C
T_J	Operating Junction Temperature	–	–	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Typical values are V_{IN}/V_{BAT} = 5 V, C_{OUT} = 100 μF and T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage	Validate device functionality across the V_{IN} recommended operating range.	3.6	–	24	V
V_{BAT}	Input Voltage	Validate device functionality across the V_{BAT} recommended operating range.	2.7	–	5.5	V
V_{UVLO_VBAT}	Under−voltage Lockout Threshold	V_{BAT} falling	2.3	–	2.5	V
$V_{UVLO\_HYS\_VBAT}$	Under−voltage Lockout Hysteresis	V_{BAT} rising	–	200		mV
$I_{VIN\_ON\_5V}$	Input Quiescent Current on VIN	V_{IN} = 5 V; V_{BAT} = 0 V, Switch closed, OVP/BO/OCP/ NTC detection enabled, T_A = 25°C	–	240	277	μA
$I_{VIN\_ON\_24V}$	Input Quiescent Current on VIN	V_{IN} = 24 V; V_{BAT} = 0 V, Switch closed, OVP/BO/OCP/NTC detection enabled, T_A = 25°C	–	330	433	μA
I_{VBAT_ON}	Input Quiescent Current on VBAT	V_{IN} = 0 V; V_{BAT} = 5 V; Switch opened, only NTC detection enabled; T_A = 50°C; R_{NTC} + R_{BIAS} = 43.7 kΩ	–	2.8	6.5	μA
$I_{VBAT\_ON\_NTC\_ON}$	Input Quiescent Current on VBAT	V_{IN} = 0 V; V_{BAT} = 5 V; Switch opened, only NTC detection enabled; T_A = 50°C; without NTC resistor	–	39.1	–	μA
$I_{VBAT\_ON\_NTC\_OFF}$	Input Quiescent Current on VBAT	V_{IN} = 0 V; V_{BAT} = 5 V; Switch opened, only NTC detection enabled; T_A = 50°C; without NTC resistor	–	2.1	–	μA
R_{ON_5V}	On Resistance	V_{IN} = 5.0 V; I_{OUT} = 500 mA; T_A = 25°C	–	15	20	mΩ
R_{ON_24V}	On Resistance	V_{IN} = 24 V; I_{OUT} = 500 mA; T_A = 25°C	–	15	20	mΩ
$R_{ON\_5V\_3.5A}$	On Resistance	V_{IN} = 5.0 V; I_{OUT} = 3500 mA; T_A = 25°C (Note 3)	–	15	20	mΩ
$R_{ON\_24V\_3.5A}$	On Resistance	V_{IN} = 24 V; I_{OUT} = 3500 mA; T_A = 25°C (Note 3)	–	15	20	mΩ
I_INRUSH		V_{IN} = 5 V; C_{OUT} = 1 mF	–	177	–	mA
		V_{IN} = 20 V; C_{OUT} = 1 mF	–	229	–	mA
R_{DISC_VOUT}	Resistance for Active Discharge	V_{BAT} = 5 V, switch is off, T_A = 25°C	–	300	400	Ω
R_{DISC_VIN}	Resistance for Active Discharge	V_{BAT} = 5 V, switch is off, T_A = 25°C	–	10	–	kΩ

OVER TEMPERATURE (OT) PROTECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{LDO}	VLDO Output Voltage	V_{BAT} = 2.7 V, I_{load} > 2 mA	1.71	1.8	1.89	V
I_{LDO}	VLDO Output Current	V_{BAT} = 2.7 V, V_{LDO} > 1.71 V	2	–	–	mA
C_VLDO	VLDO Output Capacitance		0.047	–	0.47	μF
R_{DIS_VLDO}	Discharge Resistance when LDO is Disable	V_{BAT} = 3.6 V, V_{LDO} = 1.8 V	–	7.3	–	kΩ
OTP_TRIP_SYS	Thermal Trip System	With R_{bias} = 10.5k 1%, and NCP15WF104F03RC NTC resistor (Note 3)	–3	–	3	°C
OTP_TRIP_IC	Thermal Trip IC		–0.8	–	0.8	°C

ELECTRICAL CHARACTERISTICS (continued)
(Typical values are V_{IN}/V_{BAT} = 5 V, C_{OUT} = 100 μF and T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OVER TEMPERATURE (OT) PROTECTION						
T_HYS	Thermal Hysteresis	With R_{bias} = 10.5k 1%, and NCP15WF104F03RC NTC resistor (Note x3)	23	24	25	°C
αTRIP VREF_THERM		Internal reference for comparators used for temperature sensing.	0.495	0.500	0.505	V/V
VREF_THERM _REL	Internal reference for comparators used for temperature sensing release		0.702	0.709	0.716	V/V
OVER VOLTAGE (OV) PROTECTION						
V_{IH_OVP}	Voltage Increasing, Logic High	High	0.3	–	–	V
V_{IL_OVP}	Voltage Decreasing, Logic Low	Low	–	–	0.15	V
V_{offset_ovp}	Offset of OVP Comparator (Note x3)		–	0.0418	–	V
V_{REF_OVP}	Internal Reference Voltage of OVP Detection		–	1.19	–	V
V_{OVP_Trip}	Over−voltage Protection Threshold Accuracy	V_{IN} rising	−5	–	5	%
V_{OVP_hysis}	Over−voltage Protection Hysteresis	V_{IN} falling	–	100	–	mV
$V_{ovp\_internal}$	Internal Fixed OVP Threshold (V_{IN} Rising)	V_{IN} rising	5.8	6	6.2	V
$V_{hysis\_internal}$	Over−voltage Protection Hysteresis	V_{IN} falling	–	200	–	mV
T_{ovp}	Over−voltage Protection Response Time	R_L = 10, C_L = 0 F, time from V_{IN} > V_{OVLO} to V_{OUT} start to drop down	–	100	–	ns
$T_{ovp\_rec\_}$	Over−voltage Protection Recover time	R_L = 10, C_L = 0 F, time from V_{IN} < V_{OVLO} to V_{OUT} = 0.1 × V_{IN}	–	30	–	ms
C_OVP	Capacitance on OVP Pin	OVP = 0.1 V, Freq. = 1 MHz , T_A = 25°C (Note 3)	–	5	6	pF
$V_{OUT\_LEAKAGE\_OVP}$	V_{OUT} Leakage Resistance when OVP Event Triggered	V_{OUT} = 0~20 V, T_A = −40 ~ 85°C	125	–	–	kΩ
OVER CURRENT PROTECTION (OCP)						
I_{LIMIT}	Current Limit	V_{IN} = 5 V, R_{SET} = TBD Ω (50 mA), V_{OUT} = V_{IN} − 1 V	–	50	–	mA
		V_{IN} = 5 V, R_{SET} = TBD Ω (150 mA), V_{OUT} = V_{IN} − 1 V	–	150	–	mA
		V_{IN} = 5 V, R_{SET} = TBD Ω (250 mA), V_{OUT} = V_{IN} − 1 V	–	250	–	mA
		500−1000 mA, T_A = 25°C (Note 3)	−10	–	10	%
		1000−1750 mA, T_A = 25°C (Note 3)	−8	–	8	%
		1750−2500 mA, T_A = 25°C (Note 3)	−7	–	7	%
		2500−4500 mA, T_A = 25°C (Note 3)	−6	–	6	%
T_{ocp_deb}	OCP Debounce Time	Moderate Over−Current Condition, $I_{OUT} \geq I_{LIM}$; $V_{OUT} \leq V_{IN} - 1$	–	100	–	ms
BROWNOUT DETECTION (BO)						
V_{REF_BO}		V_{IN} = 3.6 V−24 V, BO Falling	1.13	1.19	1.25	V
V_{hysis_BO}	BO Detection Hysteresis	BO Rising	–	100	–	mV

ELECTRICAL CHARACTERISTICS (continued)
(Typical values are V_{IN}/V_{BAT} = 5 V, C_{OUT} = 100 μF and T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BROWNOUT DETECTION (BO)						
V_{BO}	Brownout (BO) Trip Point Accuracy	V_{IN} = 3.6 V−24 V	−5	–	5	%
V_{offset_BO}	Offset of Comparator for BO Detection (Note 3)		–	−0.0015	–	V
$T_{d\_bo\_rec}$	Brownout Recovery Delay	V_{IN} = 5 V, from BO rising over V_{hysis_BO} to 10% V_{OUT} rising	–	500	–	ms
THERMAL SHUTDOWN (TSD)						
TSD	Trip Point	Thermal shut down threshold	–	135	–	°C
TSD	Hysteresis	Thermal shut down hysteresis	–	25	–	°C
BASIC OPERATION						
R_{pd}	Pull Down Resistance of BATT_SHDN	V_{IN} = 5.5 V, T_A = −40 to 85°C, I_{FORCE} > 15 mA	–	15	30	Ω
$I_{IN\_BATT\_SHDN}$	BATT_SHDN Output HIGH−Z Leakage Current	BATT_SHDN = 0 to 5.5 V	−1	–	1	μA
$V_{switchover}$	Threshold of Power Switch to VBAT	V_{IN} Falling	–	3	–	V
$V_{hys\_switchover}$	Hysteresis Voltage of Switch over to VBAT	V_{IN} Rising	–	0.6	1.1	V
$V_{OH\_ALERT/KILL}$	Output Logic High Voltage	V_{BAT} = 2.7 V to 5.5 V, Io = −2 mA	1.5	–	1.95	V
$V_{IL\_ALERT/KILL}$	Input Logic Low Voltage	V_{BAT} = 2.7 V to 5.5 V	–	–	0.5	V
$V_{IH\_ALERT/KILL}$	Input Logic High Voltage	V_{BAT} = 2.7 V to 5.5 V	1.3	–	–	V
$R_{pd\_ALERT/KILL}$	Weak Pulldown Resistance	V_{BAT} = 2.7 V to 5.5 V	100	230	350	kΩ
DYNAMIC PARAMETERS						
T_{d_on}	Turn On Delay	V_{IN} = 5 V, R_L = 100 W, C_L = 100 μF, T_A = 25°C, from V_{IN} valid to V_{OUT} start to ramp up	–	20	–	ms
T_{d_alert}	Delay Time between ALERT and BATT_SHDN	From 90% ALERT rising to 90% BATT_SHDN falling	–	500	–	ms
T_{d_kill}	Delay Time between KILL and BATT_SHDN	From 90% KILL rising to 90% BATT_SHDN falling	–	1000	–	ms
T_{rel_deb}	Thermal Release Debounce Time		–	50	–	ms
T_NTC_SAMPLE	NTC Checking Period	(Note 3)	–	2.5	5	s
T_NTC_ON	VLDO On Time		–	5	–	ms
T_NTC_SETTLE	Settle Down Time before ADC Sampling		–	1.6	–	ms
Duty_NTC_DET	Duty Cycle of NTC Detection by T_NTC_ON/T_NTC_SAMPLE	(Note 3)	–	0.2	0.25	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Guaranteed by design. Characterized on the Bench.

Power On/Off

FPF2266 control block can sink power from both VBAT and VIN through internal power mux. Once VIN is valid which means higher than Vswitchover + Vhys_switchover, then 20 ms turn on delay will be started, and if no fault (including OV/OT/BO events) being detected after 20 ms delay, then switch will be closed automatically (OV/OT/BO event was masked during this 20ms delay), and inrush current will be limited to a fixed level to avoid any potential damage. The internal VLDO is powered by power mux.

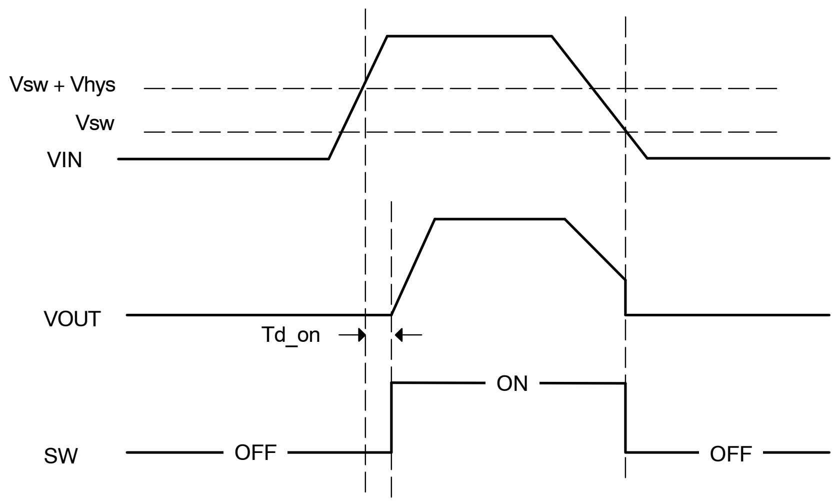


Figure 5. VIN to VOUT Power Up/Down

Brownout Detection

Brownout event is sensed via an external resistor divider connected between VIN and GND and compared with an internal reference (V_{REF_BO}). Brownout trip point is set by selecting resistor ratio with respect to V_{REF_BO}. When a brownout event is detected, internal switch is turned OFF and Auto discharge enabled. After brownout event is removed and discharge disabled (rises above internal hysteresis threshold), there is a delay before internal switch is turned on for recover. The Td_bo_rec will be applied at both normal mode and Vin power up stage.

$$VIN < \left(1 + \frac{R_{BO1}}{R_{BO2}}\right) V_{REF\_BO} \left(trip\right) \qquad \text{(eq. 1)}$$

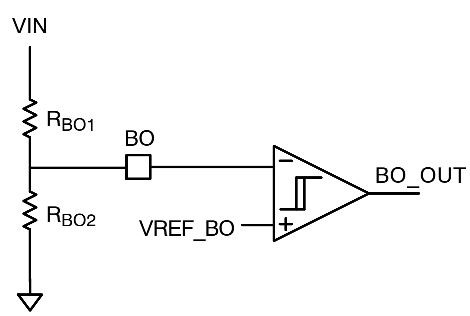


Figure 6. Brownout Detection

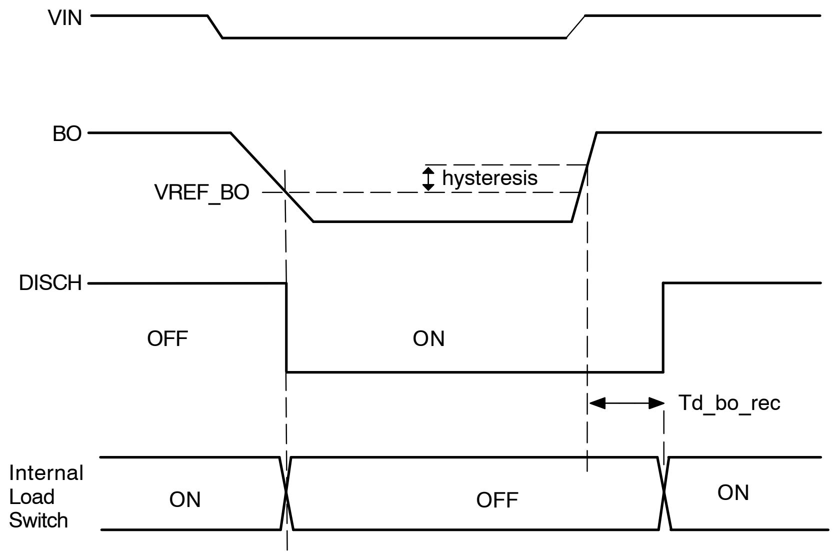


Figure 7. Brownout Detection in Normal Mode

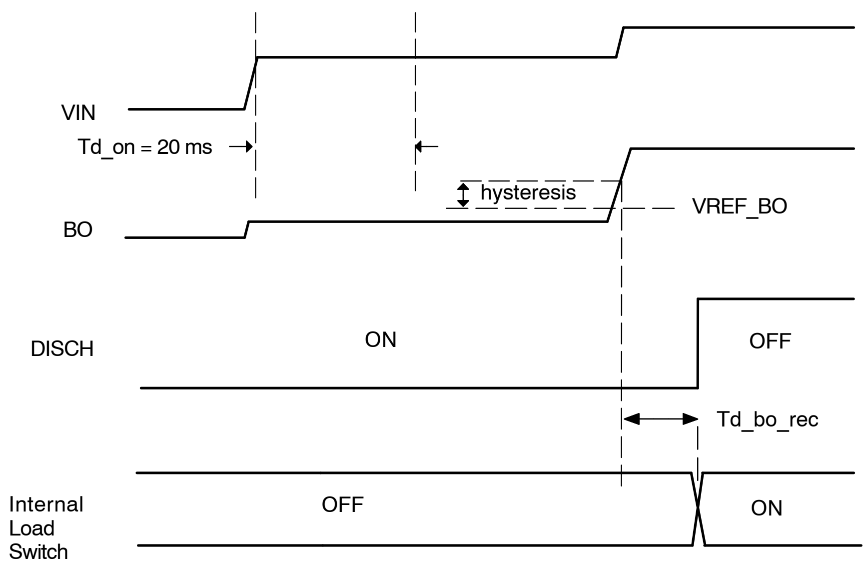


Figure 8. Brownout Detection in VIN Power Up

Active Discharge on VIN/VOUT

Internal resistive discharge path from VOUT/VIN to GND is enabled when internal switch is turned off for all fault conditions except OVP/TSD. Discharge path should be enabled for BO and OT, KILL events. Additional discharge resistance on Vin needs to be enabled as well when discharge on VOUT is enabled. Also enabled when power MUX selects VBAT and VIN < Vhys_switchover (VIN rising).

Power MUX Function

For USB/battery configuration, a power MUX is used to select between 2 inputs: VIN and battery source (VBAT). Priority is given to VIN when it is above a certain threshold (Vswitchover). If VIN is not present or falls below a certain threshold, then priority is given back to VBAT input and Kill latch need to be reset by Vswitchover.

Internal blocks to drive internal switch, support in−rush control, brownout detector, and OVP/OCP function are powered only from VIN. All other features such as over temperature protection and logic are powered from power MUX.

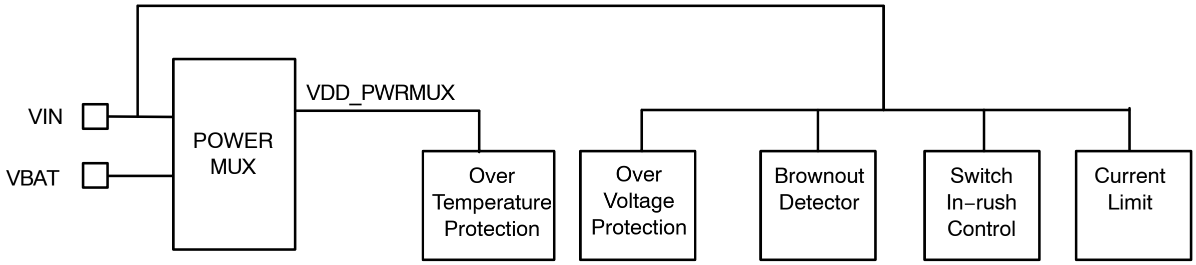


Figure 9. Power Mux Function

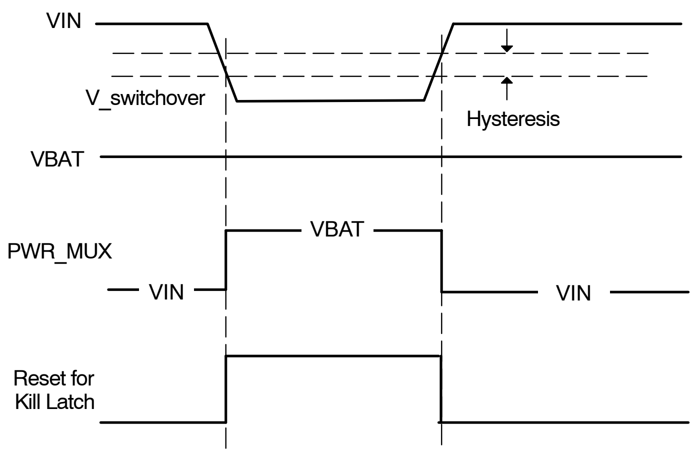


Figure 10. Power Mux Switch Over and Kill Reset

KILL Function

KILL signal is from an external source such as a SOC or MCU. When KILL signal is asserted HIGH by SOC internal switch is turned OFF after some delay.

1. *VIN Applied (VBAT may or may not be applied)*
   a. Condition is latched after some debounce time, internal switch is turned off and BATT_SHDN is pulled low.
   b. Because of latching condition, it requires VIN to be power cycled to reset/clear latch in AC/DC adapter systems. For USB/battery configuration, latch should be cleared after unplugging and re−plugging USB adapter.

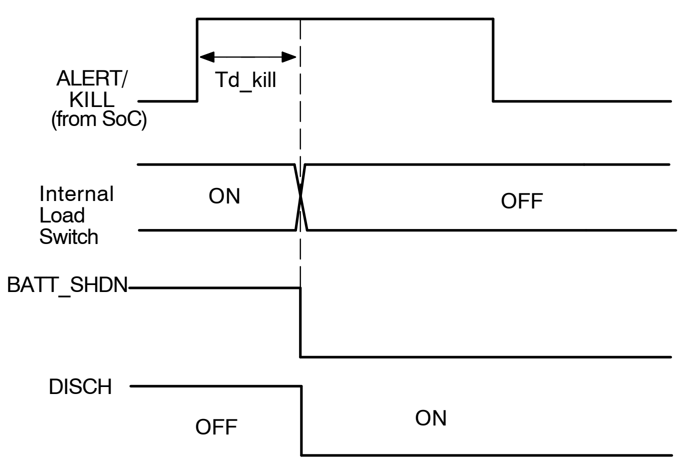


Figure 11. KILL Function Timing Diagram

For Vswitchover behavior with/without Kill latch in detail, please refer to below diagram:

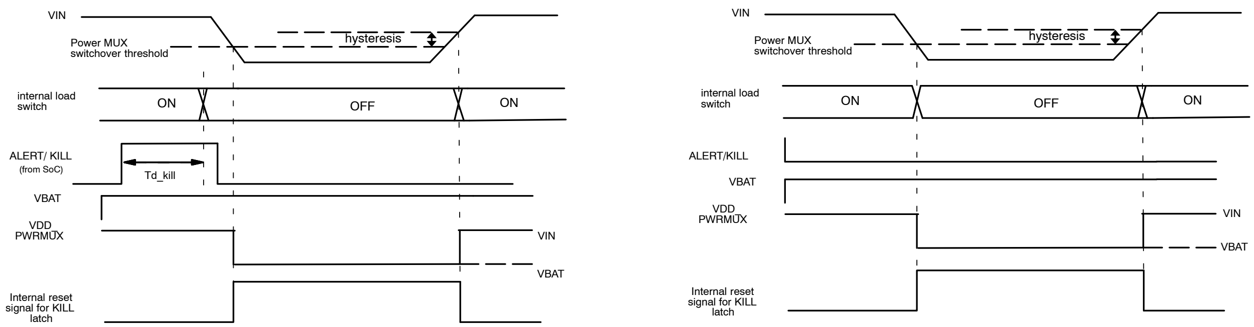


Figure 12. Vswitchover Behavior with/without Kill Latch in Detail

2. *Only VBAT is present*

a. Condition is NOT latched after some debounce time (Td_kill), and after debounce time, internal switch is turned OFF and BATT_SHDN goes LOW.

b. If KILL signal from SOC goes LOW, BATT−SHDN goes HIZ (pulled up by external resistor).

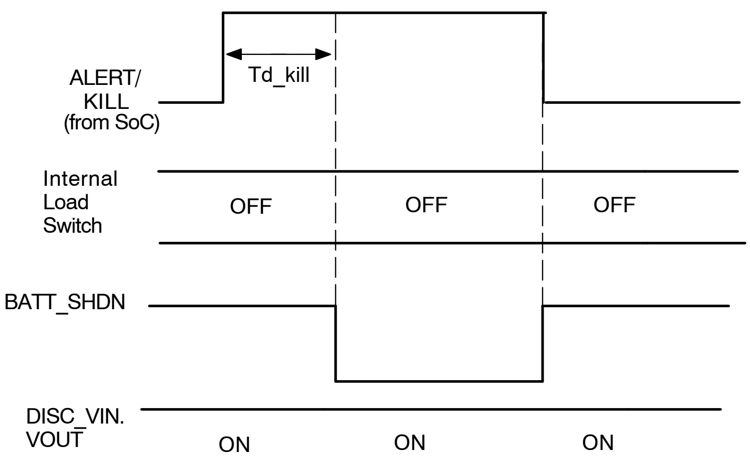


Figure 13. KILL Function Timing Diagram When VBAT is Present

Battery Disconnection (USB/Battery Configuration)

For over temperature condition or KILL signal, BATT_SHDN sends signal to battery PIC to disconnect battery.

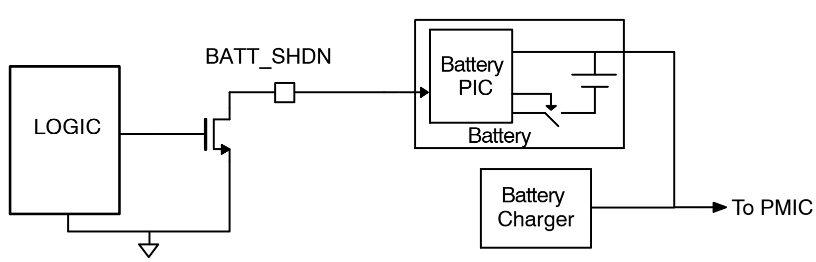


Figure 14. Battery Disconnect Diagram

Over Temperature Protection (OTP)

When an over temperature condition is detected by any of NTC channel, ALERT/KILL is pulled HIGH alerting SOC that a temperature fault condition has occurred. After Td_alert from ALERT/KILL goes HIGH and if over temperature condition is still present, internal switch is turned OFF and BATT_SHDN is pulled LOW. Once temperature fault is no longer present, internal switch shall be turned ON and BATT_SHDN output is goes to High−Z and pulled HIGH by external source with minimal delay. Also, for OT behavior under power up stage, please refer to below diagram.

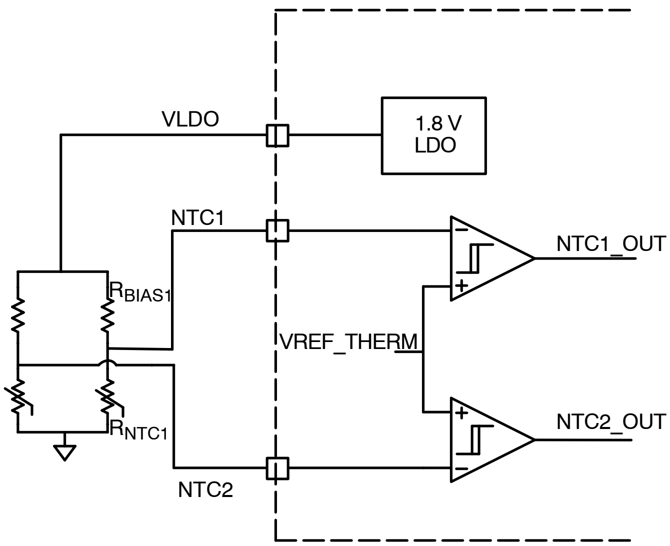


Figure 15. Over Temperature Detection Diagram

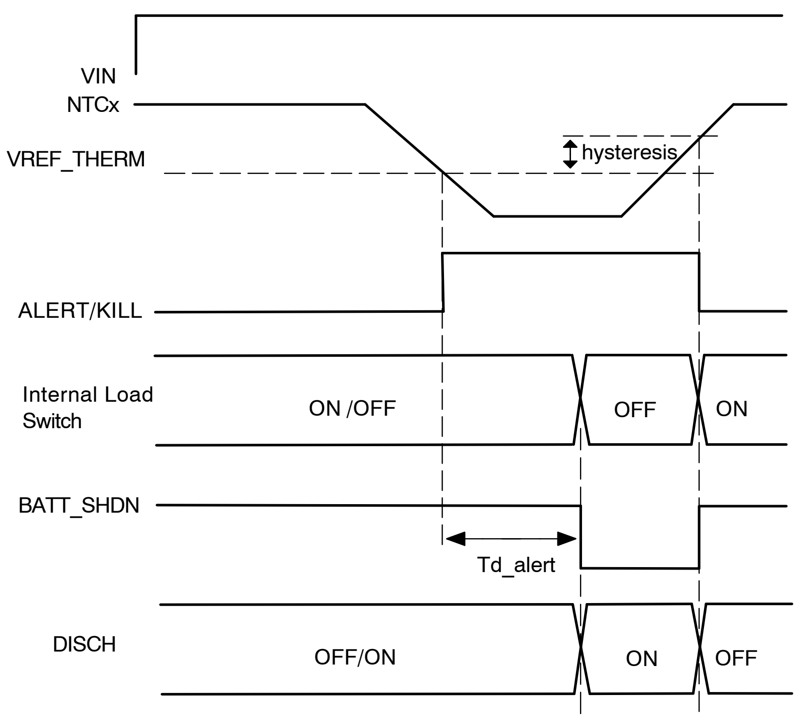


Figure 16. Over Temperature Detection Flow in Normal Case

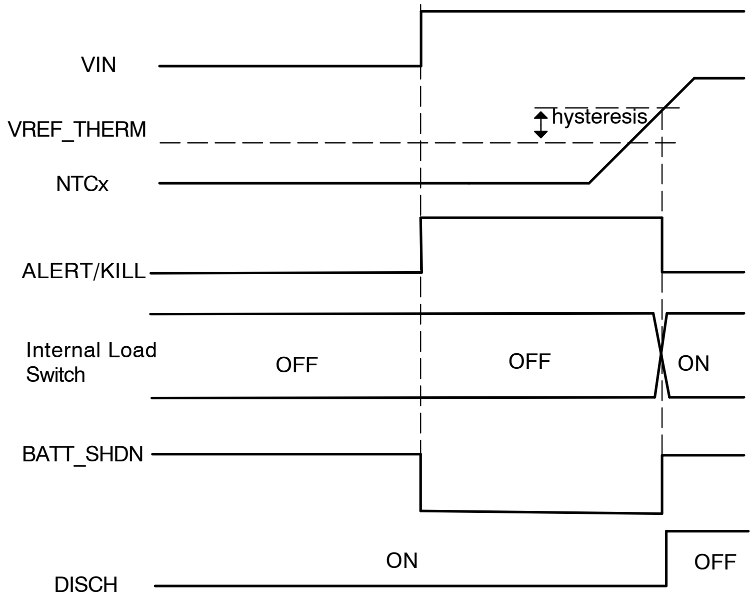


Figure 17. Over Temperature Detection Flow in Power Up Stage

Thermal Shut Down (TSD)

To protect the device from over temperature, the power switch turns OFF immediately when the junction temperature exceeds TSD and no need to enable VIN/VOUT discharge, the device can be only re−enabled with a delay once temperature drop down below threshold.

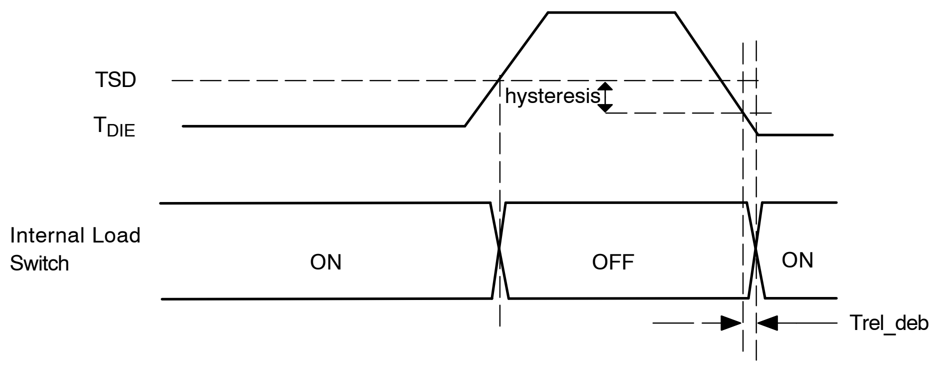


Figure 18. Thermal Shut Down and Timing Diagram

Over−voltage Protection (OVP)

Over−voltage (OV) condition can be sensed via an external resistor divider connected between VIN and GND and compared with an internal reference (VREF_OVP), or via an internally fixed threshold. Internal fixed OV threshold is selected by tying OVP pin to GND. External OV trip point is set by selecting resistor ratio with respect to VREF_OVP. When an OV condition is detected, internal switch is turned OFF in less than 100 ns. After OV condition is removed (falls below internal hysteresis threshold), there is a delay before internal switch is turned ON, VIN/VOUT discharge resistor keep off during OVP event.

$$\mathrm{VIN} > \left(1 + \frac{\mathrm{Rov1}}{\mathrm{Rov2}}\right) V_{REF\_OVP}\,(\mathrm{trip}) \qquad \text{(eq. 2)}$$

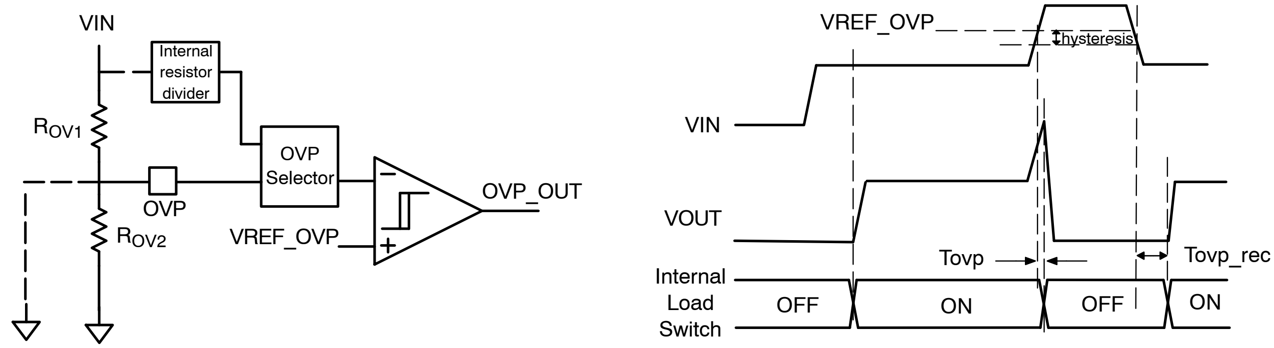


Figure 19. Over Voltage Detection and Timing Diagram

NTC Detection

For achieving low standby current, once power mux switch to VBAT, FPF2266 will start to toggle VLDO output which used as power source of NTC and bias resistor ON and OFF with a fixed period T_NTC_SAMPLE = 2.5 s and T_NTC_ON = 5 ms on time , also internal comparator will sample the voltage level of Pin NTC1/2 after T_NTC_SETTLE = 1.6 ms settle timer. If power mux was powered by VIN, then no need to toggle VLDO.

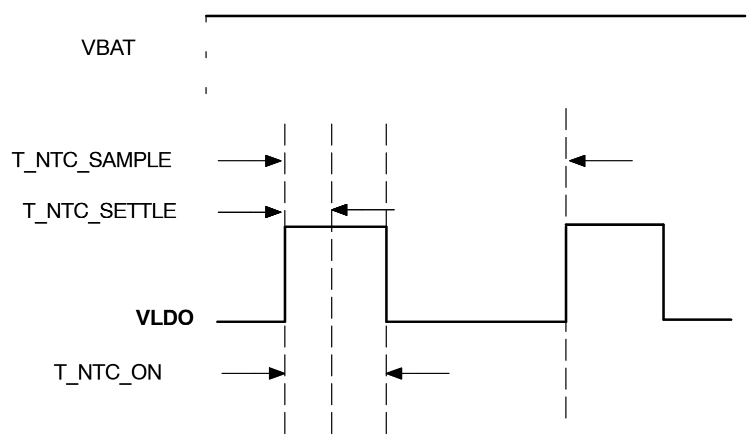


Figure 20. NTC Sample Timing (VBAT Only)

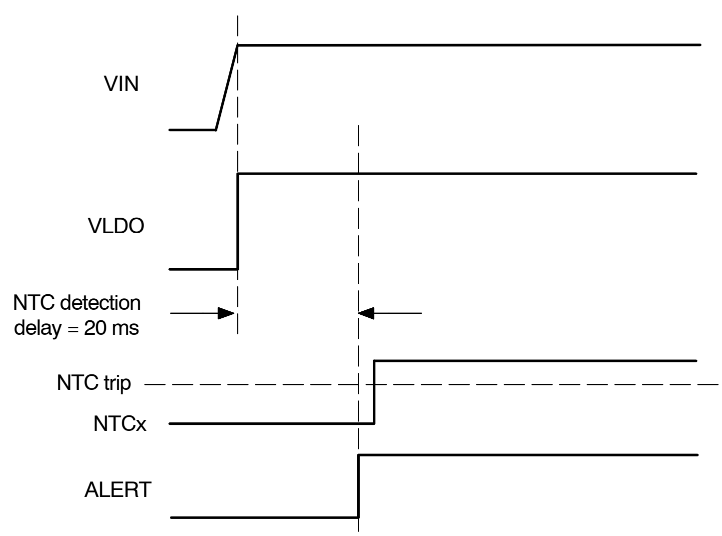


Figure 21. NTC Sample Timing (VIN Power Up)

Over Current Protection (OCP)

The current limit ensures that the current through the switch does not exceed the maximum setting value, while not limit the minimum value. The current at which the part's limit is adjustable through the selection of the external resistor connected to the ILIM pin. The device acts as a constant−current source when the load draws more than the maximum value set by the device until thermal shutdown occurs. The device recovers if the die temperature drops below the threshold temperature. The current limit is set with an external resistor connected between the ILIM and GND pins. The resistor is selected using the formula:

$$\text{Typ ILIM} = \frac{576}{\text{RSET}} \qquad \text{(eq. 3)}$$

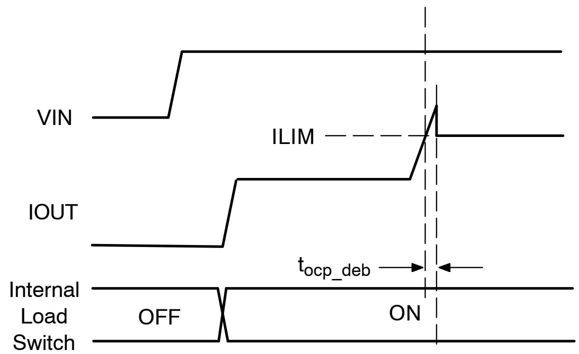


Figure 22. OCP Timing

Soft−Start and Inrush Current Limitation

FPF2266 integrates inrush current control block to control the inrush current might happens during VOUT start up with up to 2.2 mF COUT, also FPF2266 will clamp the inrush current to around the 175 mA typical during soft start active period, until the thermal shutdown happens and switch open, once the temperature back to normal condition, then switch will be enabled again.

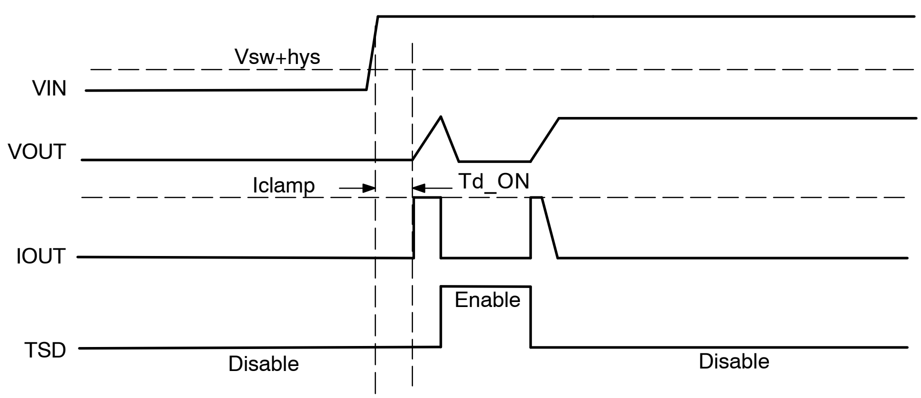


Figure 23. Inrush Control

Hard Short Protection

FPF2266 implements hard short protection feature in case of any short event happens after switch closed. Once the VOUT drops below 2.35 V at this condition, the hard short protection will be active and internal switch will be opened in less than 5 μs. It will release and take another try to close back switch after 30 ms delay, if the short still present, then inrush protection will be triggered, and inrush current will be limited to a safe level.

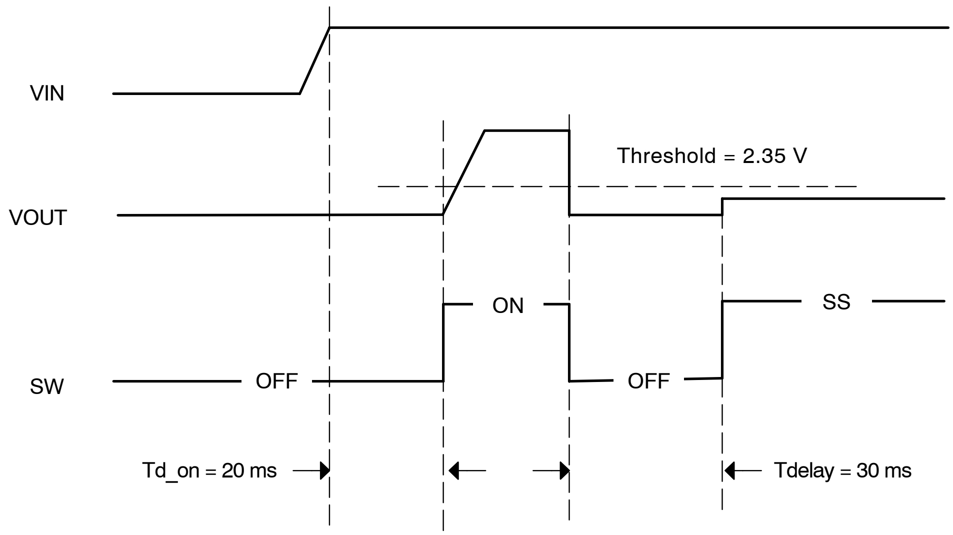


Figure 24. Hard Short Protection Flow

Working Flow

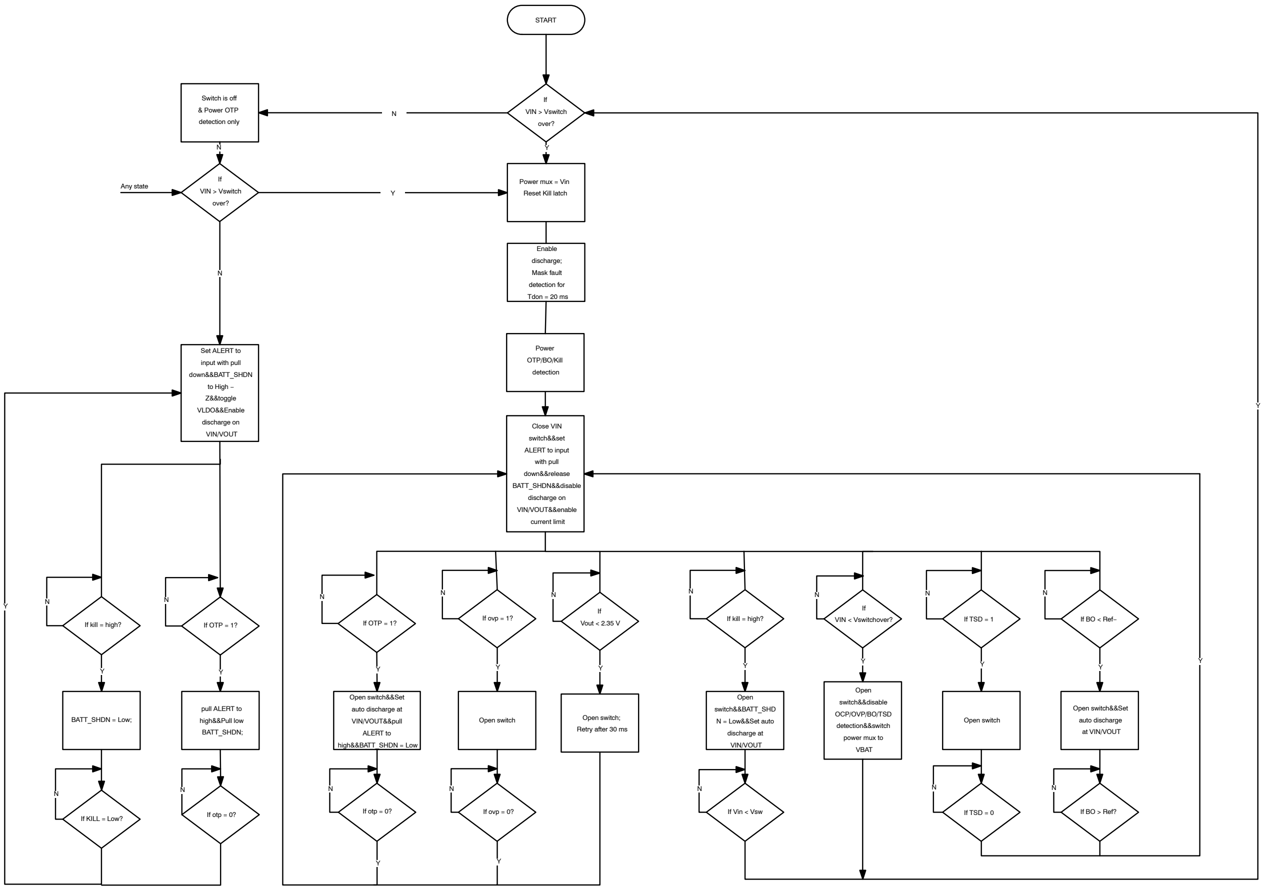


Figure 25. Working Flow

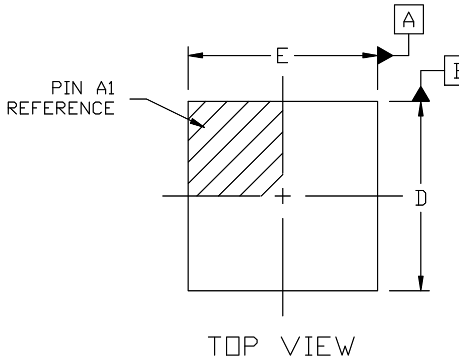
ORDERING INFORMATION

Part Number	Marking	Operating Temperature Range	Package	Shipping†
FPF2266UCX	26	−40°C to +85°C	WLCSP16 (4×4 − 16 Balls) (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

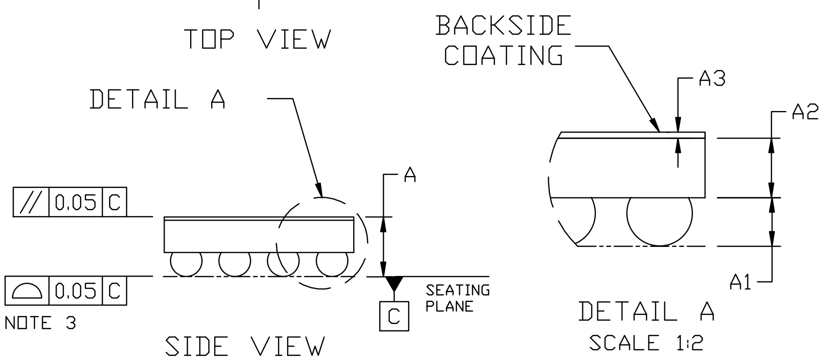
PACKAGE DIMENSIONS

WLCSP16 1.560x1.560x0.470
CASE 567UX
ISSUE O

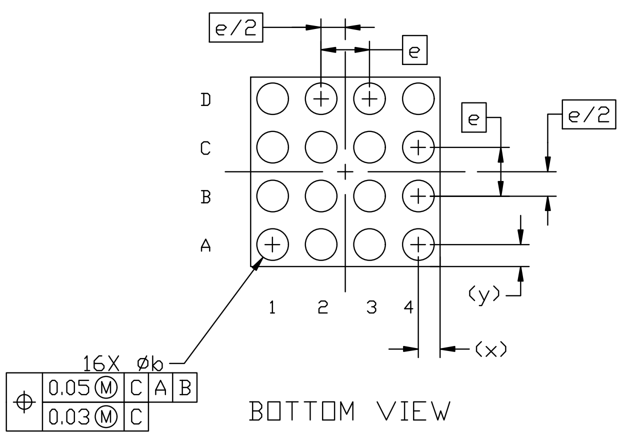


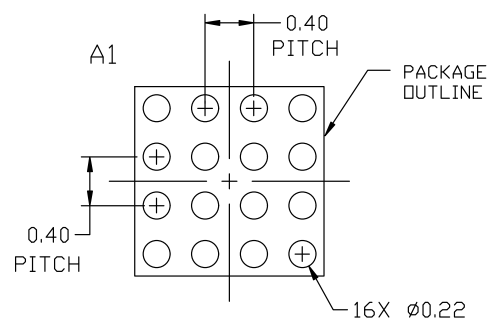
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.452	0.490	0.528
A1	0.178	0.198	0.218
A2	0.252	0.267	0.282
A3	0.022	0.025	0.028
b	0.240	0.260	0.280
D	1.530	1.560	1.590
E	1.530	1.560	1.590
e	0.400 BSC		
x	0.180 BSC		
y	0.180 BSC		





RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

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