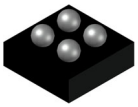
IntelliMAX™ Ultra-Small, Slew-Rate-Controlled Load Switch

FPF1204



WLCSP4 0.76x0.76x0.525
CASE 567ZH

MARKING DIAGRAM

XX	= Specific Device Code
&K	= 2−Digits Lot Run Traceability Code
&2	= 2−Digit Date Code
&.	= Pin One Dot
&Z	= Assembly Pant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

Description

The FPF1204 is an ultra−small integrated IntelliMAX load switch with integrated P−channel switch and analog control features. Integrated slew−rate control prevents inrush current and the resulting excessive voltage drop on the power rail. The input voltage range operates from 1.2 V to 5.5 V to provide power−disconnect capability for post−regulated power rails in portable and consumer products. The low shut−off current allows power designs to meet standby and off−power drain specifications.

The FPF1204 is controlled by a logic input (ON pin) compatible with standard CMOS GPIO circuitry found on Field Programmable Gate Array (FPGA) embedded processors. The FPF1204 is available in 0.76 mm x 0.76 mm 4−bump WLCSP.

Features

- 1.2 V to 5.5 V Input Voltage Operating Range
- Typical R_{ON}:
  - 45 mΩ at V_{IN} = 5.5 V
  - 55 mΩ at V_{IN} = 3.3 V
  - 90 mΩ at V_{IN} = 1.8 V
  - 185 mΩ at V_{IN} = 1.2 V
- Slew Rate Control with t_R:
  - 100 μs
- Output Discharge Function
- Low <1.5 μA Quiescent Current
- ESD Protected: Above 7 kV HBM, 2 kV CDM
- GPIO / CMOS−Compatible Enable Circuitry
- 4−Bump, WLCSP 0.76 mm x 0.76 mm, 0.4 mm Pitch
- These are Pb−Free Devices

Applications

- Mobile Devices and Smart Phones
- Portable Media Devices
- Tablet PCs
- Advanced Notebook, UMPC, MID
- Portable Medical Devices
- GPS and Navigation Equipment

APPLICATION DIAGRAM

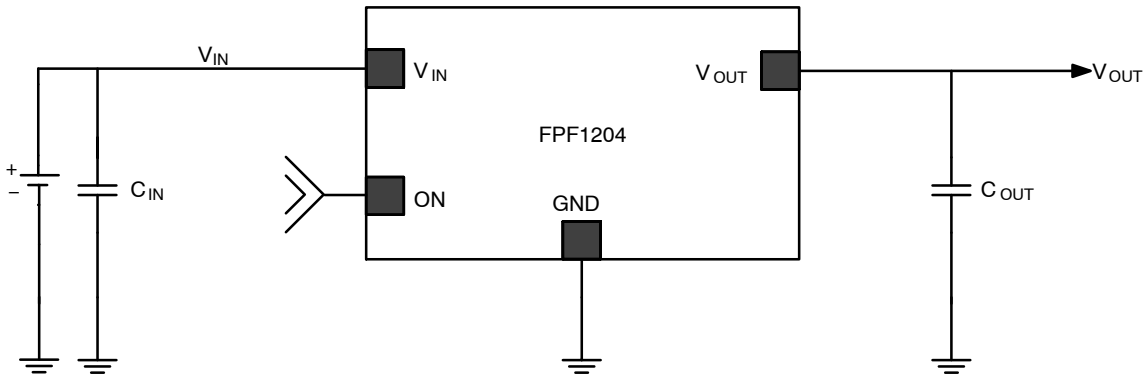


Figure 1. Typical Application

FUNCTIONAL BLOCK DIAGRAM

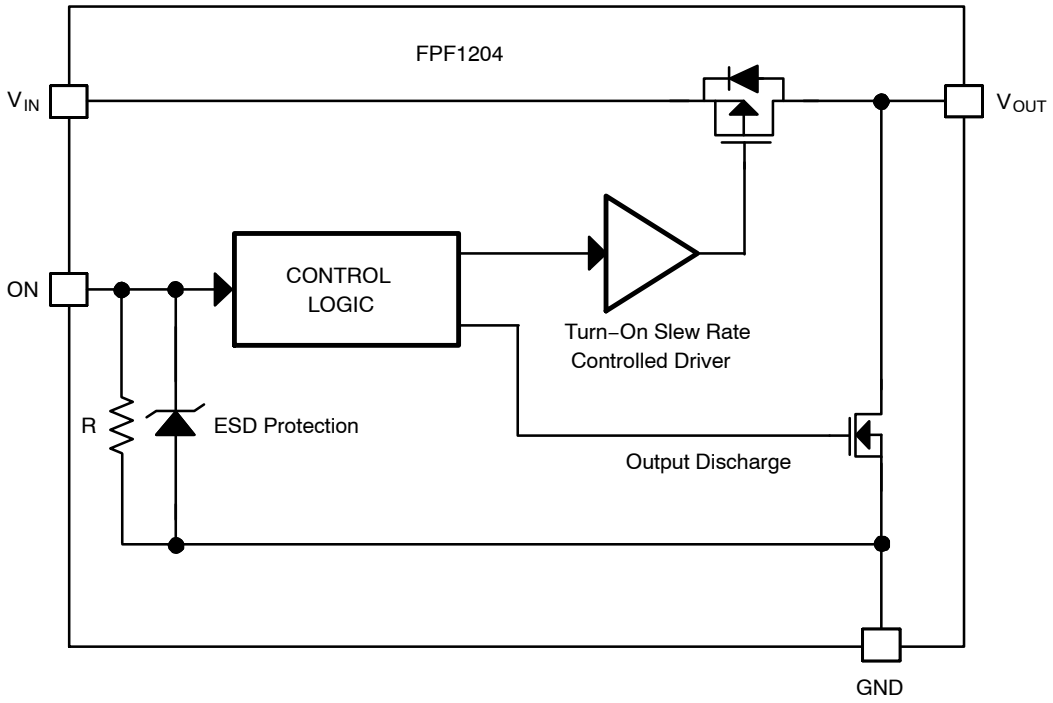


Figure 2. Functional Block Diagram

PIN CONFIGURATIONS

Figure 3. WLCSP Bumps Facing Down (Top View)

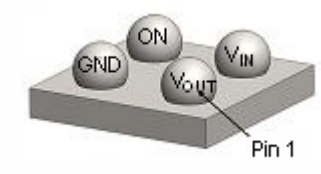


Figure 4. WLCSP Bumps Facing Up (Bottom View)

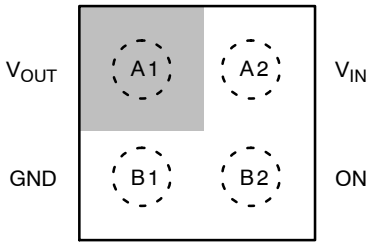


Figure 5. Pin Assignments (Top View)

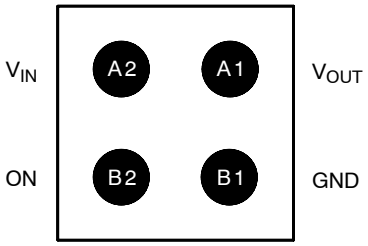


Figure 6. Pin Assignments (Bottom View)

PIN DEFINITONS

Pin No.	Name	Description
A1	V_{OUT}	Switch output
A2	V_{IN}	Supply input: input to the power switch
B1	GND	Ground
B2	ON	ON/OFF Control, active HIGH

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{IN}	V_{IN}, V_{OUT}, V_{ON} to GND		−0.3	6.0	V
I_{SW}	Maximum Continuous Switch Current at Ambient Operating Temperature		–	2.2	A
P_D	Power Dissipation at T_A = 25°C		–	1.0	W
T_{STG}	Storage Temperature Range		−65	+150	°C
Θ_{JA}	Thermal Resistance, Junction−to−Ambient	1S2P with One Thermal Via (Note 1)	–	110	°C/W
		1S2P without Thermal Via (Note 2)	–	95	
ESD	Electrostatic Discharge Capability (Note 1, 2)	Human Body Model, JESD22−A114	7	–	kV
		Charged Device Model, JESD22−C101	2	–	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured using 2S2P JEDEC std. PCB.
2. Measured using 2S2P JEDEC PCB COLD PLATE Method.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	1.2	5.5	V
T_A	Ambient Operating Temperature	−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V_{IN} = 1.2 V to 5.5 V and T_A = −40 to +85°C. Typical values are at V_{IN} = 3.3 V and T_A = 25°C.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
BASIC OPERATION						
V_{IN}	Supply Voltage		1.2	–	5.5	V
$I_{Q(OFF)}$	Off Supply Current	V_{ON} = GND, V_{OUT} = Open, V_{IN} = 5.5 V	–	0.1	1.0	μA
I_{SD}	Shutdown Current	V_{ON} = GND, V_{OUT} = GND	–	0.1	1.0	μA
I_Q	Quiescent Current	I_{OUT} = 0 mA, V_{ON} = V_{IN}, = 5.5 V	–	0.1	1.5	μA
R_{ON}	On Resistance	V_{IN} = 5.5 V, I_{OUT} = 200 mA, T_A = 25°C	–	45	55 (Note 3)	mΩ
		V_{IN} = 3.3 V, I_{OUT} = 200 mA, T_A = 25°C	–	55	65 (Note 3)	
		V_{IN} = 1.8 V, I_{OUT} = 200 mA, T_A = 25°C	–	90	100 (Note 3)	
		V_{IN} = 1.2 V, I_{OUT} = 200 mA, T_A = 25°C	–	185	220 (Note 3)	
R_{PD}	Output Discharge $R_{PULL\ DOWN}$	V_{IN} = 3.3 V, V_{ON} = OFF, I_{FORCE} = 20 mA, T_A = 25°C	–	65	75	Ω
V_{IH}	On Input Logic HIGH Voltage	V_{IN} = 1.2 V to 5.5 V	1.15	–	–	V
V_{IL}	On Input Logic LOW Voltage	V_{IN} = 1.2 V to 5.5 V	–	–	0.65	V
R_{ON_PD}	Pull−Down Resistance at ON Pin	V_{IN} = 1.2 V to 5.5 V	–	8.3	–	MΩ
I_{ON}	On Input Leakage	V_{ON} = V_{IN} or GND	–	–	1	μA
DYNAMIC CHARACTERISTICS						
t_{DON}	Turn−On Delay (Note 4)	V_{IN} = 3.3 V, R_L = 10 Ω, C_L = 0.1 μF, T_A = 25°C	–	70	–	μs
t_R	V_{OUT} Rise Time (Note 4)		–	100	–	
t_{ON}	Turn−On Time (Note 6)		–	170	–	
t_{DOFF}	Turn−Off Delay (Note 4, 5)	V_{IN} = 3.3 V, R_L = 10 Ω, C_L = 0.1 μF, T_A = 25°C	–	4.0	–	μs
t_F	V_{OUT} Fall Time (Note 4, 5)		–	2.5	–	
t_{OFF}	Turn−Off Time (Note 5, 7)		–	6.5	–	
t_{DOFF}	Turn−Off Delay (Note 4, 5)	V_{IN} = 3.3 V, R_L = 500 Ω, C_L = 0.1 μF, T_A = 25°C	–	6.0	–	μs
t_F	V_{OUT} Fall Time (Note 4, 5)		–	11	–	
t_{OFF}	Turn−Off Time (Note 5, 7)		–	17	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. This parameter is guaranteed by design and characterization; not production tested.
4. t_{DON} / t_{DOFF} / t_R / t_F are defined in Figure 21.
5. Output discharge enabled during off−state.
6. t_{ON} = t_R + t_{DON}
7. t_{OFF} = t_F + t_{DOFF}

TYPICAL PERFORMANCE CHARACTERISTICS

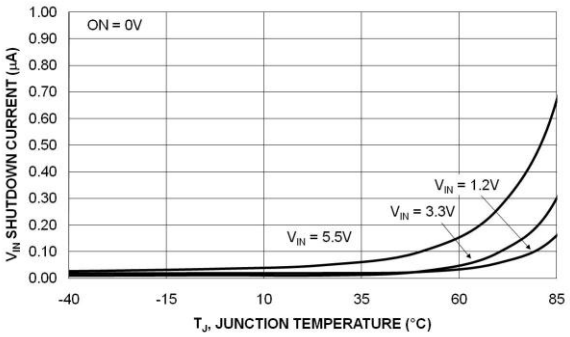


Figure 7. Shutdown Current vs. Temperature

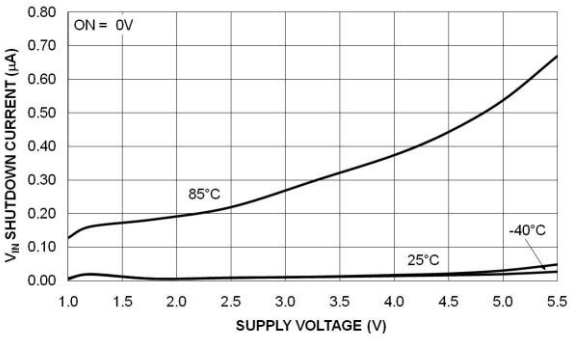


Figure 8. Shutdown Current vs. Supply Voltage

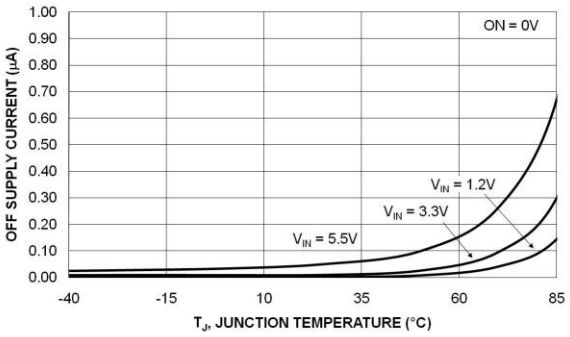


Figure 9. Off Supply Current vs. Temperature (V_{OUT} Floating)

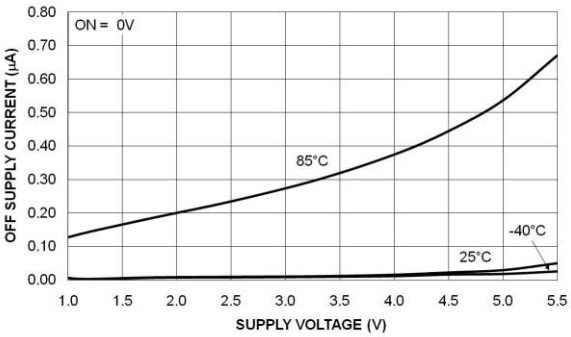


Figure 10. Off Supply Current vs. Supply Voltage (V_{OUT} Floating)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

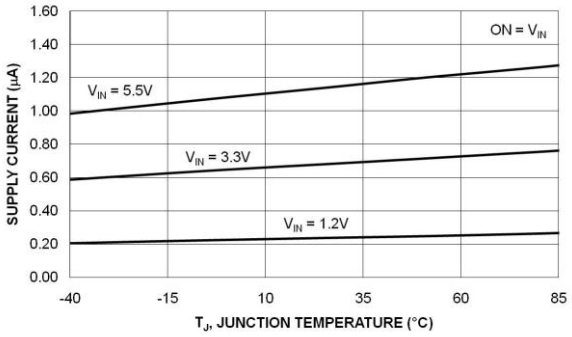


Figure 11. Quiescent Current vs. Temperature

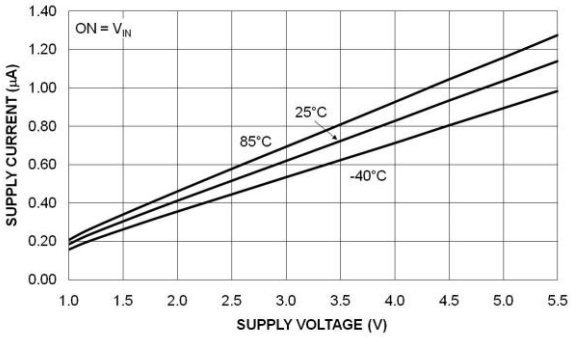


Figure 12. Quiescent Current vs. Supply Voltage

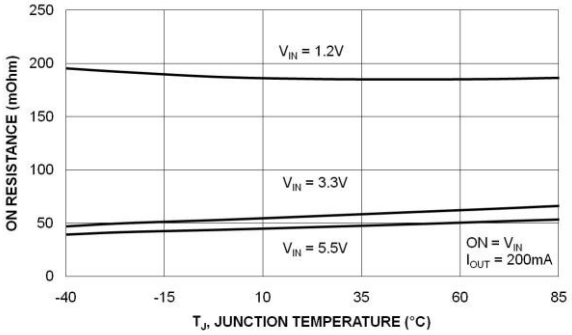


Figure 13. R_{ON} vs. Temperature

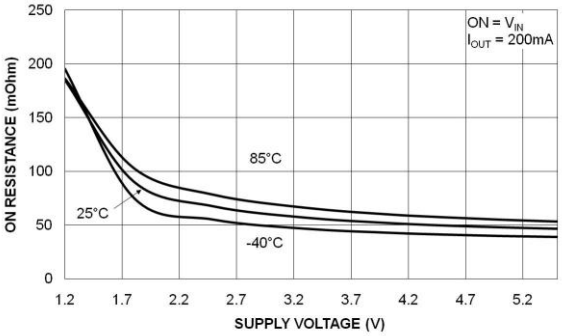


Figure 14. R_{ON} vs. Supply Voltage

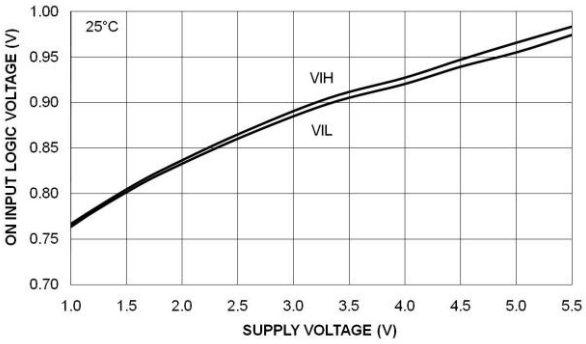


Figure 15. ON Pin Threshold vs. V_{IN}

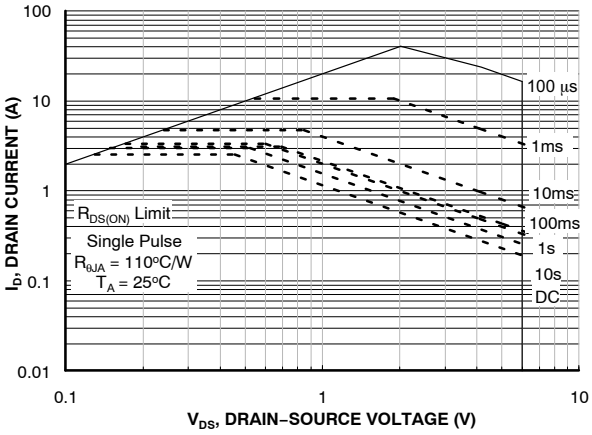


Figure 16. Drain Current vs. Drain−Source Voltage Safe Operating Area

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

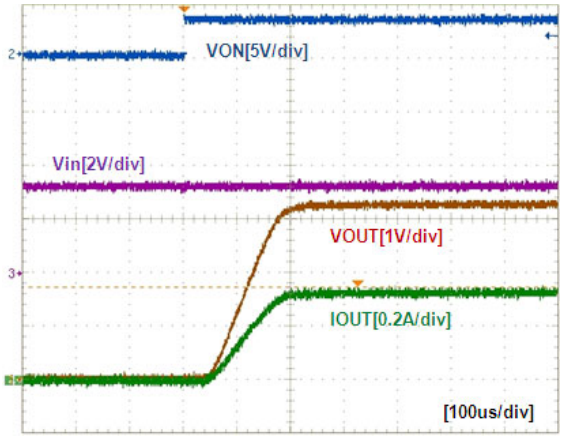


Figure 17. Turn−On Response
(V_{IN} = 3.3 V, C_{IN} = 1 μF, C_{OUT} = 0.1 μF, R_L = 10 Ω)

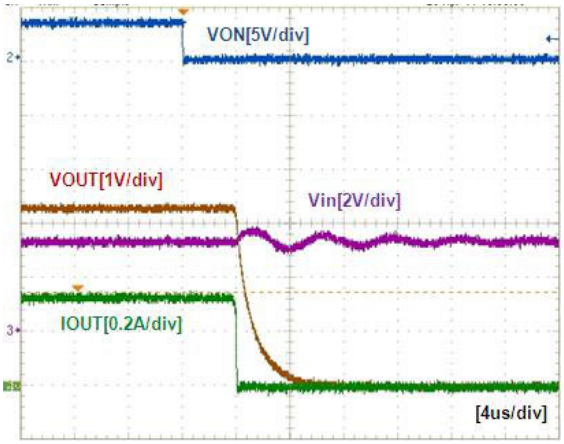


Figure 18. Turn−Off Response (V_{IN} = 3.3 V, C_{IN} = 1 μF, C_{OUT} = 0.1 μF, R_L = 10 Ω)

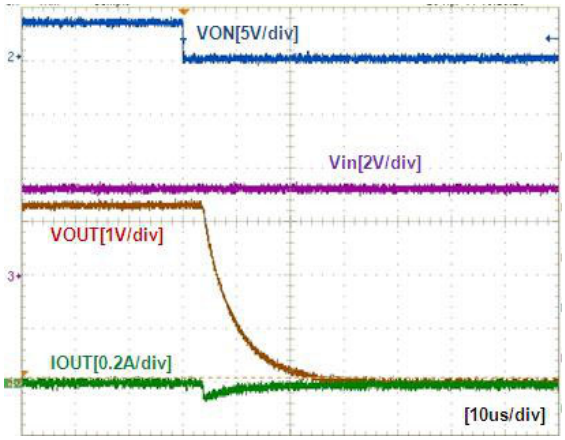


Figure 19. Turn−Off Response (V_{IN} = 3.3 V, C_{IN} = 1 μF, C_{OUT} = 0.1 μF, R_L = 500 Ω)

OPERATION AND APPLICATION DESCRIPTION

The FPF1204 is a low−R_{ON} P−channel load switch with controlled turn−on. The core of each device is a 55 mΩ P−channel MOSFET and controller capable of functioning over a wide input operating range of 1.2 to 5.5 V.

The FPF1204 contains a 65 Ω on−chip load resistor for quick output discharge when the switch is turned off.

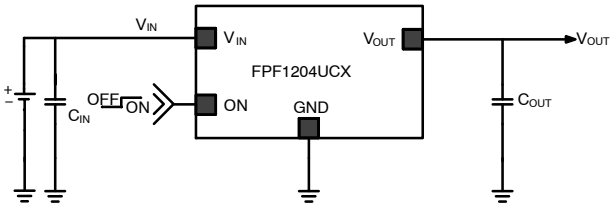


Figure 20. Typical Application

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short−circuit, a capacitor must be placed between the V_{IN} and GND pins. A 1 μF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher−value C_{IN} can be used to reduce the voltage drop in higher−current applications.

Output Capacitor

A 0.1 μF capacitor, C_{OUT}, should be placed between the V_{OUT} and GND pins. This capacitor prevents parasitic board inductance from forcing V_{OUT} below GND when the switch is on. C_{IN} greater than C_{OUT} is highly recommended. C_{OUT} greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}.

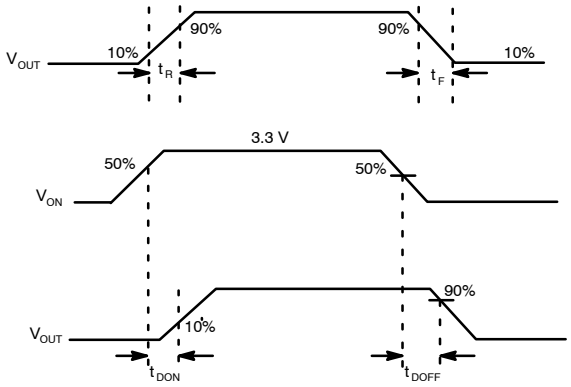


Figure 21. Timing Diagram

Board Layout

For best performance, traces should be as short as possible. To be most effective, input and output capacitors should be placed close to the device to minimize the effect of parasitic trace inductance on normal and short−circuit operation. Using wide traces or large copper planes for all pins (VIN, VOUT, ON, and GND) minimizes the parasitic electrical effects and the case−ambient thermal impedance. However, the VOUT pin should not connect directly to the battery source due to the discharge mechanism of the load switch.

ORDERING INFORMATION

Part Number	Top Mark	Switch (Typical) at 3.3V_{IN}	Output Discharge	ON Pin Activity	t_R	Package	Shipping†
FPF1204UCX	QM	55 mΩ	65 Ω	Active HIGH	100 μs	4−Bump, Wafer−Level Chip−Scale Package (WLCSP), 0.76 mm x 0.76 mm, 0.4 mm Pitch	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

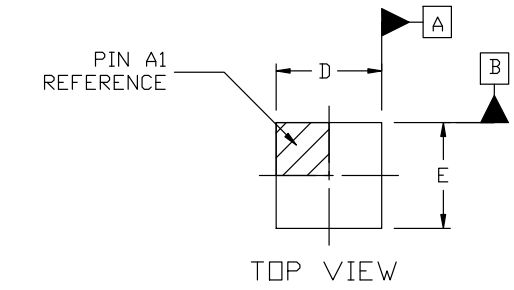
The table below pertains to the Packaging information on the following page.

PRODUCT DIMENSIONS

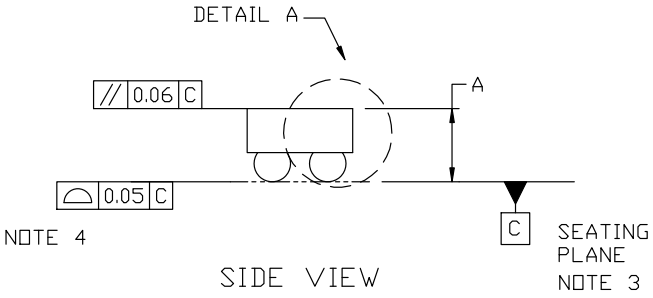
D	E	X	Y
760 μm ±30 μm	760 μm ±30 μm	0.180 mm ±0.018 μm	0.180 mm ±0.018 μm

PACKAGE DIMENSIONS

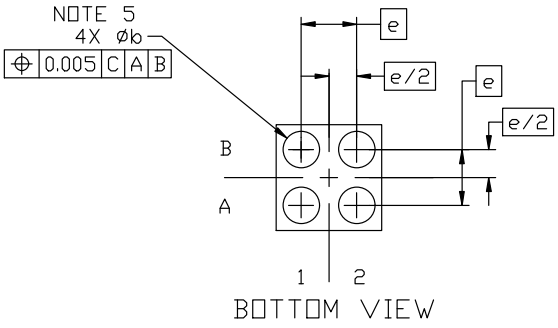
WLCSP4 0.76x0.76x0.525, 0.4P
CASE 567ZH
ISSUE O



TOP VIEW



SIDE VIEW

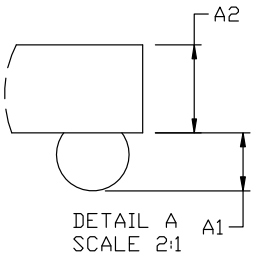


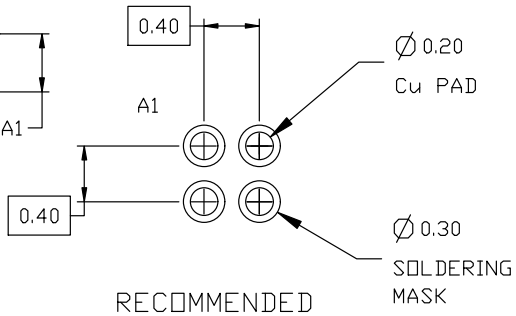
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.486	0.525	0.564
A1	0.187	0.208	0.229
A2	0.299	0.317	0.335
b	0.240	0.260	0.280
D	0.755	0.760	0.765
E	0.755	0.760	0.765
e	0.400 BSC		





RECOMMENDED
MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales