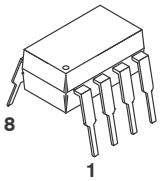
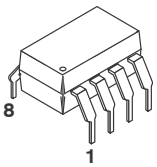
2V, Fully Differential Optical Coupled Isolation Amplifier

FOD7840



PDIP8 9.655x6.6, 2.54P
CASE 646CQ



PDIP8 GW
CASE 709AF

Description

The FOD7840x family is an optically coupled isolation amplifier. It consists of a gallium aluminum arsenide (GaAlAs) light emitting diode and a highly accurate sigma-delta A/D converter on the input side, and a precise D/A converter with differential output on the output side. This optocoupler is used for current sensing in motor drives or general-purpose current sensing and monitoring. The FOD7840x series offers various gain tolerances: FOD7840A (±1% gain tolerance) and the FOD7840B (±3% gain tolerance) and FOD7840 (±5% gain tolerance).

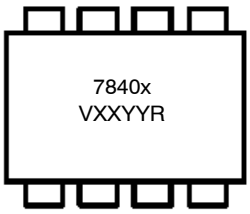
Features

- Advanced Sigma-Delta (Σ-Δ) A/D Converter Technology
- Fully Differential Circuit Topology
- 100 kHz Bandwidth
- −0.3 mV Input Offset Voltage
- 0.0005 V/V/°C Gain drift vs. Temperature
- 0.02% Non-Linearity (NL200 = 0.35% Max)
- 15 kV/μs minimum Common Mode Rejection (CMR) at VCM = 1000 V
- MSL Level 1
- Safety and Regulatory Approvals
  - UL/cUL1577, 3.75 kV_{RMS} for 1 Minute
  - DIN EN/IEC 60747-5-5 VIORM=891 Vpeak

Typical Applications

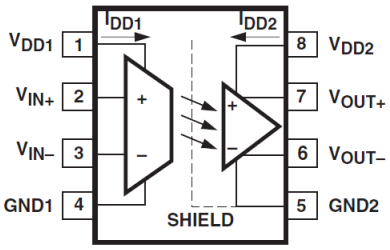
- General Purpose Current Sensing and Monitoring
- General Purpose Analog Signal Isolation
- Motor Phase and Rail Current Sensing
- Industrial Fieldbus Communications
- Switched Mode Power Supply Signal Isolation
- Inverter Current Sensing

MARKING DIAGRAM



7840	= Device Number
x	= Gain rank, A, B or none.
V	= DIN_EN/IEC60747-5-5 Option (only appears on component ordered with this option)
XX	= Two Digit Year Code
YY	= Two Digit Work Week
R	= Assembly Package Code
S	= Surface Mount Device
D	= Through−Hole Device

FUNCTIONAL BLOCK DIAGRAM



NOTE: 0.1 μF bypass capacitor must be connected between pins 1 and 4, and between pins 5 and 8.

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Table 1. SAFETY AND INSULATION RATINGS

As per DIN EN/IEC 60747-17, this digital isolator is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings must be ensured by means of protective circuits.

Symbol	Parameter		Min	Typ	Max	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	< 150 V_{RMS}	–	I–IV	–	
		< 300 V_{RMS}	–	I–IV	–	
		< 450 V_{RMS}	–	I–III	–	
CTI	Climatic Classification		–	55/115/21	–	
	Pollution Degree (DIN VDE 0110/39)		–	2	–	
	Comparative Tracking Index		175	–	–	
V_{PR}	Input-to-Output Test Voltage, Method b, $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC		2306	–	–	V_{peak}
	Input-to-Output Test Voltage, Method a, $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test with t_m = 10 s, Partial Discharge < 5 pC		1968	–	–	V_{peak}
V_{IORM}	Highest Allowable Over Voltage (Transient Overvoltage, t_{ini} = 60 sec)		1230	–	–	V_{peak}
V_{IOTM}	Highest Allowable Over Voltage		6000	–	–	V_{peak}
E_{CR}	External Creepage		8.0	–	–	mm
E_{CL}	External Clearance		7.4	–	–	mm
DTI	Distance Through Insulation (Insulation Thickness)		0.4	–	–	mm
T_{Case}	Safety Limit Values – Maximum Values in Failure; Case Temperature		175	–	–	°C
$P_{S,INPUT}$	Safety Limit Values – Maximum Values in Failure; Input Power		400	–	–	mW
$P_{S,OUTPUT}$	Safety Limit Values – Maximum Values in Failure; Output Power		600	–	–	mW
R_{IO}	Insulation Resistance at TS, V_{IO} = 500 V		10^9	–	–	Ω
V_{ISO}	Maximum Withstanding Insulation Voltage		5000	–	–	V

Table 2. PIN DEFINITION

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Input Side, Relative to GND_1
2	V_{IN+}	Positive Input
3	V_{IN-}	Negative Input (normally connected to GND_1)
4	GND_1	Input Side Ground
5	GND_2	Output Side Ground
6	V_{OUT-}	Negative Output
7	V_{OUT+}	Positive Output
8	V_{DD2}	Supply Voltage for Output Side, Relative to GND_2

Table 3. ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise specified)

Symbol	Parameter	Min	Max	Unit
T_{STG}	Storage Temperature	−55	125	°C
T_{OPR}	Operating Temperature	−40	100	°C
T_J	Junction Temperature	−40	125	°C
T_{SOL}	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260		°C
V_{DD1}, V_{DD2}	Supply Voltage	0	5.5	V
V_{IN+}, V_{IN-}	Steady State Input Voltage	−2	V_{DD1}+0.5	V
V_{IN+}, V_{IN-}	2 sec Transient Voltage	−6	V_{DD1}+0.5	V
V_{OUT+}, V_{OUT-}	Output Voltage	−0.5	V_{DD2}+0.5	mA
P_I	Input Power Dissipation		70	mW
P_O	Output Power Dissipation		60	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. RECOMMENDED OPERATING RANGES

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Operating Temperature	−40	+85	°C
V_{DD1} V_{DD2}	Supply Voltage (Notes 1, 2)	4.5	5.5	V
V_{IN+}, V_{IN-}	Input Voltage (accurate and linear)	−200	200	mV
V_{IN+}, V_{IN-}	Input Voltage (functional)	−2	2	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. During power up or down, ensure that both the input and output supply voltages reach the proper recommended operating voltages to avoid any momentary instability at the output state.
2. For reliable operation at recommended operating conditions, VDD supply pins require at least a pair of external bypass capacitors, placed within 1 cm from VDD pins 1 and 8 and GND pins 4 and 5. Recommended value is 0.1 μF.

Table 5. ISOLATION CHARACTERISTICS

Apply over all recommended conditions. All typical values are measured at T_A = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ISO}	Input-Output Isolation Voltage	T_A = 25 °C, Relative Humidity < 50%, t = 1.0 minute, $I_{I-O} \leq$ 10 μA, 50 Hz (Notes 3, 4)	5000	–	–	V_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V DC (Note 3)	–	10^{12}	–	
C_{ISO}	Isolation Capacitance	Frequency = 1.0 MHz (Note 3)	–	0.9	–	pF

3. Device is considered a two-terminal device: pins 1 to 4 are shorted together and pins 5 to 9 are shorted together.
4. 5,000 V_{RMS} for 1-minute duration is equivalent to 6,000 V_{RMS} for 1-second duration.

Table 6. DC ELECTRICAL CHARACTERISTICS

Apply over all recommended conditions, T_A =−40 °C to +85 °C, V_{IN+} = V_{IN-} = 0 V and V_{DD1} = V_{DD2} = 5.0 V, unless otherwise specified. All typical values are measured at T_A = 25 °C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	Figure
V_{OS}	Input Offset Voltage	TA = 25 °C	−2.0	−0.3	2.0		1, 3, 4
		−40 °C < T_A < +85 °C	−3.0		3.0	mV	1, 3, 4
$\lvert\Delta V_{os}/\Delta T_A\rvert$	Magnitude of Input Offset , Change vs. Temperature			2.0	10.0	µV/°C	3
G1	Gain (Rank A: ±1%)	−200 mV < V_{IN+} < 200 mV, T_A = 25 °C	7.92	8.03	8.08	V/V	5, 6
G2	Gain (Rank B: ±3%)		7.76	8.03	8.24		
G3	Gain (None: ±5%)		7.6	8.03	8.4		
$\lvert\Delta G/\Delta T_A\rvert$	Magnitude of V_{OUT} Gain Change vs. Temperature			0.0005		V/V/°C	
NL_{200}	V_{OUT} 200 mV Nonlinearity	−200 mV < V_{IN+} < 200 mV		0.0194	0.35	%	7, 8
$\lvert\Delta NL_{200}/\Delta T_A\rvert$	Magnitude of V_{OUT} 200 mV Nonlinearity Change vs. Temperature			0.0001		%/°C	
NL_{100}	V_{OUT} 100 mV Nonlinearity	−100 mV < V_{IN+} < 100 mV		0.0131	0.2	%	
$\lvert V_{IN+}\rvert_{MAX}$	Magnitude Input Voltage before V_{OUT} Clipping			315		mV	9
I_{DD1}	Input Supply Current	V_{IN+} = +400 mV		7.17	12.7	mA	10
I_{DD2}	Output Supply Current	V_{IN+} = −400 mV		4.10	10.9	mA	
I_{IN+}	Input Current			−0.4	5.0	µA	11
$\lvert\Delta I_{IN+}/\Delta T_A\rvert$	Magnitude of Input Bias Current vs. Temperature			+0.31		nA/°C	11
V_{OL}	Low Level Output Voltage			1.29		V	
V_{OH}	High Level Output Voltage			3.82		V	
V_{OCM}	Output Common-Mode Voltage		2.2	2.502	2.8	V	
$\lvert I_{OSC}\rvert$	Output Short-Circuit Current			15		mA	
R_{IN}	Equivalent Input Impedance			793		kΩ	
R_{OUT}	V_{OUT} Output Resistance			10		Ω	
$CMRR_{IN}$	Input DC Common-Mode Rejection Ratio			72		dB	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 7. DC ELECTRICAL CHARACTERISTICS (Gain Rank)

Device	Gain Rank	Min	Typ	Max	Unit
FOD7840A	Gain (Rank A: ±1%	7.92	8.03	8.08	V/V
FOD7840B	Gain (Rank B: ±3%)	7.76	8.03	8.24	
FOD7840	Gain (None: ±5%)	7.6	8.03	8.4	

Table 8. AC ELECTRICAL CHARACTERISTICS

Apply over all recommended conditions, T_A =−40 °C to +85 °C, V_{IN+} = V_{IN-} = 0 V and V_{DD1} = V_{DD2} = 5.0 V, unless otherwise specified. All typical values are measured at T_A = 25 °C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	Figure
BW	V_{OUT} Bandwidth (−3 dB)	V_{IN+} = 200 mVpk-pk. sine wave	50	100		kHz	12, 13
N_{OUT}	V_{OUT} Noise	V_{IN+} = 0 V		24		mV_{rms}	
t_{PD10}	V_{IN} to V_{OUT} Signal Delay (50 to 10%)	V_{IN+} = 0 mV to 150 mV step. Measured at output of OPA132 on Figure 15.		2.73	3.3	μs	14, 15
t_{PD50}	V_{IN} to V_{OUT} Signal Delay (50 to 50%)			4.22	5.6		
t_{PD90}	V_{IN} to V_{OUT} Signal Delay (50 to 90%)			6.10	9.9		
$t_{R/F}$	V_{OUT} Rise/Fall Time (10 to 90%)			3.41	6.6		
CMTI	Common Mode Transient Immunity	T_A = 25 °C, VCM = 1000 V	15			kV/μs	16
PSR	Power Supply Rejection	With recommended application circuit		112		mV_{rms}	

TYPICAL PERFORMANCE CHARACTERISTICS AND TEST CIRCUIT

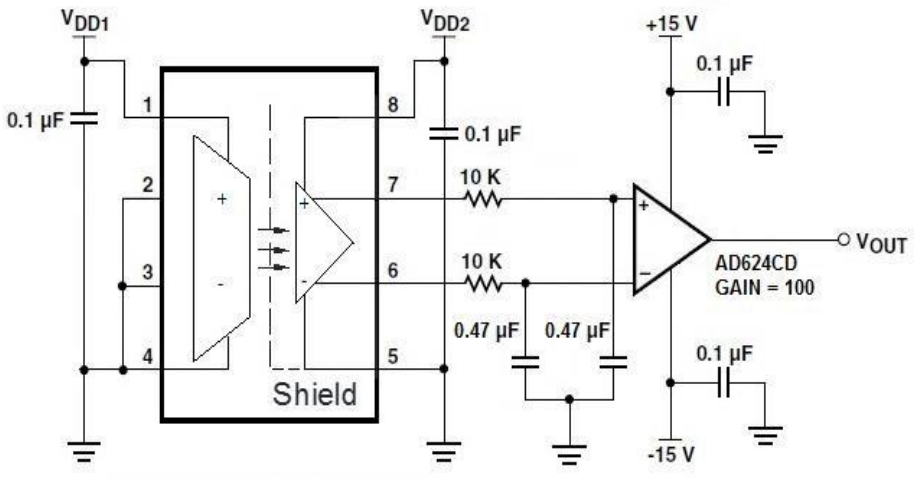


Figure 1. Input Voltage Test Circuit

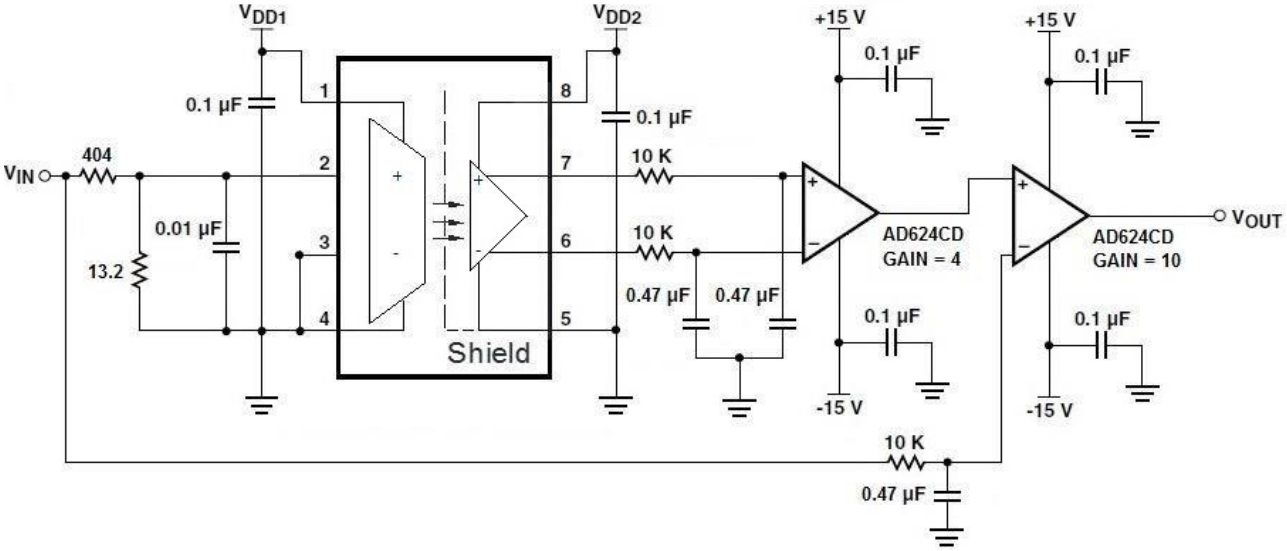


Figure 2. Gain and Nonlinearity Test Circuit

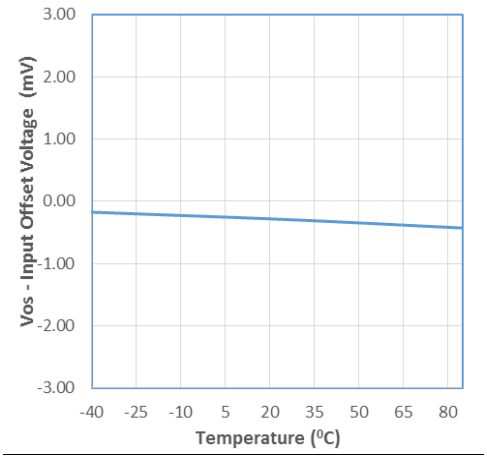


Figure 3. Input Offset Voltage vs. Temperature

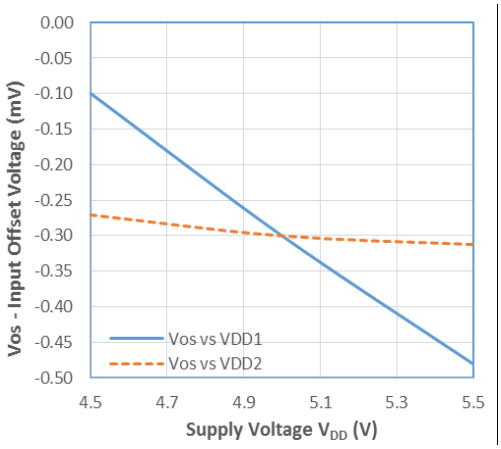


Figure 4. Input Offset Voltage vs. Supply

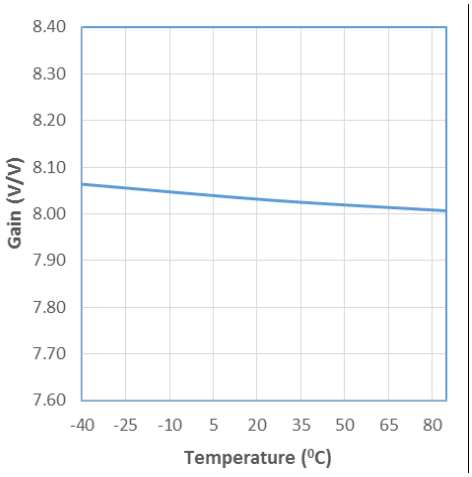


Figure 5. Gain vs. Temperature

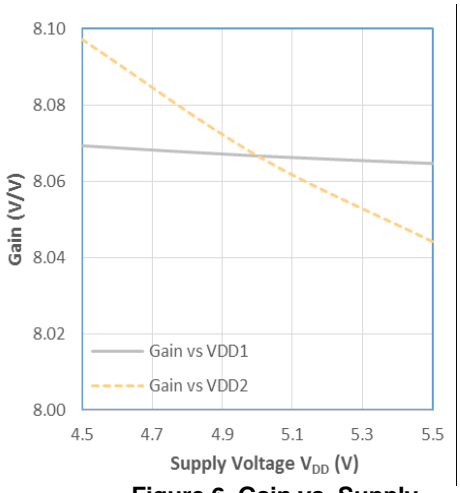


Figure 6. Gain vs. Supply

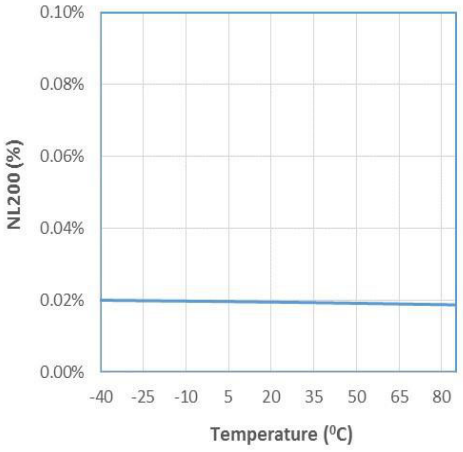


Figure 7. Nonlinearity vs. Temperature

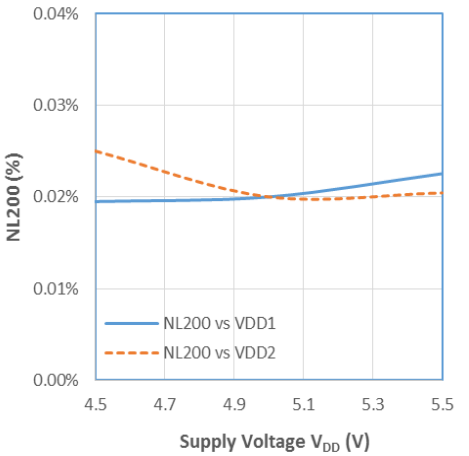


Figure 8. Nonlinearity vs. Supply

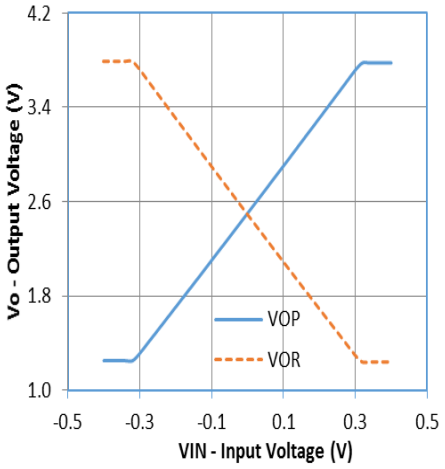


Figure 9. Output Voltage vs. Input Voltage

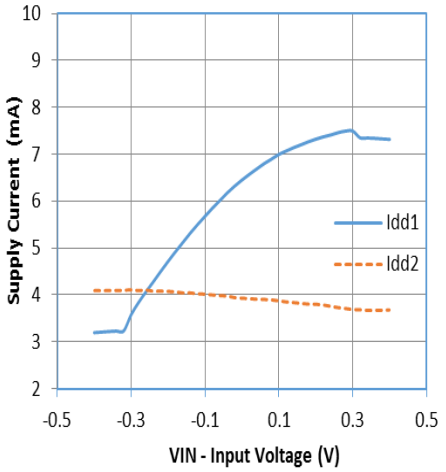


Figure 10. Supply Current vs. Input Voltage

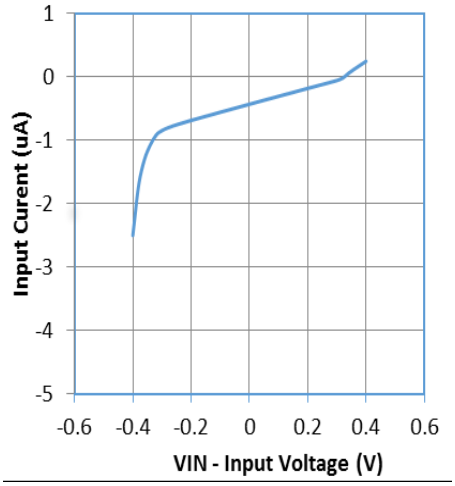


Figure 11. Input Current vs. Input

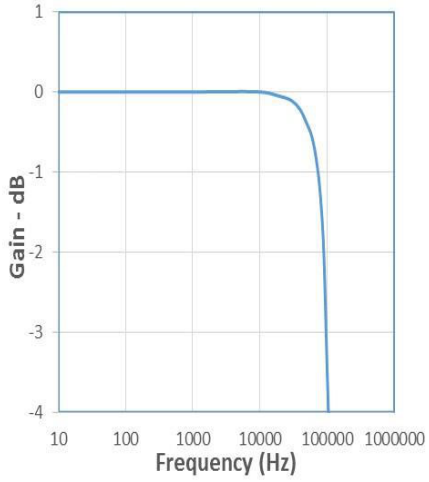


Figure 12. Supply Current vs. Input Voltage

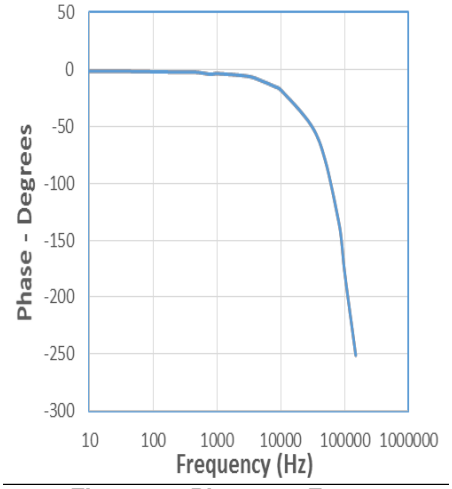


Figure 13. Phase vs. Frequency

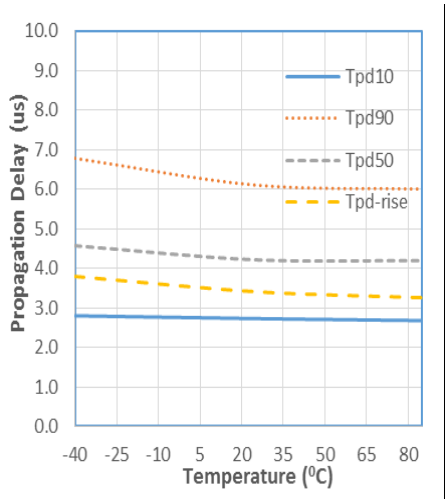


Figure 14. Propagation Delay vs. Temperature

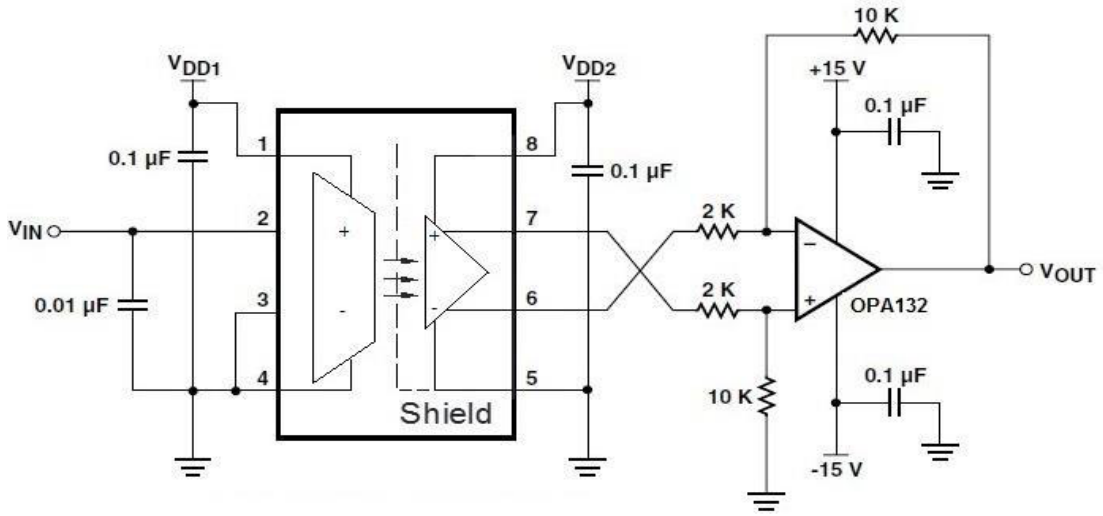


Figure 15. Propagation Delay Test Circuit

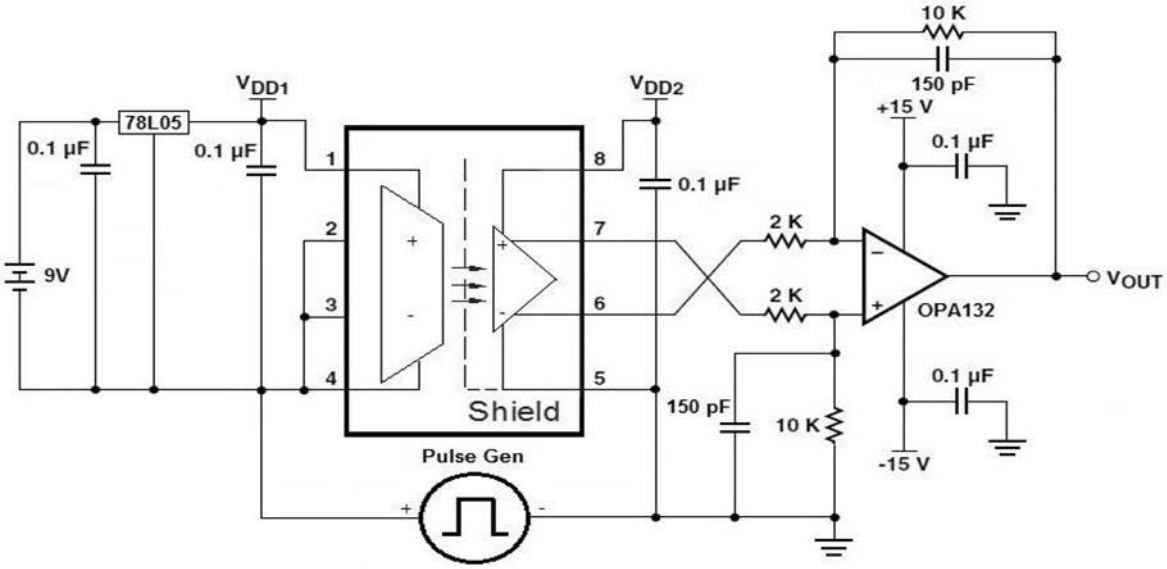


Figure 16. CMTI Test Circuit

REFLOW PROFILE

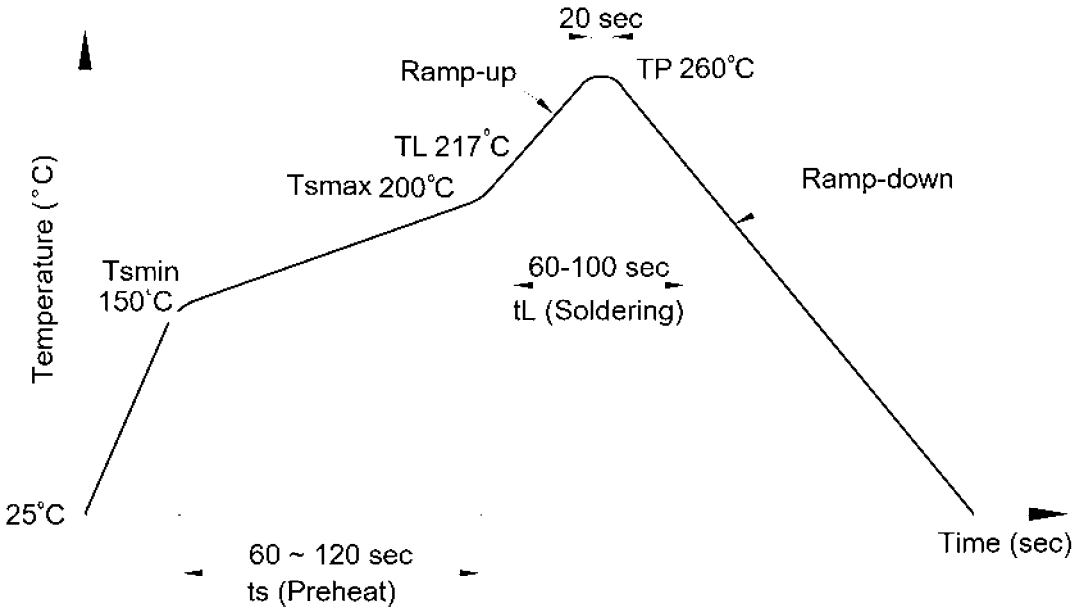


Figure 17.

Table 9. REFLOW PROFILE

Profile Feature	Pb-Free Assembly Profile
Temperature Min. (T_{smin})	150 °C
Temperature Max. (T_{smax})	200 °C
Time (t_S) from (T_{smin} to T_{smax})	60–120 s
Ramp-up Rate (t_L to t_P)	3 °C/s max.
Liquidous Temperature (T_L)	217 °C
Time (t_L) Maintained Above (T_L)	60–100 s
Peak Body Package Temperature	260 °C + 0 °C / –5 °C
Ramp-down Rate (T_P to T_L)	3–6 °C/s max.

Table 10. ORDERING INFORMATION

Part Number	Grade*	Package	Shipping†
FOD7840SV	none	SMT 8-Pin (Lead Bend), DIN EN/IEC60747-5-5 option	50 Units / Tube
FOD7840SD	none	SMT 8-Pin (Lead Bend)	1000 / Tape & Reel
FOD7840SDV	none	SMT 8-Pin (Lead Bend), DIN EN/IEC60747-5-5 option	1000 / Tape & Reel
FOD7840A	A	DIP 8-Pin	50 Units / Tube
FOD7840AV	A	DIP 8-Pin, DIN EN/IEC60747-5-5 option	50 Units / Tube
FOD7840ASV	A	SMT 8-Pin (Lead Bend), DIN EN/IEC60747-5-5 option	50 Units / Tube
FOD7840ASD	A	SMT 8-Pin (Lead Bend)	1000 / Tape & Reel
FOD7840ASDV	A	SMT 8-Pin (Lead Bend), DIN EN/IEC60747-5-5 option	1000 / Tape & Reel
FOD7840B	B	DIP 8-Pin	50 Units / Tube
FOD7840BV	B	DIP 8-Pin, DIN EN/IEC60747-5-5 option	50 Units / Tube
FOD7840BSV	B	SMT 8-Pin (Lead Bend), DIN EN/IEC60747-5-5 option	50 Units / Tube
FOD7840BSD	B	SMT 8-Pin (Lead Bend)	1000 / Tape & Reel
FOD7840BSDV	B	SMT 8-Pin (Lead Bend), DIN EN/IEC60747-5-5 option	1000 / Tape & Reel
FOD7840	none	DIP 8-Pin	50 Units / Tube
FOD7840V	none	DIP 8-Pin, DIN EN/IEC60747-5-5 option	50 Units / Tube

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

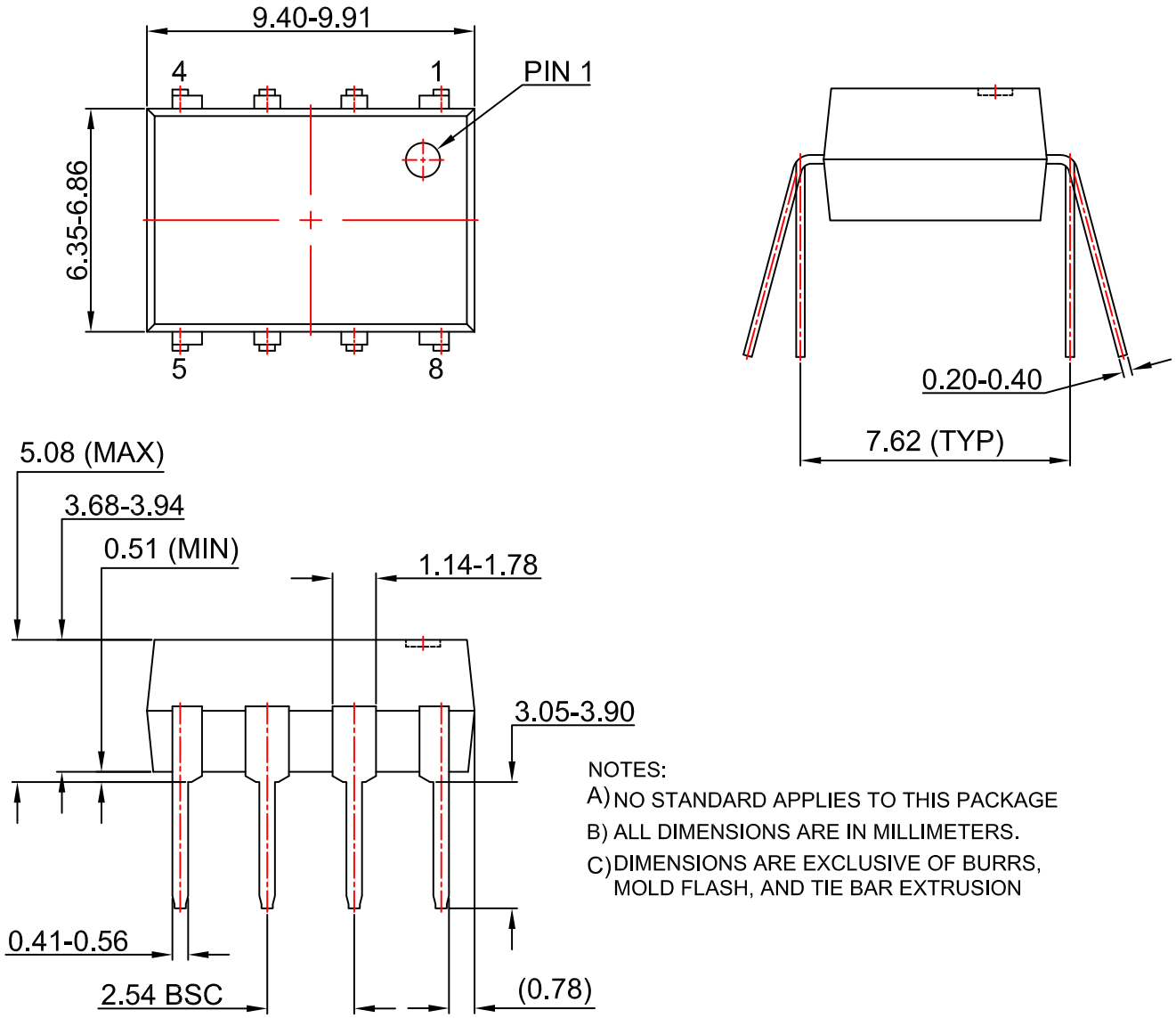
* Please Refer to Table 7.

REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial Preliminary document release.	2/4/2026
P1	Updated marking coding in marking diagram.	3/2/2026
0	Removed Case package options 646BW, 709AC & 709AD and added package option 709AF for initial document release.	4/17/2026

PDIP8 9.655x6.6, 2.54P
CASE 646CQ
ISSUE O

DATE 18 SEP 2017



NOTES:
A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

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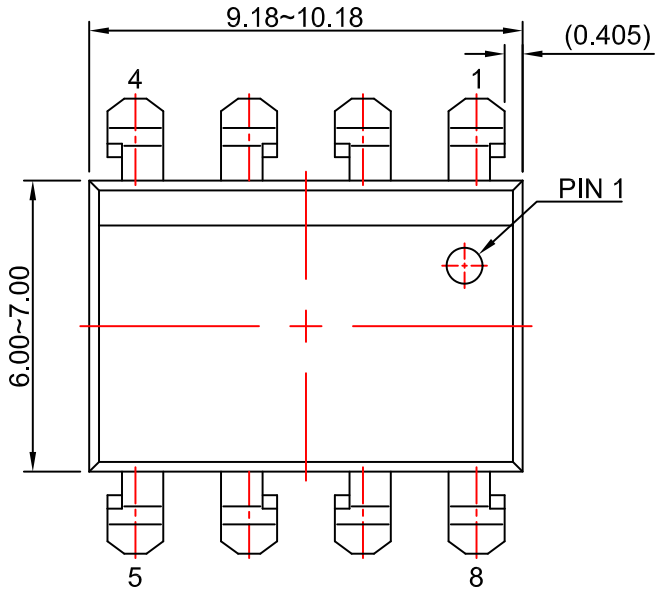
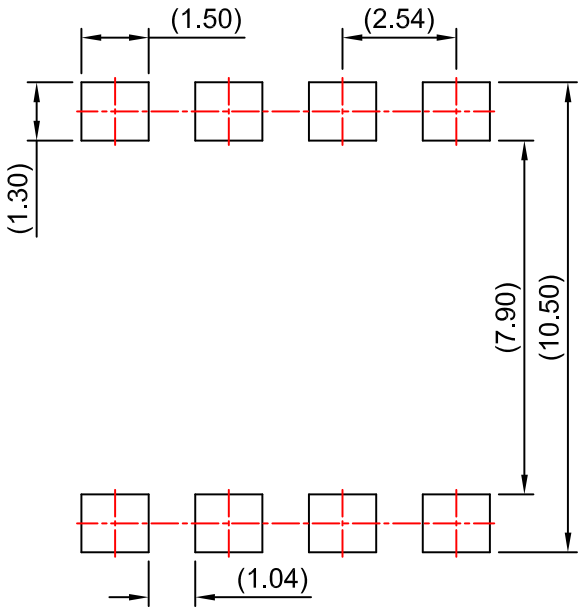
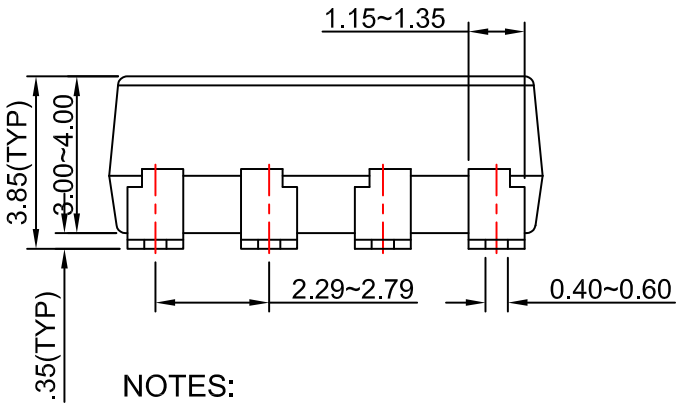
PDIP8 GW
CASE 709AF
ISSUE O

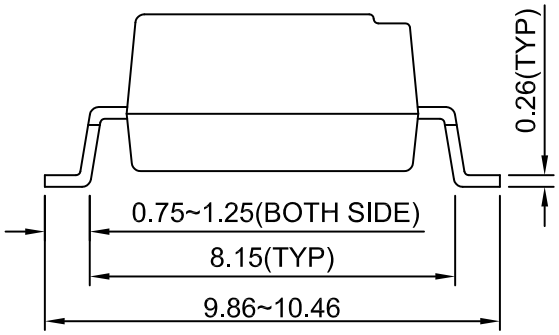
DATE 31 AUG 2016





LAND PATTERN RECOMMENDATION





NOTES:

A) NO STANDARD APPLIES TO THIS PACKAGE.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

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