

Integrated Load Switch

FDC6330L



TSOT-23-6
CASE 419BL

Description

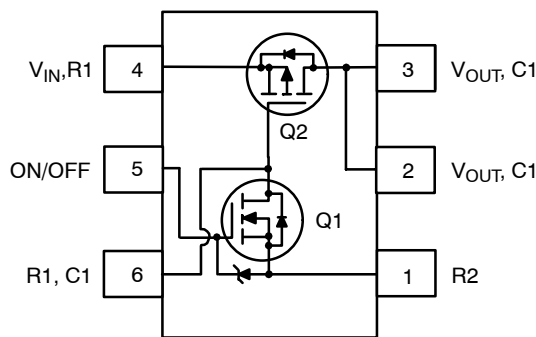
This device is particularly suited for compact power management in portable electronic equipment where 3 V to 20 V input and 2.3 A output current capability are needed. This load switch integrates a small N-Channel power MOSFET (Q1) which drives a large P-Channel power MOSFET (Q2) in one tiny SUPERSOT™-6 package.

Features

- $V_{DRO} = 0.20\text{ V @ } V_{IN} = 12\text{ V, } I_L = 2.5\text{ A, } R_{(on)} = 0.08\ \Omega$
- $V_{DRO} = 0.20\text{ V @ } V_{IN} = 5\text{ V, } I_L = 1.6\text{ A, } R_{(on)} = 0.125\ \Omega$
- Control MOSFET (Q1) Includes Zener Protection for ESD Ruggedness (> 6 kV Human Body Model)
- High Performance POWERTRENCH® Technology for Extremely Low On-Resistance
- SUPERSOT-6 Package Design Using Copper Lead Frame for Superior Thermal and Electrical Capabilities
- This is a Pb-Free and Halide Free Device

Application

- Power Management
- Load Actuation



See Application Circuit (Figure 2)

Figure 1.

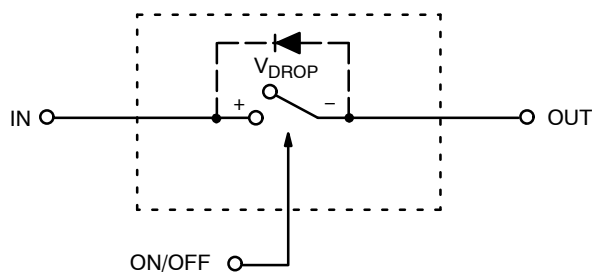
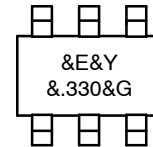


Figure 2. Equivalent Circuit

MARKING DIAGRAM



- &E = Designates Space
- &Y = Binary Calendar Year Coding Scheme
- &. = Pin One Dot
- 330 = Specific Device Code
- &G = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
FDC6330L	TSOT-23-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

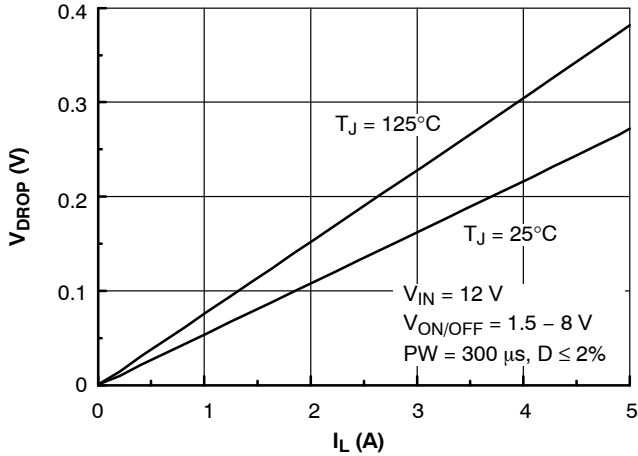


Figure 4. Conduction Voltage Drop Variation with Load Current

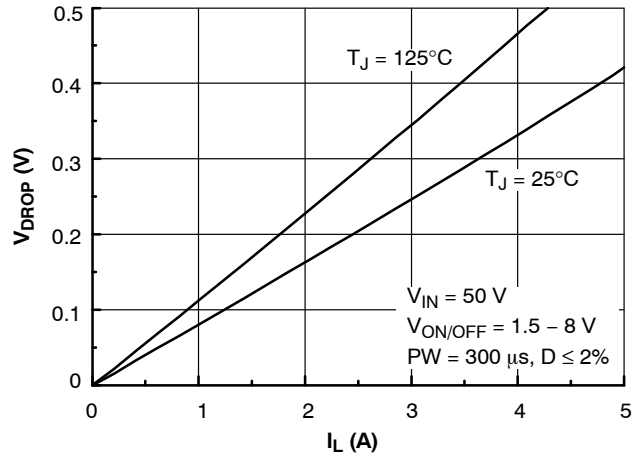


Figure 5. Conduction Voltage Drop Variation with Load Current

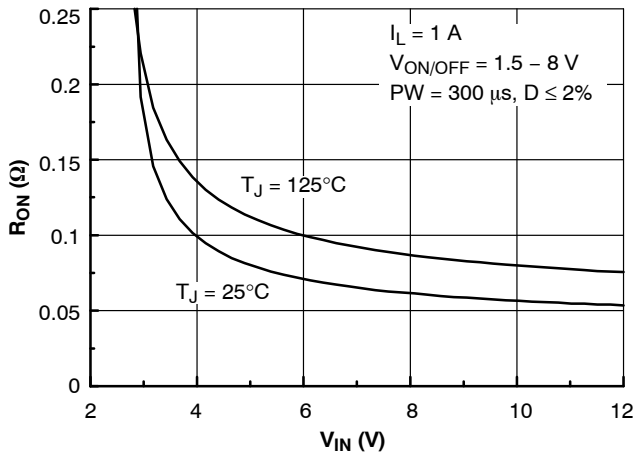


Figure 6. On-Resistance Variation with Input Voltage

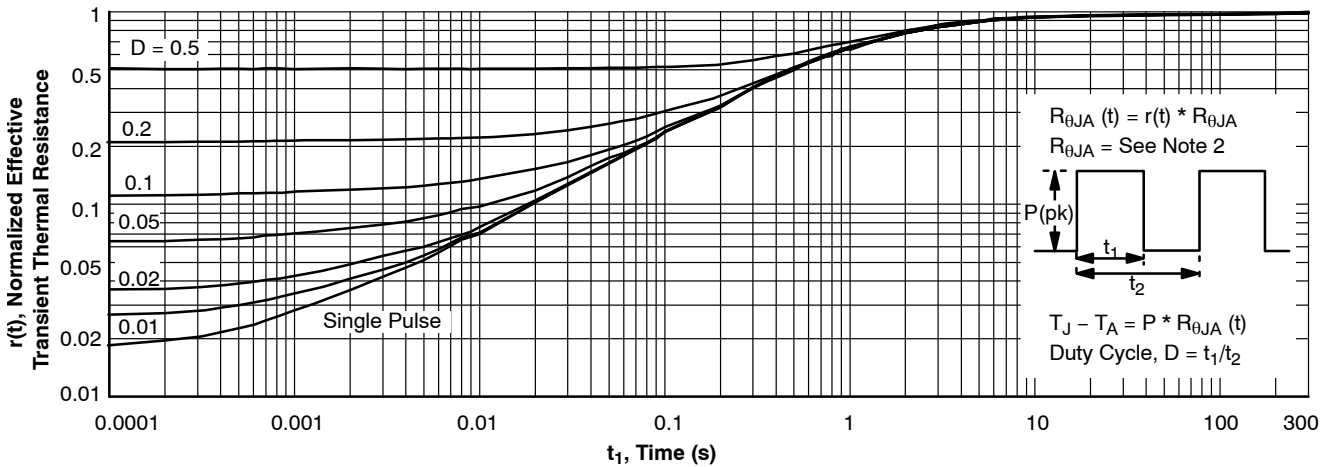


Figure 7. Transient Thermal Response Curve

NOTE: Thermal characterization performed on the conditions described in Note 2. Transient thermal response will change depending on the circuit board design.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

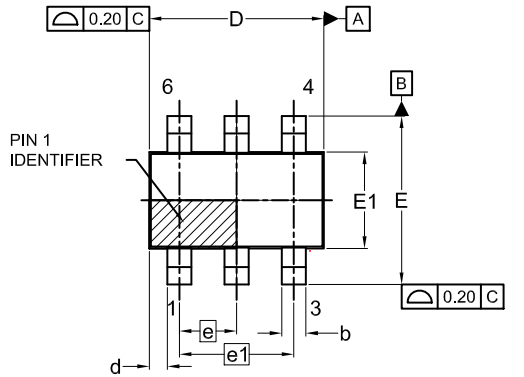
ON Semiconductor®



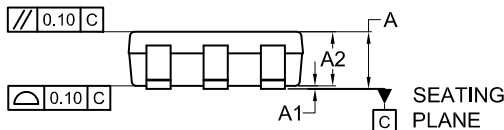
SCALE 2:1

TSOT23 6-Lead CASE 419BL ISSUE A

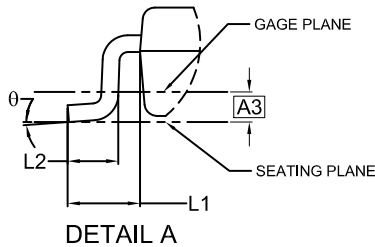
DATE 31 AUG 2020



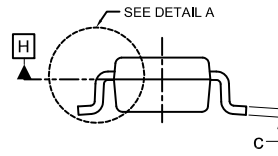
TOP VIEW



FRONT VIEW

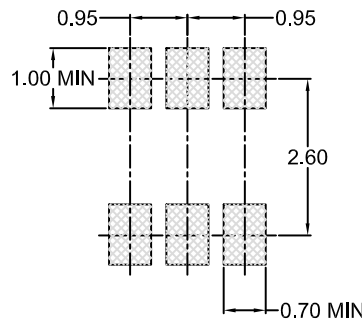


DETAIL A



SIDE VIEW

SYMM
⌀



LAND PATTERN
RECOMMENDATION

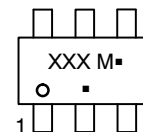
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
⌀	0°	--	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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